DIAMOND SYSTEMS CORPORATION

PROMETHEUS™

High Integration PC/104 CPU
with Ethernet and Data Acquisition

Models PR-Z32-E-ST, PR-Z32-EA-ST

User Manual V1.44

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TABLE OF CONTENTS

1. DESCRIPTION

Prometheus is an embedded PC/104 CPU that integrates 3 separate circuits onto a single compact board:

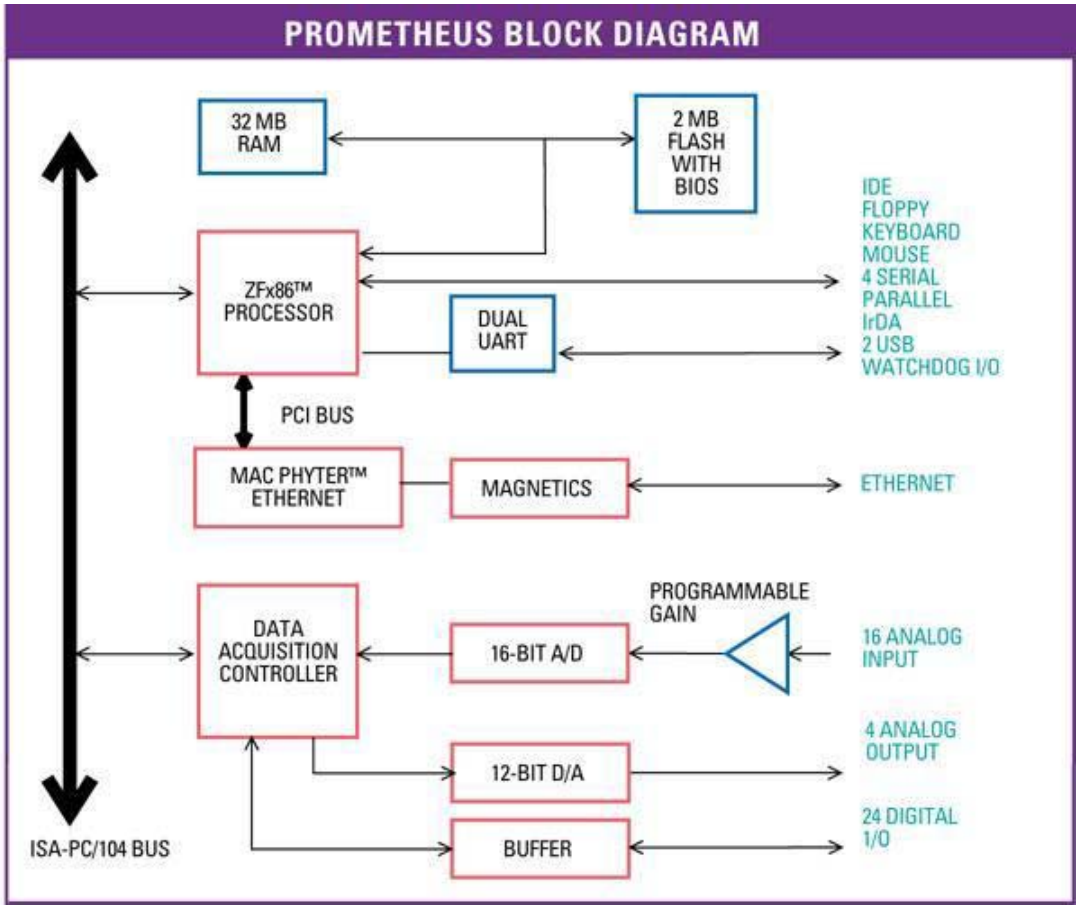
- CPU
- Ethernet
- Analog I/O (optional, model PR-Z32-EA only)

A detailed list of features is shown on the next page.

Prometheus conforms to the PC/104 standard, an embedded standard that is based on the ISA and PCI buses and provides a compact, rugged mechanical design for embedded systems. PC/104 modules feature a pin and socket connection system in place of card edge connectors, as well as mounting holes in each corner. The result is an extremely rugged computer system fit for mobile and miniature applications. PC/104 modules stack together with 0.6" spacing between boards (0.662" pitch including the thickness of the PCB). A mechanical drawing of a standard PC/104 board is shown on page 74.

For more information on PC/104, visit www.pc104.org.

Prometheus uses the PCI bus internally to connect the ethernet circuit to the processor. It uses the ISA bus internally to connect serial ports 3 and 4, as well as the data acquisition circuit, to the processor. Only the ISA bus is brought out to expansion connectors for the connection of add-on boards. Diamond Systems manufactures a wide variety of compatible PC/104 add-on board for analog I/O, digital I/O, counter/timer functions, serial ports, and power supply.



2. FEATURES

System Features

Processor Section

- 486-DX2 processor running at 100MHz with co-processor
- Pentium class platform including burst-mode SDRAM and PCI-based IDE controller and USB
- 32MB SDRAM system memory
- 50MHz memory bus for improved performance
- 2MB 16-bit wide integrated flash memory for BIOS and user programs
- 8KB unified level 1 cache

I/O

- 4 serial ports, 115.2kbaud max
- 2 ports 16550-compatible, 2 ports 16850-compatible with 128-byte FIFOs
- 2 full-featured powered USB ports
- 1 ECP-compatible parallel port
- Floppy drive connector
- IDE drive connector (44-pin version for notebook drives)
- Accepts solid-state flashdisk modules directly on board
- 100BaseT full-duplex PCI bus mastering Ethernet (100Mbps)
- IrDA port (requires external transceiver)
- PS/2 keyboard and mouse ports
- Speaker, LEDs

System Features

- Plug and play BIOS with IDE autodetection, 32-bit IDE access, and LBA support
- Built-in fail-safe boot ROM for system recovery in case of BIOS corruption
- User-selectable COM2 terminal mode
- On-board lithium backup battery for real-time-clock and CMOS RAM
- ATX power switching capability
- Programmable watchdog timer
- Power surge monitor for fail-safe operation
- Zero wait-state capability for flash memory and PC/104 bus
- +5V-only operation
- Extended temperature range operation (-40 to +85^{o}C)
- Cable-free operation when used with Diamond Systems' PNL-Z32 Panel I/O board

Data Acquisition Subsystem (Model PR-Z32-EA Only)

Analog Input

- 16 single-ended / 8 differential inputs, 16-bit resolution
- 100KHz maximum aggregate A/D sampling rate
- Programmable input ranges/gains with maximum range of ±10V / 0-10V
- Both bipolar and unipolar input ranges
- 5 ppm/^{o}C drift accuracy
- Internal and external A/D triggering
- 48-sample FIFO for reliable high-speed sampling and scan operation

Analog Output

- 4 analog outputs, 12-bit resolution
- ±10V and 0-10V output ranges
- Simultaneous update
- Adjustable output range (optional)

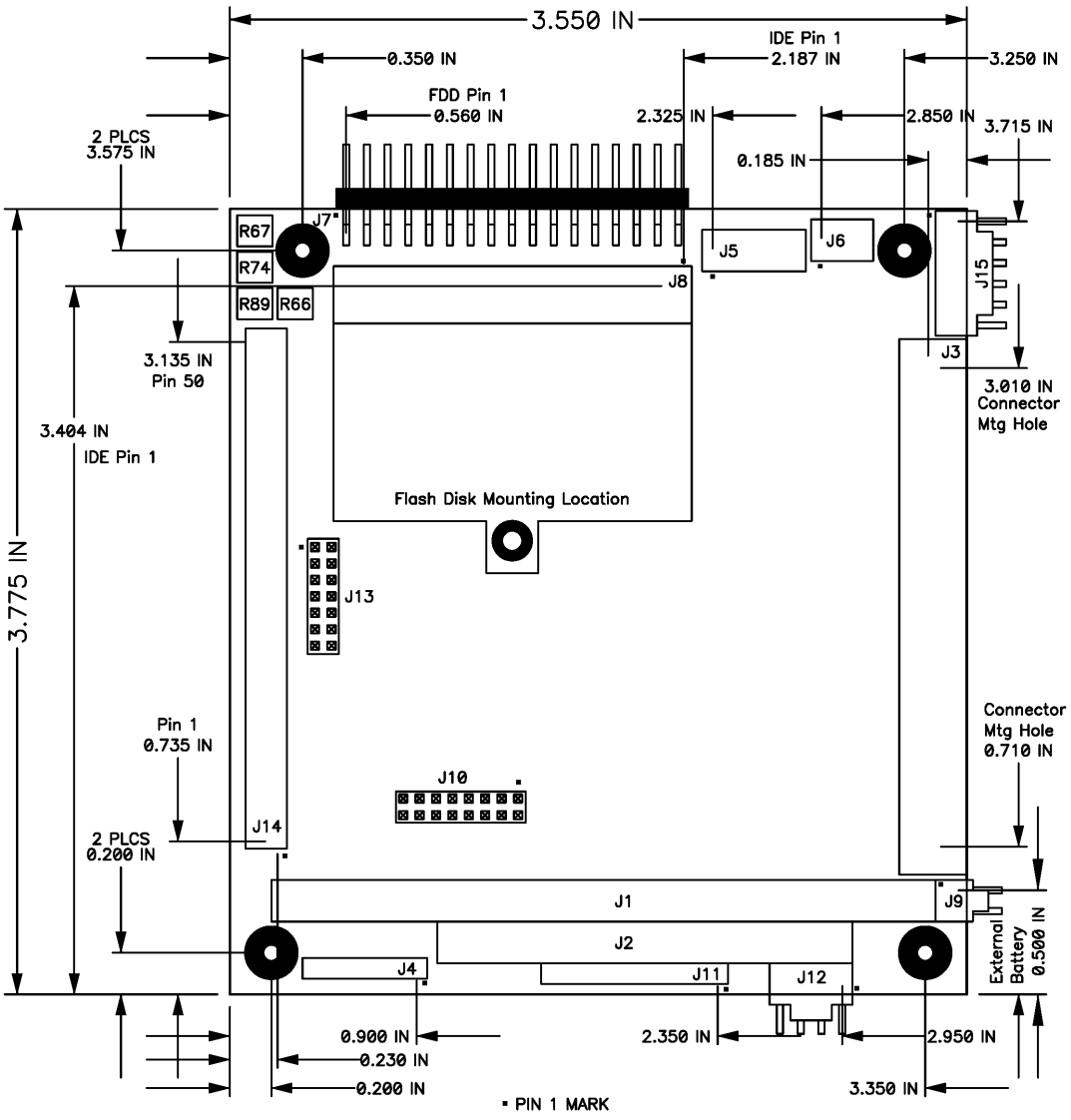
Digital I/O

- 24 programmable digital I/O, 3.3V and 5V logic compatible
- Enhanced output current capability: –8/+12mA max

Counter/Timers

- 1 24-bit counter/timer for A/D sampling rate control
- 1 16-bit counter/timer for user counting and timing functions
- Programmable gate and count enable
- Internal and external clocking capability

3. PROMETHEUS BOARD DRAWING



I/O Connectors

J1	PC/104 8-bit bus connector
J2	PC/104 16-bit bus connector
J3	Main user I/O connector
J4	Ethernet port
J5	Dual USB ports
J7	Floppy drive connector
J8	IDE drive connector
J11	Input power connector
J12	Switched output power connector
J14	Data acquisition I/O connector
J15	Auxiliary serial port connector

Configuration Jumper Blocks

J6	System recovery jumper block
J10	System configuration jumper block
J13	Data acquisition circuit configuration jumper block

4. I/O HEADERS

All cables mentioned in this chapter are included in Diamond Systems' cable kit **C-PRZ-KIT**. These cables are further described in chapter 25. Some cables are also available individually.

4.1 Main I/O Connector – J3

An 80-pin high-density connector is provided for access to the standard user I/O:

- 4 serial ports
- Parallel port
- Watchdog timer I/O
- PS/2 keyboard
- PS/2 mouse
- IrDA port
- ATX Power switch
- Reset switch
- Power and HDD LEDs

This connector mates with Diamond Systems' cable no. **C-PRZ-01**, which consists of a dual-ribbon-cable assembly with industry-standard connectors at the user end. The CPU mating connector includes integral latches for enhanced reliability. Each ribbon cable has 40 wires.

Group	Cable "A" Pin	Cable "A" Signal	Group	Cable "B" Pin	Cable "B" Signal
COM 1	1	DCD1	LPT 1	1	STB-
	2	DSR 1		2	AFD-
	3	RXD 1		3	PD0
	4	RTS 1		4	ERR-
	5	TXD 1		5	PD1
	6	CTS 1		6	INIT-
	7	DTR 1		7	PD2
	8	RI 1		8	SLIN-
	9	Ground		9	PD3
COM 2	10	DCD 2		10	Ground
	11	DSR 2		11	PD4
	12	RXD 2		12	Ground
	13	RTS 2		13	PD5
	14	TXD 2		14	Ground
	15	CTS 2		15	PD6
	16	DTR 2		16	Ground
	17	RI 2		17	PD7
	18	Ground		18	Ground
COM 3	19	DCD 3		19	ACK-
	20	DSR 3		20	Ground
	21	RXD 3		21	BUSY
	22	RTS 3		22	Ground
	23	TXD 3		23	PE
	24	CTS 3		24	Ground
	25	DTR 3		25	SLCT
	26	RI 3	Keyboard	26	KB Clk
	27	Ground		27	KB/MS V-
COM 4	28	DCD 4		28	KB Data
	29	DSR 4		29	KB/MS V+
	30	RXD 4	Mouse	30	MS Clk
	31	RTS 4		31	KB/MS V-
	32	TXD 4		32	MS Data
	33	CTS 4		33	KB/MS V+
	34	DTR 4	Utilities B	34	Ground
	35	RI 4		35	Reset-
	36	Ground		36	ATX Power
Utilities A	37	+5V Out		37	KB Lock
	38	Speaker Out		38	IR RX
	39	IDE Drive LED		39	IR TX
	40	Power LED		40	+5V In

Notes on J3 Signals

COM1 – COM4	The signals on these pins are RS-232 level signals and may be connected directly to RS-232 devices. The pinout of these signals is designed to allow a 9-pin male IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC serial port connector (DTE).
LPT1	The signals on these pins comprise a standard PC parallel port. The pinout of these signals is designed to allow a 25-pin female IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC parallel port connector.
Keyboard, Mouse	These are PS/2 signals for keyboard and mouse.
Clk	Clock pin; connects to pin 5 of the PS/2 connector.
V-	Power pin; connects to pin 3 of the PS/2 connector.
Data	Data pin; connects to pin 1 of the PS/2 connector.
V+	Power pin; connects to pin 4 of the PS/2 connector.
	Pins 2 and 6 on the Mini-Din-6 PS/2 connectors are unused.
Utilities A	
+5V Out	This pin is a switched power pin that is turned on and off with the ATX power switch or with the +5V input.
Speaker Out	The signal on this pin is referenced to +5V Out. Connect a speaker between this pin and +5V Out.
IDE Drive LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
Power LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
Utilities B	
Reset-	Connection between this pin and Ground will generate a Reset condition.
ATX Power	When ATX is enabled, a momentary contact between this pin and Ground causes the CPU to turn on, and a contact of 4 seconds or longer will generate a power shutdown. ATX power control is enabled with a jumper on jumper block J10 (see page 16).
KB Lock	When this pin is connected to Ground, the keyboard and mouse inputs are ignored.
IR RX, IR TX	IrDA pins. Can be connected directly to an IrDA transceiver.
+5V In	Connected to +5V input power on J11 (see page 10). This pin is not switched by ATX control. This pin is provided for auxiliary use such as front panel lighting or other circuitry at the user's discretion.

Connector Part Numbers

J3 plug on CPU board: 3M / Robinson Nugent no. P50E-080P1-S1-TG

Both cable-mount and board-mount connectors are available to mate with J3:

Cable-mount socket: 3M / Robinson Nugent no. P50E-080S-TG

Board-mount socket: 3M / Robinson Nugent no. P50-080S-R1-TG

4.2 Input Power – J11

1	+5V In
2	Ground
3	Ground
4	+12V In
5	Ground
6	+5V In
7	-12V In
8	-5V In
9	ATX Control

Input power for Prometheus may be supplied either through J11 from an external supply or directly through the PC/104 bus power pins if a PC/104 power supply is used with the CPU.

Prometheus requires only +5VDC input power to operate. All other required voltages are generated on board with miniature switching regulators. However since the PC/104 bus includes pins for ±5V and ±12V, these voltages may be supplied through J11 if needed. The +5V and +12V voltages are controlled by the ATX power manager switches, while -5V and -12V are routed directly to the corresponding pins on PC/104 bus and are not controlled by the ATX function.

Make sure that the power supply used has enough current capacity to drive your system. The Prometheus CPU requires up to 1.1A on the +5V line. If you have a disk drive or other modules connected, you need additional power. In particular, many disk drives need extra current during startup. If your system fails to boot properly, or if disk accesses do not work properly, the first thing to check is the power supply voltage level. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the +5V supply.

Multiple +5V and Ground pins are provided for extra current carrying capacity if needed. Each pin is rated at 3A max (15W). For the Prometheus CPU, the panel I/O board, and a video board, 3A is sufficient, so +5 and Ground require only a single wire each. In this case the first 4 pins may be connected to a standard 4-pin miniature PC power connector if desired.

For a larger PC/104 stack the total power requirements should be calculated to determine whether additional wires are necessary.

ATX control enables the +5V and +12V power to be switched on and off with an external momentary switch. A short press on the switch will turn on power, and holding the switch on for 4 seconds or longer will turn off power.

Diamond Systems' cable no. **698009** mates with J11. It provides 9 color-coded wires with stripped and tinned leads for connection to user-supplied power sources. This cable may also be used with Diamond Systems' Jupiter-MM series power supplies in vehicle-based applications. In this configuration, the input power is supplied to the Jupiter-MM board, and the Jupiter-MM output power is connected to J11 on the CPU using cable 698009. When used in this way, make sure the two red +5V wires are both connected to the +5V output screw terminal on Jupiter-MM.

4.3 Output Power – J12

1	+5V Out
2	Ground
3	Ground
4	+12V Out

J12 provides switched power for use with external drives. If ATX is enabled, the power is switched on and off with the ATX input switch. If ATX is not enabled, the power is switched on and off in conjunction with the external power.

Diamond Systems' cable no. **698006** mates with J12. It provides a standard full-size power connector for a hard drive or CD-ROM drive and a standard miniature power connector for a floppy drive.

4.4 Ethernet – J4

1	Common
2	RX-
3	Common
4	RX+
5	TX-
6	TX+

J4 is a 1x6 pin header. It mates with Diamond Systems' cable no. **698002**, which provides a panel-mount RJ-45 jack for connection to standard CAT5 network cables.

4.5 USB – J5

Key (pin cut)	1	2	Shield
USB2 Pwr-	3	4	USB1 Pwr-
USB2 Data+	5	6	USB1 Data+
USB2 Data-	7	8	USB1 Data-
USB2 Pwr+	9	10	USB1 Pwr+

J5 is a 2x5 pin header. It mates with Diamond Systems' cable no. **698012**, which provides 2 standard USB type A jacks in a panel-mount housing.

4.6 Auxiliary Serial Port Connector – J15

1	RX COM1	Pin 2 on DB9 #1
2	TX COM1	Pin 3 on DB9 #1
3	Ground	Pin 5 on DB9 #1
4	RX COM2	Pin 2 on DB9 #2
5	TX COM2	Pin 3 on DB9 #2
6	Ground	Pin 5 on DB9 #2

This 6-pin header is provided for auxiliary access to serial ports 1 and 2 with signals RX, TX, and Ground for each port. This connector may be used in low-cost limited I/O configurations as an alternative to the 80-pin connector J3.

Do not use both J15 and the corresponding pins on J3 simultaneously.

Diamond Systems' cable no. **698005** converts the 6 pins to two standard DB9M connectors with industry-standard pinout for RS-232 DTE.

4.7 Watchdog/Failsafe Features – J6

ZFIX	1	2	Ground
+3.3V	3	4	WDI
PRST-	5	6	WDO

J6 serves two main functions. It is used for watchdog timer access, and it is used to enable the ZFx86 failsafe feature (ZFIX mode) for reprogramming the BIOS or downloading files to the flash memory. J6 also contains a reset indicator signal PRST- that goes low for 200ms whenever a system reset occurs.

When the CPU is installed with a Panel Board, the failsafe feature is activated with a momentary switch on the panel board labeled ZFIX, and the watchdog timer feature is accessed with header J9 on the upper right edge of the panel board.

The watchdog timer circuit is described on page 20 of this manual. It may be programmed directly, as described in the ZFx86 training manual included with the Prometheus documents, or with Diamond Systems' Universal Driver software.

The failsafe feature is described on page 21 of this manual.

4.8 Floppy Drive – J7

Ground	1	2	High Density
Ground	3	4	Unused
Ground	5	6	Unused
Ground	7	8	Index
Ground	9	10	Motor Enable
Ground	11	12	Drive Select B
Ground	13	14	Drive Select A
Ground	15	16	Motor Enable
Ground	17	18	Direction
Ground	19	20	Step
Ground	21	22	Write Data
Ground	23	24	Write Enable
Ground	25	26	Track 0
Ground	27	28	Write Protect
Ground	29	30	Read Data
Ground	31	32	Select Protect
Ground	33	34	Disk Change

J7 is a 2x17 pin header. It mates with Diamond Systems' cable no. **698008** or any standard floppy drive interface cable. Up to two floppy drives can be connected. The connector furthest away from the others is used to connect to the board. The connector at the far end of the cable (after the twist) is for Drive A, and the middle connector is for Drive B.

4.9 IDE Drive – J8

RESET-	1	2	Ground
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
Ground	19	20	Key (Not Used)
DRQ	21	22	Ground
IDEIOW-	23	24	Ground
IDEIOR-	25	26	Ground
IORDY	27	28	Ground
DACK-	29	30	Ground
IRQ14	31	32	Pulled low for 16-bit operation
A1	33	34	Not Used
A0	35	36	A2
CS0-	37	38	CS1-
LED-	39	40	Ground
+5V	41	42	+5V
Ground	43	44	Not Used

J8 is a 2x22 (44-pin) 2mm-pitch pin header. It mates with Diamond Systems' cable no. **698004**, and may be used to connect up to 2 IDE drives (hard disks, CD-ROMs, or flashdisk modules). The 44-pin connector includes power and mates directly with notebook drives and flashdisk modules. To use a standard format hard disk or CD-ROM drive with a 40-pin connector, an adapter PCB such as Diamond Systems' ACC-IDEEXT is required.

4.10 Data Acquisition I/O Connector – J14 (Model PR-Z32-EA only)

Prometheus model PR-Z32-EA includes a 50-pin header labeled J14 for all data acquisition I/O. This header is located on the left side of the board. Pin 1 is the lower right pin and is marked on the board. Diamond Systems' cable no. **C-50-18** provides a standard 50-pin connector at each end and mates with this header.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4 / Gate 0	21	22	DIO C5 / Gate 1
DIO C6 / Clk 1	23	24	DIO C7 / Out 0
Ext Trig	25	26	Tout 1
+5V Out	27	28	Dground
Vout 0	29	30	Vout 1
Vout 2	31	32	Vout 3
Aground (Vout)	33	34	Aground (Vin)
Vin 0	35	36	Vin 8
Vin 1	37	38	Vin 9
Vin 2	39	40	Vin 10
Vin 3	41	42	Vin 11
Vin 4	43	44	Vin 12
Vin 5	45	46	Vin 13
Vin 6	47	48	Vin 14
Vin 7	49	50	Vin 15

Signal Name	Definition
DIO A7-A0	Digital I/O port A; programmable direction
DIO B7-B0	Digital I/O port B; programmable direction
DIO C7-C0	Digital I/O port C; programmable direction C7-C4 may be configured for counter/timer signals; see page 41
Ext Trig	External A/D trigger input
Tout 1	Counter/Timer 1 output
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 – 0 in single-ended mode; High side of input channels 7 – 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 – 8 in both single-ended mode; Low side of input channels 7 – 0 in differential mode
Vout0-3	Analog output channels 0 – 3
+5V Out	Connected to switched +5V supply
Aground (Vout), (Vin)	Analog ground; used for analog circuitry only Vout pin is for the analog outputs; Vin pin is for the analog inputs
Dground	Digital ground; used for digital circuitry only

4.11 PC/104 Bus Connectors

The PC/104 bus is essentially identical to the ISA Bus except for the physical design. It specifies two pin and socket connectors for the bus signals. A 64-pin header J1 incorporates the 62-pin 8-bit bus connector signals, and a 40-pin header J2 incorporates the 36-pin 16-bit bus connector signals. The additional pins on the PC/104 connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104 board on top of the board, while the male pins on the bottom enable the board to plug into another board below it.

In the pinout figures below, the tops correspond to the left edge of the connector when the board is viewed from the primary side (side with the CPU chip and the female end of the PC/104 connector) and the board is oriented so that the PC/104 connectors are along the bottom edge of the board.

View from Top of Board

J2: PC/104 16-bit bus connector

Ground	D0	C0	Ground
MEMCS16-	D1	C1	SBHE-
IOCS16-	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0-	D8	C8	LA17
DRQ0	D9	C9	MEMR-
DACK5-	D10	C10	MEMW-
DRQ5	D11	C11	SD8
DACK6-	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7-	D14	C14	SD11
DRQ7	D15	C15	SD12
+5V	D16	C16	SD13
MASTER-	D17	C17	SD14
Ground	D18	C18	SD15
Ground	D19	C19	Key (pin cut)

J1: PC/104 8-bit bus connector

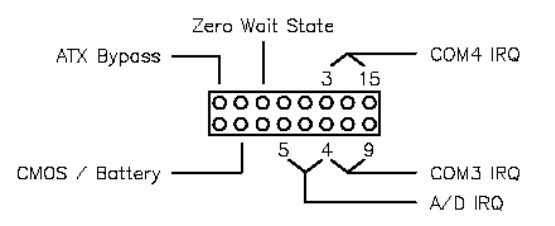
IOCHCHK-	A1	B1	Ground
SD7	A2	B2	RESET
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	Key (pin cut)
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	Refresh-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	Ground
Ground	A32	B32	Ground

5. JUMPER CONFIGURATION

Refer to the Prometheus board drawing on page 7 for locations of the configuration items mentioned here. Also see page 45 for information on configuration J13 for the data acquisition circuit.

5.1 J10: System Configuration

Jumper block J10 is used for configuration of IRQ levels, wait states, ATX power control, and CMOS RAM.



Serial Port and A/D IRQ Settings

COM3 may be set to IRQ4 or IRQ9. COM4 may be set to IRQ3 or IRQ15. The A/D circuit (on model PR-Z32-EA) may be set to IRQ5 or IRQ4 if COM3 does not use it. In addition, it is possible to set up all 3 circuits to share IRQ4 or IRQ5.

Wait States

The ISA bus may be configured for standard wait states or zero wait states. In most configurations and board combinations, the zero wait state setting will work properly and provide faster performance. However it should be tested in your application to verify correct operation. In standard configuration, the CPU issues 2 wait states for 16-bit cycles and 3 wait states for 8-bit cycles.

ATX Power Control

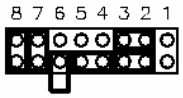
The ATX power control is set with this jumper block. If the ATX jumper is out, ATX works normally; an external momentary switch may be used to turn power on and off. A quick contact turns the power on, and a long contact (> 4 seconds) turns the power off. If the ATX jumper is in, the ATX function is bypassed and the system will power up as soon as power is connected.

Erasing CMOS RAM

The CMOS RAM may be cleared with a jumper as shown on the next page. This will cause the CPU to power up with the default BIOS settings. To clear the CMOS RAM, power down the CPU, install the jumper as shown, return it to its default position, and then power up again.

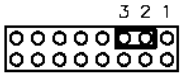
Before erasing CMOS RAM, write down any custom BIOS settings you have made!

Default Settings

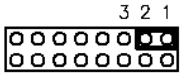


Default Settings:
COM3 = IRQ4
COM4 = IRQ3
A/D = IRQ5
Standard ISA bus wait state
Backup battery enabled
ATX bypass

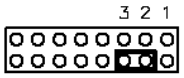
The different configurations for J10 are shown below. Each illustration shows only the jumper of interest. An asterisk (*) indicates the default setting.



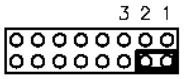
COM4 = IRQ3 *



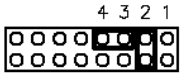
COM4 = IRQ15



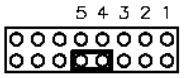
COM3 = IRQ4 *



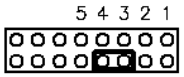
COM3 = IRQ9



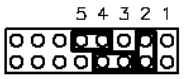
COM3 & COM4 = IRQ3



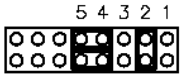
A/D = IRQ5 *



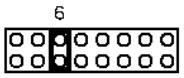
A/D = IRQ4



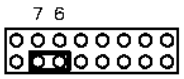
COM3 & COM4 & A/D = IRQ4



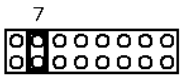
COM3 & COM4 & A/D = IRQ5



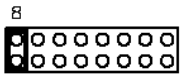
Zero Wait State



Clear CMOS RAM / Battery Disconnected



Backup Battery Enabled *



In=ATX Bypass *
Out = ATX Enabled

5.2 J6: Watchdog Timer & System Recovery

J6 is used to configure the watchdog timer and enable system recovery (failsafe mode) in case of BIOS corruption. This jumper has different dimensions than J10 and J13, and the jumpers are not interchangeable.

Watchdog timer operation is described in detail on page 20.

Failsafe mode operation is described on page 21.

6. SYSTEM FEATURES

6.1 System Resources

The table below lists the default system resources utilized by the circuits on Prometheus.

Device	Address (Hex)	IRQ	DMA
Serial Port COM1	I/O 3F8-3FF	4	-
Serial Port COM2	I/O 2F8 – 2FF	3	-
Serial Port COM3	I/O 3E8 – 3EF	4	-
Serial Port COM4	I/O 2E8 – 2EF	3	-
Parallel Port LPT1	I/O 378 – 37F	7	3
IDE Controller	I/O 1F0 – 1F7	14	-
Floppy Controller			-
A/D Circuit (PR-Z32-EA only)	I/O 280 – 28F	5	-
Ethernet	I/O 1000	10	-
USB		11	-

6.2 CPU Chip Selects

The ZF Micro CPU chip contains 4 user-configurable I/O chip selects and 4 user-configurable memory chip selects. These chip selects are visible in the BIOS setup screens. Three of the I/O chip selects are used by the Prometheus design. Chip selects 1 and 2 are used for the two serial ports COM3 and COM4. Chip select 3 is used by the data acquisition circuitry on model PR-Z32-EA. Chip select 0 is not used.

Chip Select	Function	Mode	Address Range	I/O Size	Window Size
0	Not used	--	--	--	--
1	COM3	R/W	3E8 – 3EF	8 bits	8 bytes
2	COM4	R/W	2E8 – 2EF	8 bits	8 bytes
3	Data Acquisition	R/W	280 – 28F	8 bits	16 bytes

These chip select settings should not be modified unless you need to change the addresses of one or more of the affected circuits for a special system configuration and are fully aware of the impact of your changes.

6.3 Console Redirection to a Serial Port

In many applications without a video card it may be necessary to obtain keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Prometheus supports this operation by enabling keyboard input and character output onto a serial port (console redirection). A serial port on another PC can be connected to the serial port on Prometheus with a null modem cable, and a terminal emulation program (such as Hyperterminal) can be used to establish the connection. The terminal program must be capable of transmitting special characters including F2 (some programs or configurations trap special characters).

The default Prometheus BIOS setting enables console redirection onto COM2 during POST (power on self-test). The communication parameters are 115.2Kbaud, N, 8, 1. When the CPU is powered up, the BIOS will output POST information to COM2 and monitor it for any keyboard activity. You can enter the BIOS by pressing F2 during this time. In the default configuration, after POST is finished and the CPU boots, console redirection is disabled.

There are three possible configurations for console redirection:

- POST only (default)
- Always On
- Disabled

To modify the console redirection settings, enter the BIOS, select the Advanced menu, and then select Console Redirection. In Com Port Address, select Disabled to disable the function, On-board COM A for COM1, or On-board COM B for COM2 (default).

If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port. To reenter BIOS when console redirection is disabled, you must either install a PC/104 video board and use a keyboard and terminal or erase the CMOS RAM, which will return the BIOS to its default settings. CMOS RAM may be erased by moving a jumper. See page 16 for instructions.

Before erasing CMOS RAM, write down any custom BIOS settings you have made!

If you erase the CMOS RAM, the next time the CPU powers up COM2 will return to the default settings of 115.2Kbaud, N, 8, 1 and operate only during POST.

If you selected COMA or COMB, then continue with the configuration:

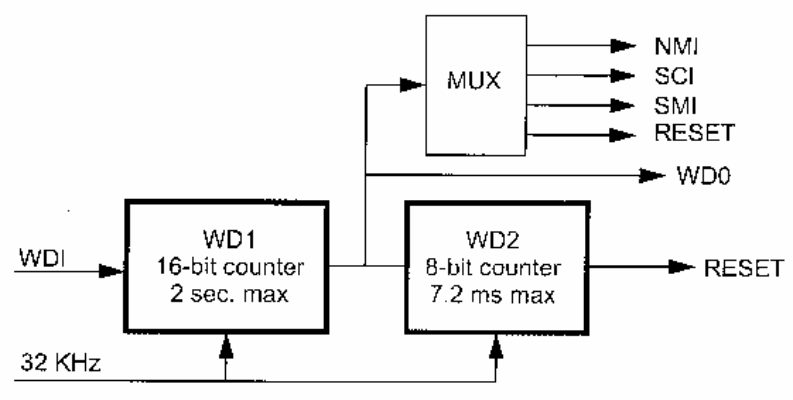
For Console Type select PC ANSI. You can modify the baud rate and flow control here if desired.

At the bottom, for Continue C.R. after POST, select Off (default) to turn off after POST or select On to remain on always.

Exit the BIOS and save your settings.

6.4 Watchdog Timer

Prometheus contains a watchdog timer circuit consisting of two programmable timers, WD1 and WD2, cascaded together. The input to the circuit is WDI, and the output is WDO. Both signals appear on I/O connector WDI may be triggered in hardware or in software. A special “early” version of WDO may be output on the WDO pin. When this signal is connected to WDI, the watchdog circuit will be retriggered automatically. A block diagram is provided here:



The duration of each timer is user-programmable. When WD1 is triggered, it begins to count down. When it reaches zero, it triggers WD2 and may also generate a user-selectable combination of these events:

- Non-maskable interrupt (NMI)
- System controller interrupt (SCI)
- System Management interrupt (SMI)
- Hardware reset

WD2 then begins to count down. When WD2 counter reaches zero, it will unconditionally cause a hardware reset. The WD2 timer is provided to give external circuits time to respond to the WDO event before the hardware reset occurs.

The watchdog timer circuit is programmed via I/O registers 0CH through 12H. Detailed programming information is in the ZFx86 Training Manual included in the Documents folder of the Prometheus CD. The watchdog timer is supported in the DSC Universal Driver software version 5.1 and later.

6.5 Failsafe Mode / BIOS Recovery

The ZFx86 failsafe feature consists of a small command interpreter built in to the ZFx86 CPU chip. The ZFx86 contains a ROM with the command interpreter as well as an 8KB RAM. It may be used to power up the system and download the BIOS to recover from situations in which the BIOS accidentally becomes corrupted or erased. The failsafe feature is used in the factory to program the BIOS in new Prometheus boards for the first time.

To enable the failsafe feature when the panel board is not used, install a jumper between pins 1 and 3 of J6 on Prometheus. To enable failsafe feature when the panel board is used, press the ZFIX button on the panel board while pressing and releasing the Reset button (the ZFIX button must be released after the Reset button is released). During the next system reset, the board will power up to the failsafe boot ROM and provide user I/O through COM1. At this point the DSC utility program ZFTERM.EXE may be used to download the BIOS to the board. See the information in the \Utilities\BIOS Recovery folder of the Prometheus files area of the DSC customer CD for instructions on using this program.

6.6 Flash Memory

Prometheus contains a 2Mbyte 16-bit wide flash memory chip for storage of BIOS and optional user files. The BIOS occupies the upper 256Kbytes, leaving the rest available for user applications.

6.7 Backup Battery

Prometheus contains an integrated RTC / CMOS RAM backup battery. The battery is located adjacent to the PC/104 bus connector J1. This battery has a capacity of 30mAH and will last approximately 2 years in power-off state. The battery is activated for the first time during initial factory configuration and test.

6.8 System Reset

Prometheus contains a chip to control system reset operation. Reset will occur under either of two conditions:

- User causes reset with a ground contact on the Reset input
- Input voltage drops below 3.0V.

The ISA Reset signal is an active high pulse with a duration of 200ms.

7. BIOS

7.1 BIOS Settings

Prometheus uses a BIOS from Phoenix Technologies modified to support the custom features of the ZF Micro ZFx86 chip and the Prometheus board. Some of these features are described here.

To enter the BIOS during system startup (POST – power on self-test), press F2.

Serial Ports

-The address and interrupt settings for serial ports COM1 – COM4 may be modified. COM1 and COM2 address and interrupt settings are done in the BIOS, Advanced menu, I/O Device Configuration. See page 27 for details.

-The addresses of COM3 and COM4 are configurable in the BIOS. Select Advanced menu, Advanced Chipset Control, ISA I/O Chip Select Setup. See page 27 for details.

Parallel Port

-The parallel port settings may be modified on the same screen as serial ports COM1 and COM2 (I/O Device Configuration).

Data Acquisition

-The on-board data acquisition circuit is modified on the same screen as serial ports COM3 and COM4 (ISA I/O Chip Select Setup).

Floppy / IDE Settings

-On the Advanced screen, I/O Device Configuration, the following settings should be retained:

Floppy disk controller	Enabled
Base I/O address	Primary
Local Bus IDE adapter	Primary

Miscellaneous

-On the Advanced screen, the following settings should be retained:

USB Host Controller	Enabled
USB BIOS Legacy Support	Disabled (Legacy support is not currently provided)
Installed O/S	Other
Large Disk Access Mode	DOS
Remote Management Baud Rate	Ignore; feature not supported on Prometheus

-On the PCI Configuration page (from the Advanced screen), the following setting should be retained:

ISA Graphics Device Installed	No
PCI IRQ Level 1-4	Autoselect for all
PCI/PNP ISA UMB Region Exclusion	Available for all

-The features on the Power screen are not supported on Prometheus.

7.2 BIOS Download / Recovery

Because the BIOS is stored in reprogrammable Flash memory, it is possible that the BIOS could be accidentally erased when trying to write other files into the Flash. To recover from this situation the CPU chip on Prometheus contains a special failsafe Boot-Up ROM (BUR) that can be activated on power-up. A Diamond Systems software utility is provided to enable system recovery by downloading the BIOS to the flash memory through serial port COM1 when the CPU is booted up to the BUR.

The recovery procedure requires another PC running Windows 95, or Windows 98. This host machine is connected to the Prometheus CPU using a null modem serial cable connected to COM1 on each computer. Three files are required on the host PC: Zftrm.exe, Loadbios.com, and the file containing the BIOS, Prm1.rom. These files should be in the same directory.

PC Serial Port End (DB-9)	Prometheus COM1 end	Corresponding pin on J6
2 (RX)	3 (TX)	2 (TX)
3 (TX)	2 (RX)	1 (RX)
5 (Ground)	5 (Ground)	3 (Ground)

Null modem cable required pinout

To boot up the Prometheus CPU to BUR, set the jumper on J6 on Prometheus to the BUR position. If using the Panel I/O board, press the Link switch while powering up or resetting the computer. The link switch must be held down slightly longer than the reset switch is released in order to power up to the BUR. When the Prometheus CPU boots up you will see the BUR display in the terminal program. The required communication parameters are 9600, n, 8, 1.

Now run the accompanying batch file recover.bat to begin the process. This batch file executes the following command:

```
zftrm.exe loadbios.com prm1.rom
```

Each flash manufacturer utilizes a different programming protocol. Zfterm.exe knows about AMD and Atmel parts, which are used on Prometheus boards. If the software cannot recognize the flash device as an AMD or Atmel part then the CPU might have a hardware problem, or else the program is an old version and needs to be upgraded. If this is the case, the software will exit with a message indicating that the device is not supported. Contact Diamond Systems technical support for further assistance.

After the software recognizes the device, it first completely erases the flash chip. This might take up to 90 seconds. After the chip is erased the software reports “Flash Erased” and then starts downloading the BIOS image from the host and programming the chip. To completely download and reprogram the BIOS takes several minutes. While this happens characters are continuously scrolled across the screen of the host PC. It is recommended that no other applications or tasks be running on the host PC during this time.

When the device is completely reprogrammed with the BIOS, the host will report the completion and the program will terminate. The Prometheus CPU is now ready to reboot in normal mode. Remove the null modem cable, and return the jumper on J6 to its default position.

7.3 Disk-On-Board™ Flash File Storage

Prometheus supports the use of its on-board flash memory as a disk drive. About 1.45Mbytes of the total 2MB capacity is available for this function. This valuable feature lets you run a DOS operating system right from the flash without having to use any external storage media in your finished application. You save the cost of external disk drives or flashdisk modules and associated cables and assembly time. Simply format the unused portion of the on-board flash to work as a disk drive, connect a floppy or hard disk to transfer your files, then disconnect them, and the system is ready to run. Complete instructions are included here.

To use the Disk-On-Board feature, you must have BIOS version 1.07M or later installed on your Prometheus. When you power up the board, the screen will indicate the BIOS version number. If you have an earlier version, you can download the latest BIOS from the Diamond Systems website along with an update utility program. The instructions for updating the BIOS are included with the BIOS package on our website and are also included in this manual. All Prometheus boards shipped on or after Septeember 23, 2002 include the Disk-On-Board feature.

Initial Setup

- Install BIOS version 1.07M or later if not already installed. Earlier versions of the Prometheus BIOS do not support this feature. Please see the BIOS recovery section of the users manual or the instructions included with the BIOS upgrade package on our website.
- Boot the system and enter the BIOS setup by pressing F2 early in the boot up.
- Go to Advanced->Advanced Chipset Control and enable the “Flash Virtual Drive”.
- Save and exit the BIOS by hitting F10. **WARNING: Do not skip this step.**
- The system will boot again. Reenter the BIOS after it boots by hitting the F2 key.
- Go to Advanced->Advanced Chipset Control again. Highlight “FLASH Initialize” then hit <enter>. You will see a percentage complete indicator. After completion the BIOS will return to the “Advanced” screen.

  WARNING: When you press enter, the flash memory will be initialized and erased. Any data currently in the flash (except the BIOS) will be lost!
- Hit the <ESC> key to return to the main tabbed menus.
- Go to the Boot tab.
- Highlight “Removable Devices” and hit <enter>.
- The “Onboard Flash” will be listed after “Legacy Floppy Drives”. This will make it a non-bootable B: drive. You can change it to a bootable A: drive by hitting the <+> or <-> key to move it to the top. This should only be done after it has been formatted and loaded with operating system files (see below), otherwise your system will not boot.
- Save and exit the BIOS by hitting the F10 key.

Operating System Formatting

- Attach a floppy drive to Prometheus.
- Boot to a DOS system disk in the floppy drive.
- At the A: prompt type “format b: /s” to format the Onboard Flash drive with the system files.
- To make this drive a bootable A: drive, reboot the system and re-enter the BIOS. Go back to the Boot menu to change the boot order by listing the “Onboard Flash” before the “Legacy Floppy Drive”.

Known Limitations

- RFD (onboard flash drive) is not compatible with DOS expanded memory configuration in EMM386.EXE. Use the NOEMS switch appended to the end of the EMM386 line in your config.sys to bypass EMS. Example line in config.sys:

  device=c:\DOS\EMM386.exe NOEMS
- The onboard flash chip has a limitation of 2,000,000 erase cycles, so swap drives or virtual memory functions should not be used.
- Currently we are shipping 2M byte Flash chips so Onboard Flash drives can be formatted with 1.45M bytes left over. 4 and 8M byte versions can be custom ordered. Contact sales@diamondsystems.com for more information.
- Only 16 bit OS's are supported for this Onboard Flash. MSDOS 6.22 and ROMDOS 6.22 and 7.0 have been tested. Other OS's may work as long as it has some sort of 16-bit compatibility mode.

Life Cycle Management and Calculations

The Disk-On-Board feature provides a simple form of wear leveling. Each time data is written, the next consecutive available memory space is used, and the current location is marked as garbage and made available for later use. This way the system walks through the entire available space before rewriting the current file location. This technique helps to dramatically increase the chip's lifetime, because the entire chip is used to spread out the wear caused by the repeated erase cycles.

A typical embedded application consists of reading a file, updating it, and repeating the process over and over again. The formula for calculating the number of times this may be done before the flash reaches its limit is as follows:

```
Number of file writes = (size of chip / size of file) * lifetime of chip
```

Where size of chip = 1.45MB and lifetime of chip = 2,000,000. This formula reveals the increase in lifetime provided by the wear leveling. The lifetime is increased by the ratio of the chip's total capacity to the file size.

To calculate the number of days the chip will last, simply factor in the number of updates per day:

```
Lifetime in days = number of file writes / file writes per day
```

8. SYSTEM I/O

8.1 Ethernet

Prometheus includes a 100Mbps Ethernet connection using 100BaseT wiring. The signals are provided on a 6-pin header J4 on the bottom edge of the board.

Diamond Systems' cable no. **698002** mates with this header and provides a standard RJ-45 connector in panel-mount form for connecting to standard Cat5 network cables.

1	Common
2	RX-
3	Common
4	RX+
5	TX-
6	TX+

J4 – Ethernet Connector

The Ethernet chip is the National Semiconductor DP83815 MacPhyter chip. It is connected to the ZfX86 CPU via the board's internal PCI bus. It resides at address 1000 and uses IRQ 10.

The Prometheus Software CD includes Ethernet drivers for Windows 95, Windows 98, Windows NT, and Linux. The latest drivers can also be downloaded from National Semiconductor's website at www.national.com. Search for DP83815 to reach the product folder.

A DOS utility program is also provided for testing the chip and accessing the configuration EEPROM. Each board is factory-configured for a unique MAC address using this program. To run the program, you must boot the computer to DOS. The program will not run properly in a DOS window inside of Windows. In normal operation this program should not be required.

8.2 Serial Ports

Prometheus contains 4 serial ports. Each port is capable of transmitting at speeds of up to 115.2Kbaud. Ports COM1 and COM2 are built into the ZF Micro CPU chip. They consist of standard 16550 type UARTs with 16-byte FIFOs. Ports COM3 and COM4 are derived from an Exar 16C2850 dual UART chip and include 128-byte FIFOs. Ports 3 and 4 may be operated at speeds up to 1.5Mbaud with installation of high-speed drivers as a custom option.

The serial ports use the following default system resources:

Port	Address range	IRQ
COM1	I/O 3F8 – 3FF	4
COM2	I/O 2F8 – 2FF	3
COM3	I/O 3E8 – 3EF	4
COM4	I/O 2E8 – 2EF	3

The settings of COM1 and COM2 may be changed in the system BIOS. Select the Advanced menu, then I/O Device Configuration. Serial Port A is COM1, and Serial Port B is COM2. The base address and interrupt level may be modified on this page.

The settings of COM3 and COM4 may be changed using a different procedure:

The addresses of these two ports are selected on the Advanced menu of the BIOS. Select Advanced Chipset Control, then ISA I/O Chip Select Setup. I/O Window – io_cs1 is for COM3 and I/O window – io_cs2 is for COM4. The only parameter that may be changed is the address. The other settings must remain in their default values:

Window state:	Enabled
Base Address:	(user selectable)
Read/Write control:	Read/Write
Window data width:	8-bits
Active Level:	Active Low
Window size:	08

After making any desired changes, go to the top-level Exit menu and select Exit Saving Changes.

The interrupt (IRQ) settings for COM3 and COM4 are selected with J10. COM3 may use IRQ4 or IRQ9. COM4 may use IRQ3 or IRQ15. If both serial ports share the same IRQ, they may share IRQ4 or IRQ5. See page 16 for serial port IRQ jumper settings.

8.3 Parallel Port

The parallel port (LPT1) is an IEEE-1284 compatible bidirectional port. It includes filtering for reduced EMI operation. It operates in ECP mode (set up in the BIOS). The parallel port has the following default configuration:

Port	Mode	Address range	IRQ	DMA
LPT1	ECP	I/O 378 – 37F	7	3

The parallel port settings may be modified in the BIOS. Select Advanced menu, then I/O Device Configuration. The above four settings may then be modified.

9. NOTES ON OPERATING SYSTEMS AND BOOTING PROCEDURES

9.1 Booting to DOS From a Floppy Drive

In some revisions of the ZF Micro processor chip and Phoenix BIOS on Prometheus, there is a short period of conflict between the floppy drive and the programmable chip selects during the booting from a floppy disk in certain operating systems such as Windows 98. This conflict makes it impossible to boot to DOS from a floppy disk with these chip selects enabled. The following workaround procedure may be used to enable booting to floppy drive.

1. Enter the BIOS (press F2 during startup).
2. Change the boot sequence (Boot menu) to boot from floppy drive.
3. Go to the Advanced screen, then select Advanced Chipset Control / ISA I/O Chip Select Setup. You will see four chip selects. CS0 is not used. CS1 is used for COM3, CS2 is used for COM4, and CS3 is used for the data acquisition circuit.
4. Scroll down to CS1, CS2, and CS3. Change the setting “Window State” for each of these chip selects to [Disable]. This temporarily disables COM3, COM4 and the Data Acquisition System.
5. Save the new settings and exit the BIOS.
6. The system will now boot to DOS from the floppy drive.

9.2 Installing an OS From a Floppy Drive onto a Flashdisk Module

1. Make sure the flashdisk module jumper is configured for Master.
2. Install the flashdisk module onto the CPU. See installation instructions on page 63.
3. Follow the instructions above for booting to a floppy drive.
4. If necessary, run FDISK and perform the following steps:
    a. Remove all partitions on the flashdisk module.
    b. Create a primary DOS partition on the flashdisk module.
    c. Make the DOS partition the active partition.
    d. Save your changes and exit.
5. Boot the system again from the floppy disk.
6. Format the flashdisk module using FORMAT C: /S.
7. Copy the operating system files and any other needed files to the flashdisk module.
8. Reboot your system and enter the BIOS during startup.
9. Go to the Advanced screen, then select Advanced Chipset Control / ISA I/O Chip Select Setup. Reenable chip selects CS1 through CS3.
10. Go to the Boot screen and change the boot sequence to boot from hard disk.
11. Save the new settings and exit the BIOS.
12. Power down the system and disconnect the floppy drive.
13. The system is now able to boot from the flashdisk module.

9.3 Installing an OS from a Hard Disk onto a Flashdisk Module

To install an operating system such as DOS or VxWorks from a hard drive onto a flashdisk module, follow the procedure below. The process requires a floppy drive with a bootable DOS diskette, a hard disk with the operating system, the flashdisk module, the IDE extender board, and associated cables.

You must boot to the floppy drive rather than the hard drive, because if you boot to the hard drive, it must be the master drive, making the flashdisk the slave drive. DOS will not allow you to create a bootable partition on a slave drive, and you must create the bootable partition on the flashdisk, so the flashdisk must be configured for the master.

As an alternative to this procedure you may also install the operating system from the floppy drive as outlined on page 28.

2. First install the operating system onto a hard disk.
3. Configure the hard disk jumper for Slave and the flashdisk module jumper for Master.
4. Install the flashdisk module onto the IDE extender board, model ACC-IDEEXT.
5. Connect the extender board to the CPU's IDE connector using the 44-pin ribbon cable.
6. Connect the hard disk to the appropriate connector on the extender board. If using a 44-pin cable (such as DSC no. 698004), no power cable is required. If using a 40-pin cable (such as DSC no. C-40-18), a separate power cable is required. The power may be provided either from one of the two 4-pin headers on the extender board or from the Auxiliary Power Out connector J12 on the Prometheus CPU. Use DSC cable no. 698006 for the power connection.
7. Attach a floppy drive to J7 on the Prometheus using DSC cable no. 698008 and provide power to it. DSC cable 698006 can be used for the floppy drive power.
8. Install a bootable floppy disk into the floppy drive.
9. Power up the system.
10. Make sure the BIOS is configured to boot from floppy. Press F2 to enter BIOS when booting, and go to the Boot screen to make this configuration.
11. Make sure the I/O chip selects are disabled as described in section 9.1.
12. Once the system is booted, switch to drive D: (the hard disk with the OS on it) and change to the DOS directory.
13. If necessary, run FDISK and perform the following steps:
    a. Remove all partitions on the flashdisk module.
    b. Create a primary DOS partition on the flashdisk module.
    c. Make the DOS partition the active partition.
    d. Save your changes and exit.
14. Boot the system again from the floppy disk.
15. Switch to the hard disk (D:) and change to the DOS directory.
16. Format the flashdisk module using FORMAT C: /S.
17. Copy the operating system files and any other needed files onto the flashdisk module.
18. Power down the system.
19. Remove the hard disk and extender board and install the flashdisk module directly onto the IDE connector J8 on the Prometheus CPU.
20. Power up the system again.
21. Enter the BIOS (F2) and change the bootup sequence to boot from hard disk C: (which now means the flashdisk module).

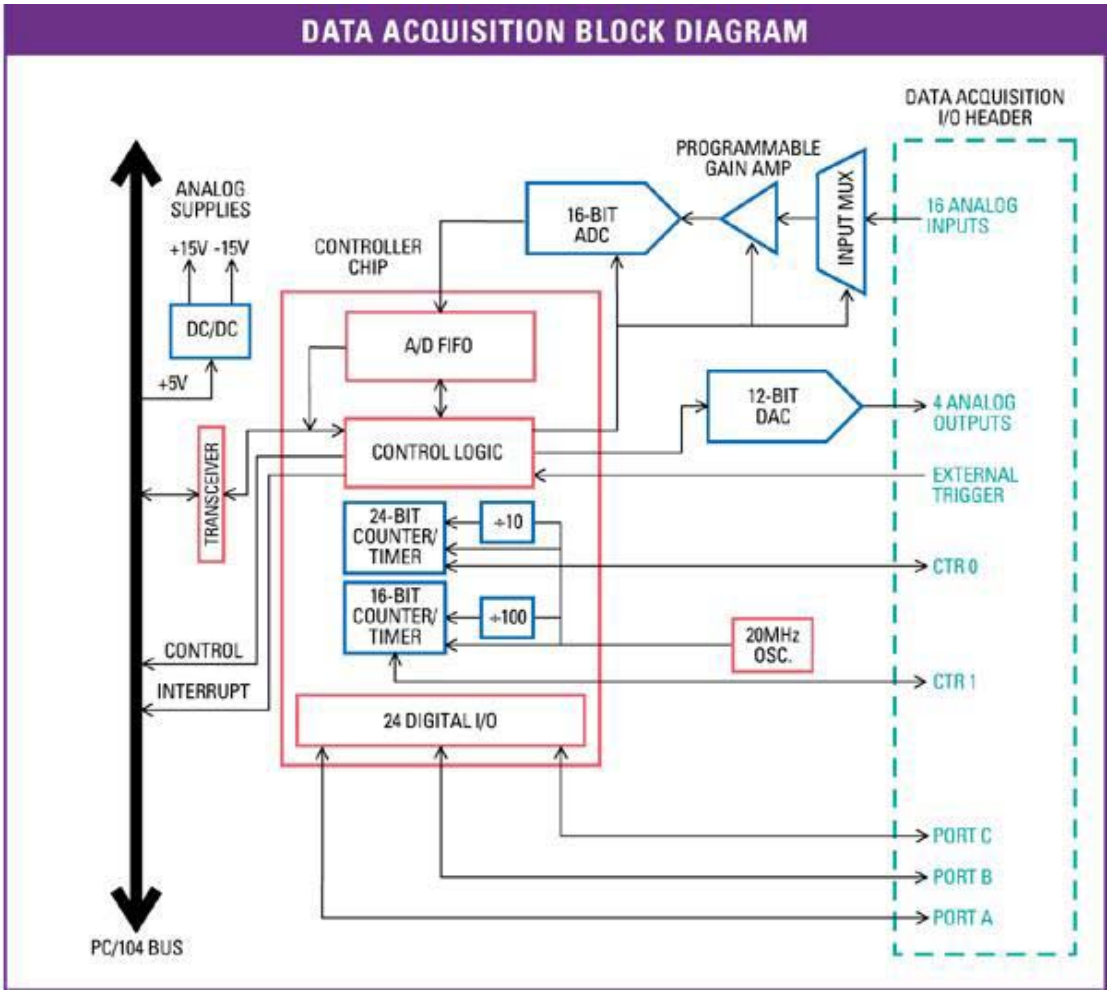
10. DATA ACQUISITION CIRCUIT

Model PR-Z32-EA contains a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. This subsystem is equivalent to a complete add-on data acquisition module.

The A/D section includes a 16-bit A/D converter, 16 input channels, and a 48-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 100KHz. The D/A section includes 4 12-bit D/A channels. The digital I/O section includes 24 lines with programmable direction. The counter/timer section includes a 24-bit counter/timer to control A/D sampling rates and a 16-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store a user-selected number of samples, and the interrupt occurs when the FIFO reaches this threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate. In DOS or similar low-overhead operating systems the circuit can operate at sampling rates of up to 100KHz, with an interrupt rate of 6.6-10KHz. (An interrupt rate of above approximately 2KHz is difficult to sustain in Windows without the possibility of missing samples.)

The A/D circuit uses the default settings of I/O address range 280h – 28Fh (base address 280) and IRQ 5. These settings can be changed if needed. The I/O address range is changed in the BIOS, and the interrupt level is changed with jumper block J10.



11. DATA ACQUISITION CIRCUITRY I/O MAP

11.1 Base Address

The data acquisition circuitry on Prometheus occupies a block of 16 bytes in I/O memory space. The default address range for this block is 280h – 28Fh (base address 280). This address should work for most applications, but it can be changed in the BIOS if necessary. Go to the Advanced screen and select Advanced Chipset Control, then ISA I/O Chip Select Setup. Scroll down to I/O Window io_cs3, which is used for the data acquisition circuit. Do not change any setting other than the base address or the circuit will not function properly. Make sure the selected address range does not conflict with any other circuit on the CPU or any add-on module. Here are the proper settings:

Window state:	Enabled
Base Address:	(user selectable, default 280h)
Read/Write control:	Read/Write
Window data width:	8-bits
Active Level:	Active Low
Window size:	16

A functional list of registers is provided below, and detailed bit definitions are provided on the next page and in the following chapter.

Base +	Write Function	Read Function
0	Command register	A/D LSB
1	Not used	A/D MSB
2	A/D channel register	A/D channel register
3	A/D gain and scan settings	A/D gain and status readback
4	Interrupt / DMA / counter control	Interrupt / DMA / counter control readback
5	FIFO threshold	FIFO threshold readback
6	D/A LSB	FIFO current depth
7	D/A MSB + channel no.	Interrupt and A/D channel readback
8	Digital I/O port A output	Digital I/O port A
9	Digital I/O port B output	Digital I/O port B
10	Digital I/O port C output	Digital I/O port C
11	Digital I/O direction control	Digital I/O direction control readback
12	Counter/timer D7-0	Counter/timer D7-0
13	Counter/timer D15-8	Counter/timer D15-8
14	Counter/timer D23-16	Counter/timer D23-16
15	Counter/timer control register	FPGA revision code

11.2 Data Acquisition Circuit Register Map

WRITE (Blank bits are unused and have no effect)

Address	7	6	5	4	3	2	1	0
0	STRTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA
1								
2	H3	H2	H1	H0	L3	L2	L1	L0
3						SCANEN	G1	G0
4	CKSEL1	CKFRQ1	CKFRQ0	ADCLK	DMAEN	TINTE	DINTE	AINTE
5			FT5	FT4	FT3	FT2	FT1	FT0
6	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
7	DACH1	DACH0			DA11	DA10	DA9	DA8
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR			DIRA	DIRCH		DIRB	DIRCL
12	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
13	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
14	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
15	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

READ (Blank bits are unused and read back as 0)

Address	7	6	5	4	3	2	1	0
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	H3	H2	H1	H0	L3	L2	L1	L0
3	STS	SD	WAIT	DACBSY	OVF	SCANEN	G1	G0
4	CKSEL1	CKFRQ1	CKFRQ0	ADCLK	DMAEN	TINTE	DINTE	AINTE
5			FT5	FT4	FT3	FT2	FT1	FT0
6			FD5	FD4	FD3	FD2	FD1	FD0
7	DMAINT	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR			DIRA	DIRCH		DIRB	DIRCL
12	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
13	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
14	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
15	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

11.3 Register Bit Definitions

In these register definitions, a bit marked 'X' is an unused bit.

All unused bits in readable registers read back as 0.

Base + 0 Write Command Register

Bit No.	7	6	5	4	3	2	1	0
Name	STRTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA

This register is used to perform various functions. The register bits are not data bits but instead command triggers. Each function is initiated by writing a 1 to a particular bit. **Writing a 1 to any bit in this register does not affect any other bit in this register.** For example, to reset the FIFO, write the value 0x10 (16) to this register to write a 1 to bit 4. No other function of the register will be performed. Multiple actions can be carried out simultaneously by writing a 1 to multiple bits simultaneously.

STRTAD Start an A/D conversion (trigger the A/D) when in software-trigger mode (AINTE = 0). Once the program writes to this bit, the A/D conversion will start and the STS bit (base + 3 bit 7) will go high. The program should then monitor STS and wait for it to go low (check if value in base + 3 is less than 128 or 0x80). When it goes low the A/D data at Base + 0 and Base + 1 may be read.

When AINTE = 1 (base + 4 bit 0), the A/D cannot be triggered by writing to this bit. Instead the A/D will be triggered by a signal selected by ADCLK in base + 4 bit 5.

RSTBRD Reset the entire board excluding the D/A. Writing a 1 to this bit causes all registers on the board to be reset to 0. The effect on the digital I/O is that all ports are reset to input mode, and the logic state of their pins will be determined by the pull-up/pull-down configuration setting selected by the user. All A/D, counter/timer, interrupt, and DMA functions will cease. However the D/A values will remain constant.

RSTDA Reset the 4 analog outputs. The analog outputs will be reset to either mid-scale or zero-scale, depending on the jumper configuration selected by the user. A separate reset is provided for the D/A so that the user may reset the board if needed without affecting the circuitry connected to the analog outputs.

RSTFIFO Reset the FIFO depth to 0. This clears the FIFO so that further A/D conversions will be stored in the FIFO starting at address 0.

CLRDMA Writing a 1 to this bit causes the DMA interrupt request flip flop to be reset.

CLRT Writing a 1 to this bit causes the timer interrupt request flip flop to be reset.

CLRD Writing a 1 to this bit causes the digital I/O interrupt request flip flop to be reset.

CLRA Writing a 1 to this bit causes the analog interrupt request flip flop to be reset.

The user's interrupt routine must write to the appropriate bit prior to exiting in order to enable future interrupts. Otherwise the interrupt line will stay high indefinitely and no additional interrupt requests will be generated by the board.

Base + 0 Read A/D LSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD7 - 0 A/D data bits 7 - 0; AD0 is the LSB; A/D data is an unsigned 16-bit value.

The A/D value is derived by reading two bytes from Base + 0 and Base + 1 and applying the following formula:

A/D value = (Base + 0 value) + (Base + 1 value) * 256

The value is interpreted as a twos complement 16-bit number ranging from –32768 to +32767. This raw A/D value must then be converted to the corresponding input voltage and/or the engineering units represented by that voltage by applying additional application-specific formulas. Both conversions (conversion to volts and then conversion to engineering units) may be combined into a single formula for efficiency.

Base + 1 Write Not Used

Base + 1 Read A/D MSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD15 - 8 A/D data bits 15 – 8; AD15 is the MSB; A/D data is an unsigned 16-bit value.

See Base + 0 Read on the previous page for information on A/D values and formulas.

Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	H3	H2	H1	H0	L3	L2	L1	L0

H3 – H0 High channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

L3 - L0 Low channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

The high channel must be greater than or equal to the low channel.

When this register is written, the current A/D channel is set to the low channel, so that the next time an A/D conversion is triggered the low channel will be sampled.

When this register is written to, the WAIT bit (Read Base + 3 bit 5) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time an A/D conversion should not be performed because the data will be inaccurate.

After writing a new gain setting (Base + 3), the WAIT bit is also set, and the program must monitor it prior to starting an A/D conversion.

The channel and gain registers can be written to in succession without waiting for the intervening WAIT signal. Only one WAIT period must be observed between the last triggering condition (write to Base + 2 or Base + 3) and the start of an A/D conversion.

The A/D circuit is designed to automatically increment the A/D channel each time a conversion is generated. This enables the user to avoid having to write the A/D channel each time. The A/D channel will rotate through the values between LOW and HIGH. For example, if LOW = 0 and HIGH = 3, the A/D channels will progress through the following sequence: 0, 1, 2, 3, 0, 1, 2, 3, 0, 1, ….

Reading from this register returns the value previously written to it.

Base + 3 Write Analog Input Gain

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	SCANEN	G1	G0

SCANEN Scan mode enable:

1 Each A/D trigger will cause the board to generate an A/D conversion on each channel in the range LOW – HIGH (the range is set with the channel register in Base + 2).

The STS bit (read Base + 3 bit 7) stays high during the entire scan.

0 Each A/D trigger will cause the board to generate a single A/D conversion on the current channel. The internal channel pointer will increment to the next channel in the range LOW – HIGH or reset to LOW if the current channel is HIGH.

The STS bit stays high during the A/D conversion.

G1-G0 Analog input gain. The gain is the ratio of the voltage seen by the A/D converter and the voltage applied to the input pin. The gain setting is the same for all input channels.

When this register is written to, the WAIT bit (Read Base + 3 bit 6) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time an A/D conversion should not be performed because the data will be inaccurate. After writing a new gain setting, the program should monitor the WAIT bit prior to starting an A/D conversion.

After writing a new channel selection (Base + 2), the WAIT bit is also set, and the program must monitor it prior to starting an A/D conversion.

The channel and gain registers can be written to in succession without waiting for the intervening WAIT signal. Only one WAIT period must be observed between the last triggering condition (write to Base + 2 or Base + 3) and the start of an A/D conversion.

The following table lists the possible analog input ranges:

G1	G0	Gain	Unipolar Range	Bipolar Range
0	0	1	Invalid	±10V
0	1	2	0-10V	±5V
1	0	4	0-5V	±2.5V
1	1	8	0-2.5V	±1.25V

Base + 3 Read Analog Input Status

Bit No.	7	6	5	4	3	2	1	0
Name	STS	SD	WAIT	DACBSY	OVF	SCANEN	G1	G0

STS A/D status. 1 = A/D conversion or scan in progress, 0 = A/D is idle.

If SCANEN = 0 (single conversion mode), STS goes high when an A/D conversion is started and stays high until the conversion is finished. If SCANEN = 1 (scan mode enabled), STS stays high during the entire scan. After starting a conversion in software, the program must monitor STS and wait for it to become 0 prior to reading A/D values from Base + 0 and Base + 1.

SD Single-ended / Differential mode indicator. 1 = SE, 0 = DI.

WAIT A/D input circuit status. 1 = A/D circuit is settling on a new value, 0 = ok to start conversion.

WAIT goes high after the channel register (Base + 2) or the gain register (Base + 3) is changed. It stays high for 9 microseconds. The program should monitor this bit after writing to either register and wait for it to become 0 prior to starting an A/D conversion.

DACBSY Indicates the DAC is busy updating (approx. 30 µS). 1 = Busy, 0 = Idle. Do not attempt to write to the DAC (registers 6 and 7) while DACBSY = 1.

OVF FIFO Overflow bit. This bit indicates that the FIFO has overflowed, meaning that the A/D circuit has attempted to write data to it when it is full. This condition occurs when data is written into the FIFO faster than it is read out.

When overflow occurs, the FIFO will not accept any more data until it is reset. The OVF condition is sticky, meaning that it remains true until the FIFO is reset, so the application program will be able to determine if overflow occurs. If overflow occurs, then you must either reduce the sample rate or increase the efficiency of your interrupt routine and/or operating system.

SCANEN Scan mode readback (see Base + 3 Write above).

G1-G0 A/D gain setting readback (see Base + 3 Write above).

Base + 4 Read/Write Interrupt / DMA / Counter Control

Bit No.	7	6	5	4	3	2	1	0
Name	CKSEL1	CKFRQ1	CKFRQ0	ADCLK	DMAEN	TINTE	DINTE	AINTE

CKSEL1 Clock source selection for counter/timer 1:

0 = internal oscillator, frequency selected by CLKFRQ1

1 = external clock input CLK1 (DIO C pins must be set for ctr/timer signals)

CKFRQ1 Input frequency selection for counter/timer 1 when CKSEL1 = 1:

0 = 10MHz, 1 = 100KHz

CKFRQ0 Input frequency selection for counter/timer 0.

0 = 10MHz, 1 = 1MHz

ADCLK A/D trigger select when AINTE = 1:

0 = internal clock output from counter/timer 0

1 = external clock input EXTTRIG

DMAEN Enable DMA operation. 1 = enable, 0 = disable.

TINTE Enable timer interrupts. 1 = enable, 0 = disable.

DINTE Enable digital I/O interrupts. 1 = enable, 0 = disable.

AINTE Enable analog input interrupts. 1 = enable, 0 = disable.

NOTE: When AINTE = 1, the A/D cannot be triggered by writing to Base + 0.

Analog output interrupts are not supported on this board.

Multiple interrupt operations may be performed simultaneously. All interrupts will be on the same interrupt level. The user's interrupt routine must monitor the status bits to know which circuit has requested service. After processing the data but before exiting, the interrupt routine must then clear the appropriate interrupt request bit using the register at Base + 0.

Base + 5 Read/Write FIFO Threshold

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	FT5	FT4	FT3	FT2	FT1	FT0

FT5–0 FIFO threshold. When the number of A/D samples in the FIFO reaches this number, the board will generate an interrupt and set AINT high (Base + 7 bit 4). The interrupt routine is responsible for reading the correct number of samples out of the FIFO.

The valid range is 1-48. If the value written is greater than 48, then 48 will be used. If the value written is 0, then 1 will be used. The interrupt rate is equal to the total sample rate divided by the FIFO threshold. Generally, for higher sampling rates a higher threshold should be used to reduce the interrupt rate. However remember that the higher the FIFO threshold, the smaller the amount of FIFO space remaining to store data while waiting for the interrupt routine to respond. If you get a FIFO overflow condition, you must lower the FIFO threshold and/or lower the A/D sampling rate.

Base + 6 Write DAC LSB

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7–0 D/A data bits 7 - 0; DA0 is the LSB. D/A data is an unsigned 12-bit value. This register must be written to before Base + 7, since writing to Base + 7 updates the DAC immediately.

Base + 6 Read A/D Channel and FIFO Status

Bit No.	7	6	5	4	3	2	1	0
Name	0	0	FD5	FD4	FD3	FD2	FD1	FD0

FD5–0 Current FIFO depth. This value indicates the number of A/D values currently stored in the FIFO.

Base + 7 Write DAC MSB + Channel No.

Bit No.	7	6	5	4	3	2	1	0
Name	DACH1	DACH0	X	X	DA11	DA10	DA9	DA8

DACH1–0 D/A channel. The value written to Base + 6 and Base + 7 are written to the selected channel, and that channel is updated immediately. The update takes approximately 20 microseconds due to the DAC serial interface.

DA11–8 D/A bits 11 - 8; DA11 is the MSB. D/A data is an unsigned 12-bit value.

Base + 7 Read Analog Operation Status

Bit No.	7	6	5	4	3	2	1	0
Name	DMAINT	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0

DMAINT DMA interrupt status. 1 = interrupt pending, 0 = interrupt not pending.

TINT Timer interrupt status, same values as above.

DINT Digital I/O interrupt status, same values as above.

AINT Analog input interrupt status, same values as above.

ADCH3-0 Current A/D channel. This is the channel that will be sampled on the **next** conversion.

When any of bits 7–4 are 1, the corresponding circuit is requesting service. The interrupt routine must poll these bits to determine which circuit needs service and then act accordingly.

Base + 8 Read / Write Digital I/O Port A

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

Base + 9 Read / Write Digital I/O Port B

Bit No.	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0

Base + 10 Read / Write Digital I/O Port C

Bit No.	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0

These 3 registers are used for digital I/O. The direction of each register is controlled by bits in the register below.

Base + 11 Read / Write Digital I/O Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOCTR	X	X	DIRA	DIRCH	X	DIRB	DIRCL

The bit assignments of this register are designed to be compatible with the 82C55 chip's control register.

DIOCTR Selects counter I/O signals or digital I/O lines C4-C7 on pins 21-24 of J14:

Pin No.	DIOCTR = 1	DIOCTR = 0	Pin direction for DIOCTR = 0
21	C4	Gate 0	Input
22	C5	Gate 1	Input
23	C6	Clk 1	Input
24	C7	Out 0	Output

NOTE: If DIOCTR = 0, then the pin direction is as shown above. If DIOCTR = 1 then the pin direction is controlled by DIRCH.

This bit resets to 1.

DIRA Port A direction. 0 = output, 1 = input

DIRB Port B direction: 0 = output, 1 = input

DIRCH Port C bits 7-4 direction: 0 = output, 1 = input

DIRCL Port C bits 3-0 direction: 0 = output, 1 = input

Base + 12 Read/Write Counter/Timer D7 - 0

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

This register is used for both Counter 0 and Counter 1. It is the LSB for both counters.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15, the selected counter's LSB register will be loaded with this value.

When reading from this register, the LSB value of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Base + 13 Read/Write Counter/Timer D15 - 8

Bit No.	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8

This register is used for both Counter 0 and Counter 1. It is the MSB for counter 1 and the middle byte for counter 0.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15, the selected counter's associated register will be loaded with this value. For counter 0, it is the middle byte. For counter 1, it is the MSB.

When reading from this register, the associated byte of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Base + 14 Read/Write Counter/Timer D23 - 16

Bit No.	7	6	5	4	3	2	1	0
Name	D23	D22	D21	D20	D19	D18	D17	D16

This register is used for Counter 0 only. Counter 0 is 24 bits wide, while Counter 1 is only 16 bits wide.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15 for Counter 0, the counter's MSB register will be loaded with this value. When issuing a Load command for counter 1, this register is ignored.

When reading from this register, the MSB value of the most recent Latch command for counter 0 will be returned. The value returned is NOT the value written to this register.

Base + 15 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

This register is used to control the counter/timers. A counter is selected with bit 7, and then a 1 is written to any ONE of bits 6 – 0 to select the desired operation for that counter. The other bits and associated functions are not affected. Thus only one operation can be performed at a time.

CTRNO Counter no., 0 or 1

LATCH Latch the selected counter so that its value may be read. The counter must be latched before it is read. Reading from registers 12-14 returns the most recently latched value. If you are reading Counter 1 data, read only Base + 12 and Base + 13. Any data in Base + 14 will be from the previous Counter 0 access.

GTDIS Disable external gating for the selected counter.

GTEN Enable external gating for the selected counter. If enabled, the associated gate signal GATE0 or GATE1 controls counting on the counter. If the GATEn signal is high, counting is enabled. If the GATEn signal is low, counting is disabled.

CTDIS Disable counting on the selected counter. The counter will ignore input pulses.

CTEN Enable counting on the selected counter. The counter will decrement on each input pulse.

LOAD Load the selected counter with the data written to Base + 12 through Base + 14 or Base + 12 and Base + 13 (depending on which counter is being loaded).

CLR Clear the current counter (set its value to 0).

To load a counter: First write the load value to Base + 12 and Base + 13 (for Counter 1) or Base + 12 through Base + 14 (for Counter 0). Then write a Load command to Base + 15. For example, to load Counter 0 with the hex value 123456:

- Write 0x12 to Base + 14 (these three bytes can be written to in any order)
- Write 0x34 to Base + 13
- Write 0x56 to Base + 12
- Write 0x02 to Base + 15 to load counter 0

To enable counting: Write 0x04 (ctr 0) or 0x84 (ctr 1) to Base + 15.

To stop counting: Write 0x08 (ctr 0) or 0x88 (ctr 1) to Base + 15.

To read a counter: First latch it, then read the value:

- Write 0x40 to Base + 15 to latch counter 0 or 0xC0 to latch counter 1
- Read LSB from Base +12
- Read Middle Byte from Base + 13
- Read MSB from Base + 14
- Assemble 3 bytes into the current counter value

More complete counter programming operations are provided in chapter 20 on page 59.

Base + 15 Read FPGA Revision Code

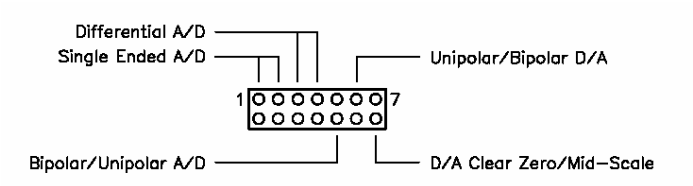
Bit No.	7	6	5	4	3	2	1	0
Name	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

This register is used to control the counter/timers. A counter is selected with bit 7, and then a 1 is written to any ONE of bits 6 – 0 to select the desired operation for that counter. The other bits and associated functions are not affected. Thus only one operation can be performed at a time.

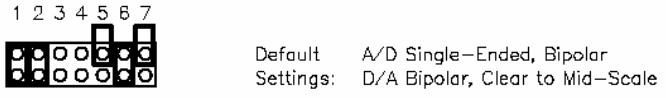
REV7-0 Revision code, read as a 2-digit hex value, i.e. 0x20 = revision 2.0

12. DATA ACQUISITION CIRCUIT CONFIGURATION

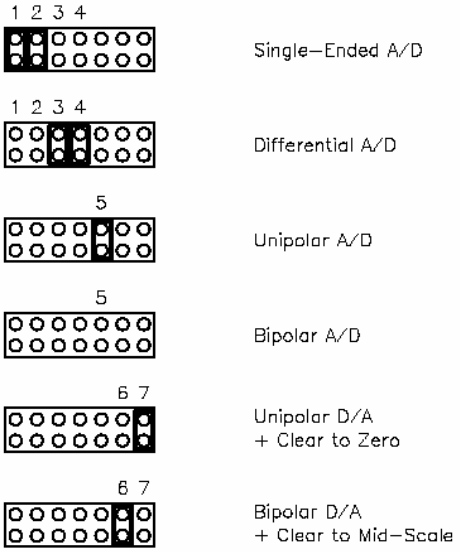
Jumper block **J13** is used to configure the A/D and D/A circuits on PR-Z32-EA. It is located on the left side of the board next to the data acquisition I/O pin header and is oriented vertically. The functions are shown below and are described in detail on the following page.



The default settings are as shown:



The various configurations are illustrated and described below. For correct configuration, pick one option from the first two configurations (single-ended or differential A/D), one option from the second two configurations (unipolar or bipolar A/D), and one option from the third two configurations (unipolar or bipolar D/A).



Single-ended / Differential Inputs

Prometheus can accept both single-ended and differential inputs. A **single-ended** input uses 2 wires, input and ground. The measured input voltage is the difference between these two wires. A **differential** input uses 3 wires: input +, input -, and ground. The measured input voltage is the difference between the + and - inputs.

Differential inputs are frequently used when the grounds of the input device and the measurement device (Prometheus) are at different voltages, or when a low-level signal is being measured that has its own ground wire. A differential input also has higher noise immunity than a single-ended input, since most noise affects both + and – input wires equally, so the noise will be canceled out in the measurement. The disadvantage of differential inputs is that only half as many are available, since two input pins are required to produce a single differential input. Prometheus can be configured for either 16 single-ended inputs or 8 differential inputs.

If you have a combination of single-ended and differential input signals, select differential mode. Then to measure the single-ended signals, connect the signal to the + input and connect analog ground to the - input.

WARNING: The maximum range of voltages that can be applied to an analog input on Prometheus without damage is ±35V. If you connect the analog inputs on Prometheus to a circuit whose ground potential plus maximum signal voltage exceeds ±35V, the analog input circuit may be damaged. Check the ground difference between the input source and Prometheus before connecting analog input signals.

Unipolar / Bipolar Inputs

The analog inputs can be configured for can be configured for unipolar (positive input voltages only) or bipolar (both negative and positive input voltages). For **unipolar** inputs, install a jumper as shown. For **bipolar** inputs, leave the jumper out.

Analog Output Configuration

The 4 analog outputs can also be configured for unipolar (positive voltages only) or bipolar (both negative and positive output voltages). In unipolar mode, the outputs range between 0-10V. In bipolar mode, the outputs range between ±10V.

When the board powers up or is reset, the analog outputs are also reset. The D/A reset method is selected with a jumper on J13. If the jumper is in, the outputs will reset to the bottom of their range (called zero-scale). If the jumper is out, the outputs will reset to the middle of their range (mid-scale). Normally the D/A is configured to power up to 0V, so that when the power is turned on the device connected to the analog output doesn't see a step change in voltage. Therefore, for unipolar mode normally the outputs should be configured for zero-scale reset, and for bipolar mode the outputs should be configured for mid-scale reset, since 0V is halfway between -10V and +10V for the ±10V range.

13. ANALOG INPUT RANGES AND RESOLUTION

13.1 Overview

Prometheus uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However the A/D converter uses twos complement notation, so the A/D value is interpreted as a signed integer ranging from –32768 to +32767.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and so this change is referred to as 1 LSB, or 1 Least Significant Bit.

The analog inputs on Prometheus have three configuration options:

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended / differential and unipolar / bipolar configuration is done with a jumper on jumper block J13 (see page 45), and the input range selection is done in software.

13.2 Input Range Selection

Prometheus can be configured to measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. This configuration is done with a jumper and applies to all inputs. In addition you can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, so it can be changed on a channel-by-channel basis. In general you should select the highest gain (smallest input range) that will allow the A/D converter to read the full range of voltages over which your input signals will vary. However, if you pick too high a gain, then the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

13.3 Input Range Table

The table below indicates the analog input range for each possible configuration. The polarity is set with a jumper on jumper block J13, and the gain is set with the G1 and G0 bits in the register at Base + 3. The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

Polarity	G1	G0	Input Range	Resolution (1 LSB)
Bipolar	0	0	±10V	305μV
Bipolar	0	1	±5V	153μV
Bipolar	1	0	±2.5V	76μV
Bipolar	1	1	±1.25V	38μV
Unipolar	0	0	Invalid	
Unipolar	0	1	0 – 10V	153μV
Unipolar	1	0	0 – 5V	76μV
Unipolar	1	1	0 – 2.5V	38μV

14. PERFORMING AN A/D CONVERSION

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (not with the driver software).

There are seven steps involved in performing an A/D conversion:

1. **Select the input channel**
2. **Select the input range**
3. **Wait for analog input circuit to settle**
4. **Initiate an A/D conversion**
5. **Wait for the conversion to finish**
6. **Read the data from the board**
7. **Convert the numerical data to a meaningful value**

14.1 Select the input channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at base + 2 (see page 35). The low 4 bits select the low channel, and the high 4 bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example:

To set the board to channel 4 only, write 0x44 to Base + 2.

To set the board to read channels 0 through 15, write 0xF0 to Base + 2.

⇒ **Note:** When you perform an A/D conversion, the current channel is automatically incremented to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write Hex 20 to base + 2. The first conversion is on channel 0, the second will be on channel 1, and the third will be on channel 2. Then the channel counter wraps around to the beginning again, so the fourth conversion will be on channel 0 again and so on.

If you are sampling the same channel repeatedly, then you set both high and low to the same value as in the first example above. Then on subsequent conversions you do not need to set the channel again.

14.2 Select the input range

Select the input range from among the available ranges shown on page 47. If the range is the same as for the previous A/D conversion then it does not need to be set again. Write this value to the input range register at Base + 3 (see page 36).

For example:

For ±5V range (gain of 2), write 0x01 to Base + 3.

14.3 Wait for analog input circuit to settle

After writing to either the channel register (Base + 2) or the input range register (Base + 3), you must allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10μS timer to assist with the wait period. Monitor the WAIT bit at Base + 3 bit 5. When it is 1 the circuit is actively settling on the input signal. When it is 0 the board is ready to perform A/D conversions.

14.4 Perform an A/D conversion on the current channel

After the above steps are completed, start the A/D conversion by writing to Base + 0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base,0x80);
```

14.5 Wait for the conversion to finish

The A/D converter chip takes up to 5 microseconds to complete one A/D conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, you will beat the A/D converter and get invalid data. Therefore the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back as bit 7 in the status register at Base + 3. When the A/D converter is busy (performing an A/D conversion), this bit is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit is 0 and the program may read the data. Here are examples:

```
while (inp(base+3) & 0x80);    // Wait for conversion to finish before proceeding
```

This method could hang your program if there is a hardware fault and the bit is stuck at 1. Better is to use a loop with a timeout:

```
int checkstatus()       // returns 0 if ok, -1 if error
    int i;
    for (i = 0; i < 10000; i++)
    {
        if !(inp(base+3) & 0x80) then return(0);          // conversion completed
    }
    return(-1);         // conversion didn't complete
```

14.6 Read the data from the board

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and is read back in two 8-bit bytes. The LSB must be read from the board before the MSB, because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, since each time a byte is read from the FIFO, the FIFO's internal pointer advances, and that byte is no longer available. Note that reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

The final data is interpreted as a 16-bit signed integer ranging from –32768 to +32767.

⇒ **Note:** The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula as shown on the next page.

In scan mode, the behavior is the same except that when the program initiates a conversion, all channels in the programmed channel range will be sampled once, and the data will be stored in the FIFO. The FIFO depth register will increment by the scan size. When STS goes low, the program should read out the data for all channels.

14.7 Convert the numerical data to a meaningful value

Once you have the A/D value, you need to convert it to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards you may need to convert the voltage to some other engineering units (for example, the voltage may come from a temperature sensor, and then you would need to convert the voltage to the corresponding temperature according to the temperature sensor's characteristics).

Since there are a large number of possible input devices, this secondary step is not included here; only conversion to input voltage is described. However you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas:

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input range

Example: Input range is ±5V and A/D value is 17761:
Input voltage = 17761 / 32768 * 5V = 2.710V

For a bipolar input range, 1 LSB = 1/32768 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for ±5V range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
…	…	…
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
…	…	…
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example: Input range is 0-5V and A/D value is 17761:
Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a unipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for 0-5V range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
…	…	…
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
…	…	…
32767	V_{FS} - 1 LSB	4.9999V

15. A/D SCAN, INTERRUPT, AND FIFO OPERATION

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an AD conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion, first LSB, then MSB. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in Base + 2. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

If the FIFO reaches its limit of 48 samples, then the next time an A/D conversion occurs the Overflow flag OVF will be set. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 1, or a hardware reset must occur.

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold should be set to 8, 16, 24, 32, 40, or 48, but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

Prometheus A/D Operating Modes

The following control bits and values are referenced in the descriptions in the table below.

AINTE	Base + 4 bit 0
SCANEN	Base + 3 bit 2
FIFO threshold	Base + 5 bits 5-0
STS	Base + 3 bit 7
LOW, HIGH	4-bit channel nos. in Base + 2
ADCLK	Base + 4 bit 4

AINTE	SCANEN	Operation
0	0	Single A/D conversions are triggered by write to B+0. STS stays high during the A/D conversion. No interrupt occurs. The user program monitors STS and reads A/D data when it goes low.
0	1	A/D scans are triggered by write to B+0. All channels between LOW and HIGH will be sampled. STS stays high during the entire scan (multiple A/D conversions). No interrupt occurs. The user program monitors STS and reads all A/D values when it goes low.
1	0	Single A/D conversions are triggered by the source selected with ADCLK. STS stays high during the A/D conversion. A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.
1	1	A/D scans are triggered by the source selected with ADCLK. STS stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.

16. ANALOG OUTPUT RANGES AND RESOLUTION

16.1 Description

Prometheus uses a 4-channel 12-bit D/A converter (DAC) to provide 4 analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB (the theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve).

⇒ **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the same thing.

16.2 Resolution

The *resolution* is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, and so this change is referred to as 1 LSB, or 1 least significant bit. The value of this LSB is calculated as follows:

1 LSB = Output voltage range / 4096

Example: Output range = 0-10V;

Output voltage range = 10V – 0V = 10V

1 LSB = 10V / 4096 = 2.44mV

Example: Output range = ±10V;

Output voltage range = 10V – (-10V) = 20V

1 LSB = 20V / 4096 = 4.88mV

16.3 Output Range Selection

Jumper block J13 is used to select the DAC output range. See page 45 for configuration data. The DACs can be configured for 0-10V or ±10V.

Two parameters are configured: unipolar/bipolar mode and power-up/reset clear mode. In most case, for unipolar mode set the board to reset to zero scale, and for bipolar mode configure the board for reset to mid-scale. In each case the DACs will reset to 0V.

16.4 D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages.

D/A Conversion Formulas for Unipolar Output Ranges

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example: Output range in unipolar mode = 0 – 10V
Full-scale range = 10V – 0V = 10V
Desired output voltage = 2.000V
D/A code = 2.000V / 10V * 4096 = 819.2 => 819

Note the output code is always an integer.

For the unipolar output range 0-10V, 1 LSB = 1/4096 * 10V = 2.44mV.

Here is an illustration of the relationship between D/A code and output voltage for a unipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for 0 – 10V range
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0024V
…	…	…
2047	V_{REF} / 2 - 1 LSB	4.9976V
2048	V_{REF} / 2	5.0000V
2049	V_{REF} / 2 + 1 LSB	5.0024V
…	…	…
4095	V_{REF} - 1 LSB	9.9976V

D/A Conversion Formulas for Bipolar Output Ranges

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example: Output range in bipolar mode = ±10V
Full-scale range = 10V – (-10V) = 20V
Desired output voltage = 2.000V
D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

For the bipolar output range ±10V, 1 LSB = 1/4096 * 20V, or 4.88mV.

Here is an illustration of the relationship between D/A code and output voltage for a bipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for ±10V range
0	$-V_{REF}$	-10.0000V
1	$-V_{REF}$ + 1 LSB	-9.9951V
…	…	…
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
…	…	…
4095	V_{REF} - 1 LSB	9.9951V

17. GENERATING AN ANALOG OUTPUT

This chapter describes the steps involved in generating an analog output (also called performing a D/A conversion) on a selected output channel using direct programming (not with the driver software).

There are three steps involved in performing a D/A conversion:

1. **Compute the D/A code for the desired output voltage**
2. **Write the value to the selected output channel**
3. **Wait for the D/A to update**

17.1 Compute the D/A code for the desired output voltage

Use the formulas on the preceding page to compute the D/A code required to generate the desired voltage.

⇒ **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.

17.2 Write the value to the selected output channel

First use the following formulas to compute the LSB and MSB values:

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

Output code = 1776

LSB = 1776 & 255 = 240 (F0 Hex); MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded DOWN. The truncated portion is accounted for by the LSB.

Now write these values to the selected channel. The LSB is written to Base + 6. The MSB and channel number are written to Base + 7. The 2-bit channel no. (0-3) is written to bits 7 and 6, and the MSB is written to bits 3-0.

```
outp(Base + 6, LSB);
outp(Base + 7, MSB + channel << 6);
```

17.3 Wait for the D/A to update

Writing the MSB and channel number to Base + 7 starts the D/A update process for the selected channel. The update process requires approximately 30 microseconds to transmit the data serially to the D/A chip and then update the D/A circuit in the chip. During this period, no attempt should be made to write to any other channel in the D/A through addresses Base + 6 or Base + 7.

The status bit DACBUSY (Base + 3 bit 4) indicates whether the D/A is busy updating (1) or idle (0). After writing too the D/A, monitor this bit until it is zero before proceeding to the next D/A operation.

18. ANALOG CIRCUIT CALIBRATION

Calibration applies only to boards with the analog I/O circuit.

The analog I/O circuit is calibrated during production test prior to shipment. Over time the circuit may drift slightly. If calibration is desired follow the procedure below. For analog I/O circuit configuration see page 45.

Four adjustments are possible:

- A/D bipolar offset
- A/D unipolar offset
- A/D full-scale
- D/A full-scale

No adjustment for D/A offset is possible.

18.1 A/D bipolar offset

Potentiometer **R66** is used for adjustment. Configure the circuit for Bipolar A/D mode. Input 0V to any input channel and perform A/D conversions on that channel. The gain setting and single-ended vs. differential mode do not matter. Adjust R66 until the A/D value is 0. To eliminate the effects of noise, it is best to take a number of readings and average the values.

18.2 A/D unipolar offset

Potentiometer **R67** is used for adjustment. Configure the circuit for Unipolar A/D mode. The gain setting and single-ended vs. differential mode do not matter. Input 0V to any input channel and perform A/D conversions on that channel. Adjust R67 until the A/D value is 0~1. To eliminate the effects of noise, it is best to take a number of readings and average the values.

18.3 A/D full-scale

Potentiometer **R74** is used for adjustment. Configure the circuit for Bipolar A/D mode ±10V. Input 9.9945V to any input channel and perform A/D conversions on that channel using a gain setting of 1. Single-ended vs. differential mode does not matter. Adjust R74 until the average A/D value is 32750. To eliminate the effects of noise, it is best to take a number of readings and average the values.

Any input voltage and A/D reading near the top of the range (10V) can be used for the calibration target voltage/reading. The above value is provided as an example.

18.4 D/A full scale

Potentiometer **R89** is used for adjustment. Configure the D/A for 0-10V output range. Write the output code of 4095 to all four D/A channels. Measure each one and adjust R89 until the average reading is as close to 9.9976 as possible.

19. DIGITAL I/O OPERATION

Prometheus contains 24 digital I/O lines organized as three 8-bit I/O ports, A, B, and C. The direction for each port is programmable, and port C is further divided into two 4-bit halves, each with independent direction. The ports are accessed at registers Base + 8 through Base + 10 respectively, and the direction register is at Base + 11.

Base +	7	6	5	4	3	2	1	0
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR			DIRA	DIRCH		DIRB	DIRCL

The digital I/O lines are located at pins 1 through 24 on the I/O header J14 (see page 14). They are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state. See the specifications on page 62 for more detail.

DIRA, DIRB, DIRCH, and DIRCL control the direction of ports A, B, C4-7, and C0-3. A 0 means output and a 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

DIOCTR is used to control the function of lines C7-C4 on the I/O connector. When DIOCTR=1, the lines are C7-C4. When DIOCTR=0, these lines are counter/timer lines:

Pin No.	DIOCTR = 1	DIOCTR = 0	Pin direction for DIOCTR = 0
21	C4	Gate 0	Input
22	C5	Gate 1	Input
23	C6	Clk 1	Input
24	C7	Out 0	Output

20. COUNTER/TIMER OPERATION

Prometheus model PR-Z32-EA contains two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA. See pages 38 and 43 for information on the counter/timer control register bits and how to perform various functions using these counters.

20.1 Counter 0 – A/D Sample Control

The first counter, Counter 0, is a 24-bit "divide-by-n" counter used for controlling A/D sampling. The counter has a clock input, a gate input, and an output. The input is a 10MHz or 1MHz clock provided on the board and selected with bit CKFRQ0 in Base + 4 bit 5. The gate is an optional signal that can be input on pin 21 of the I/O header J14 when DIOCTR (Base + 11 bit 7) is 1. If this signal is not used then the counter runs freely. The output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output appears on pin 24 of the I/O header when DIOCTR=1.

The counter operates by counting down from the programmed divisor value. When it reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 1μs, depending on the input clock selected by CKFRQ0). It then reloads to the initial load value and repeats the process indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) down to 0.06Hz (1MHz clock divided by 16,777,215, or 2^{24}-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when AINTE is 1 and ADCLK is 0 in Base + 4. Using the control register at Base + 15 the counter can be loaded, cleared, enabled, and disabled, the optional gate can be enabled and disabled, and the counter value can be latched for reading.

20.2 Counter 1 – Counting/Totalizing Functions

The second counter, Counter 1, is similar to Counter 0 except it is a 16-bit counter. It also has an input, a gate, and an output. These signals may be user-provided on the I/O header when DIOCTR=0 or the input may come from the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100KHz as determined by control bit CKFRQ1 in Base + 4.

The output is a positive-going pulse that appears on pin 26 of the I/O header. The output pulse occurs when the counter reaches zero. When the counter reaches zero it will reload and start over on the next clock pulse. The output stays high the entire time the counter is at zero, i.e. from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When DIOCTR=0, Counter 1 operates as follows: It counts positive edges of the signal on pin 23 on the I/O header. The gate is provided on pin 22. If it is high then the counter will count, and if it is low the counter will hold its value and ignore input pulses. This pin has a pull-up so the counter can operate without any external gate signal.

NOTE: When counting external pulses, Counter 1 will only update its read register every 4th pulse. This behavior is due to the synchronous design of the counter having to contend with the asynchronous input pulses. The count register contents are correct on the 4th pulse but will remain static until 4 more pulses occur on the input.

When DIOCTR=1, Counter 1 operates as follows: It takes its input from the on-board clock generator based on the value of the CKFRQ1 bit in Base + 4. There is no gating and the counter runs continuously.

Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode the output signal on pin 26 is of interest. In totalizer/counter mode the counter value is of interest and may be read by first latching the value and then reading it.

20.3 Command Sequences

Diamond Systems provides driver software to control the counter/timers on Prometheus. The information here is intended as a guide for programmers writing their own code in place of the driver and also to give a better understanding of the counter/timer operation.

The counter control register is shown below.

Base + 15 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

To make a counter run (load and enable a counter)

1. Load the desired initial value into the counter.
2. If you want to use the gate function, enable the gate.
3. Enable the counter.

To read a counter

1. Latch the counter. The counter continues to operate.
2. Read the value from the data registers.

A counter may be enabled or disabled at any time. If disabled, the counter will ignore incoming clock edges.

The gating may be enabled or disabled at any time. When gating is disabled, the counter will count all incoming edges. When gating is enabled, if the gate is high the counter will count all incoming edges, and if the gate is low the counter will ignore incoming clock edges.

Loading and enabling a counter

For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

a. Write the data to the counter:

Break the load value into 3 bytes, low, middle, and high (two bytes for counter 1). Then write the bytes to the data registers in any sequence.

Counter 0
```
outp(base+12,low);
outp(base+13,middle);
outp(base+14,high);
```

Counter 1
```
outp(base+12,low);
outp(base+13,high);
```

b. Load the counter:

Counter 0
```
outp(base+15,0x02);
```

Counter 1
```
outp(base+15,0x82);
```

c. Enable the gate if desired:

Counter 0
```
outp(base+15,0x10);
```

Counter 1
```
outp(base+15,0x90);
```

d. Enable the counter:

Counter 0
```
outp(base+15,0x04);
```

Counter 1
```
outp(base+15,0x84);
```

Reading a counter

a. Latch the counter:

Counter 0	**Counter 1**
outp(base+15,0x40);	outp(base+15,0xC0);

b. Read the data:

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1)

Counter 0	**Counter 1**

low=inp(base+12);
middle=inp(base+13);
high=inp(base+14);
	low=inp(base+12);
	high=inp(base+13);

c. Assemble the bytes into the complete counter value:

Counter 0	**Counter 1**
val = high * 2^16 + middle * 2^8 + low;	val = high * 2^8 + low;

Enabling the counter gate

Counter 0	**Counter 1**
outp(base+15,0x10);	outp(base+15,0x90);

The counter will run only when the gate input is high.

Disabling the counter gate

Counter 0	**Counter 1**
outp(base+15,0x20);	outp(base+15,0xA0);

The counter will run continuously.

Clearing a counter

Clearing a counter is done when you want to restart an operation. Normally you only clear a counter after you have stopped (disabled) and read the counter. If you clear a counter while it is still enabled, it will continue to count incoming pulses, so its value may not stay at zero.

a. Stop (disable) the counter:

Counter 0	**Counter 1**
outp(base+15,0x08);	outp(base+15,0x88);

b. Read the data (optional). See “Reading a counter” above.

c. Clear the counter:

Counter 0	**Counter 1**
outp(base+15,0x01);	outp(base+15,0x81);

21. DATA ACQUISITION SPECIFICATIONS

Analog Inputs (PR-Z32-EA only)

No. of inputs	8 differential or 16 single-ended (user selectable)
A/D resolution	16 bits (1/65,536 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1.25V Unipolar: 0-10V, 0-5V, 0-2.5V
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Overvoltage protection	±35V on any analog input without damage
Nonlinearity	±3LSB, no missing codes
Drift	5PPM/^{o}C typical
Conversion rate	100,000 samples per second max
Conversion trigger	software trigger, internal pacer clock, or external TTL signal
FIFO	48 samples; programmable interrupt threshold

Analog Outputs (PR-Z32-EA only)

No. of outputs	4
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0-10V or user-programmable Bipolar: ±10V or user-programmable
Output current	±5mA max per channel
Settling time	4μS max to ±1/2 LSB
Relative accuracy	±1 LSB
Nonlinearity	±1 LSB, monotonic

Digital I/O (PR-Z32-EA only)

No. of lines	24
Compatibility	3.3V and 5V logic compatible
Input voltage	Logic 0: -0.5V min, 0.8V max; Logic 1: 2.0V min, 5.5V max
Input current	±1μA max
Output voltage	Logic 0: 0.0V min, 0.4V max; Logic 1: 2.4V min, 3.3V max
Output current	Logic 0: 12mA max; Logic 1: -8mA max
I/O capacitance	10pF max

Counter/Timers (PR-Z32-EA only)

A/D pacer clock	24-bit down counter
Pacer clock source	10MHz, 1MHz, or external signal
General purpose	16-bit down counter
GP clock source	10MHz, 100KHz, or external signal

General

Power supply	+5VDC ±5%
Current consumption	0.7A – 1.1A typical
Operating temperature	-40 to +85^{o}C
Operating humidity	5% to 95% noncondensing

22. FLASHDISK MODULE

Prometheus is designed to accommodate an optional flashdisk module. This module contains 32MB to 128MB of solid state non-volatile memory that operates like an IDE drive without requiring any additional driver software support.

Model	Capacity
FD-32	32MB
FD-64	64MB
FD-96	96MB
FD-128	128MB

22.1 Installing the Flashdisk Module

The flashdisk module installs directly on the IDE connector J8 and is held down with a spacer and two screws onto a mounting hole on the board. It fits within the height limit of the PC/104 specification, so another board may be installed on top of the Prometheus CPU.

The flashdisk module contains a jumper for master/slave configuration. For master, install the jumper over pins 1&2, and for slave install the jumper over pins 2&3.

22.2 Configuration

To configure the CPU to work with the Flashdisk module, enter the BIOS (press F2 during startup). Select the Main menu, then select IDE Primary Master. Enter the following settings:

Type:	User
Cylinders:	489 for 32MB flashdisk
Heads:	4 for 32MB flashdisk
Sectors:	32 for 32MB flashdisk
Multi Sector Transfer:	Disable
LBA Mode Control:	Enable
32 Bit I/O:	Disable
Transfer Mode:	Fast PIO 1
Ultra DMA Mode:	Disable

Exit the BIOS and save your change. The system will now boot and recognize the FlashDisk module as drive C:.

22.3 Using the Flashdisk with Another IDE Drive

Since the flashdisk occupies the board's IDE connector, mounting it on the board prevents the simultaneous use of another IDE drive. To utilize both the flashdisk and another drive, an adapter board, such as Diamond Systems' ACC-IDEEXT, and cables are required. The ACC-IDEEXT adapter board is described on page 69.

22.4 Power Supply

The 44-pin cable carries power from the CPU to the adapter board and will power the flashdisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the CPU's power out connector (J12) or from one of the two 4-pin headers on the ACC-IDEEXT board. Diamond Systems' cable no. **698006** may be used with either power connector to bring power to the drive.

23. I/O PANEL BOARD

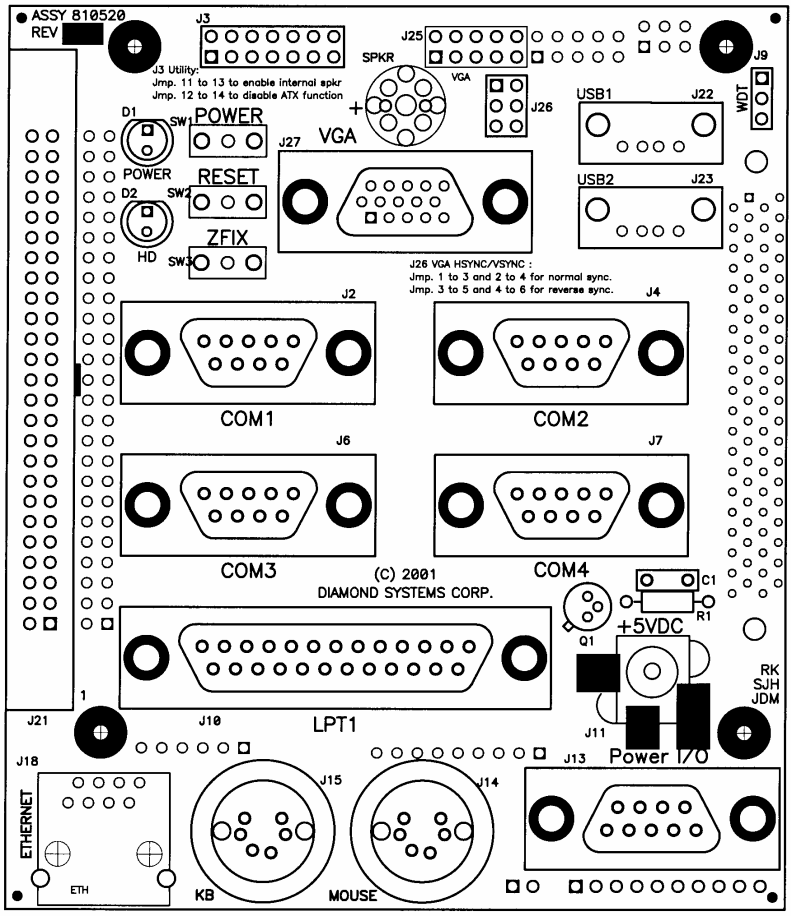
23.1 Description

An I/O panel board accessory is available to convert all I/O headers on Prometheus to industry-standard connectors. Using this panel board eliminates all internal cables, resulting in increased ruggedness and quicker assembly. In addition a standard precut cover plate is available to enable mounting the panel board and CPU in Diamond Systems' **Pandora** enclosure system.

The panel board is available in two models:

PNL-Z32-E Mates with **PR-Z32-E-ST** CPU with ethernet and no data acquisition circuit

PNL-Z32-EA Mates with **PR-Z32-EA-ST** CPU with ethernet and data acquisition circuit



PNL-Z32-E / PNL-Z32-EA *I/O Panel Board for Prometheus*

23.2 Panel Board I/O Connectors

The I/O connectors below are located on the top side of the board and are for connection to external equipment.

Location	Type	Description
J2	DB-9M	Serial port COM1
J4	DB-9M	Serial port COM2
J6	DB-9M	Serial port COM3
J7	DB-9M	Serial port COM4
J10	DB-25F	Parallel port LPT1
J11	2.5mm	+5VDC input power (tip = +, ring = -)
J13	DB-9M	Multi I/O power connector
J14	MD-6	PS/2 mouse connector
J15	MD-6	PS/2 keyboard connector
J18	RJ-45	Ethernet connector
J21	IDC-50	Data acquisition connector (Model PNL-Z32-EA only)
J22	USB A	USB connector
J23	USB A	USB connector
J27	DB-15F	Video (VGA) connector

Panel Board Top Side / External Use I/O Connectors

Additional connectors are on the bottom side and are intended for use with other boards and circuitry inside the enclosure, such as a video board or DC/DC power supply.

Location	Type	Description
J3	Pin header	Speaker and miscellaneous functions
J5	Pin header	Power connection to DC/DC power supply input
J12	Pin header	Power connection to/from DC/DC power supply
J25	Pin header	Pass-through connector for VGA board

Panel Board Bottom Side / Internal Use I/O Connectors

23.3 Panel Board Cables

The panel board ships with a 10-wire video cable (DSC part no. **698010**) and a 2-wire power cable (DSC part no. **698011**). These are intended for use with the optional accessory video board and a Jupiter-MM (JMM) power supply when these boards are used together with the Prometheus CPU and panel board.

The 10-wire video cable connects the VGA output of the video board to pin header J25 on the panel board. J25 is compatible with a number of companies' PC/104 video boards that provide a 10-pin connector for the video out.

23.4 Panel Board Hardware

The panel board also comes with mounting hardware for installing it and the CPU into an enclosure such as the Pandora system.

23.5 Panel Board Power Connections

Prometheus requires only +5V for operation. The panel boad is simply a connector board and requires no power. Make sure that the power supply used has enough current capacity to drive your system. The Prometheus CPU requires up to 1.1A. If you have a disk drive or other modules connected, you need additional power. In particular, many disk drives need extra current during startup. If your system fails to boot properly, or if disk accesses do not work properly, the first thing to check is the power supply voltage level. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the +5V supply.

The panel board has two external input power connectors, J11 and J13, to satisfy a variety of input power scenarios.

J11 is a circular jack with a 2.5mm post. This connector is intended for direct 5VDC +/-5% input from the Diamond Systems PS-5VUS-01 wall adapter or an equivalent supply. The polarity for the power connector is tip = +5V, ring = Ground.

J13 is a DB9 male connector with multiple input voltages and applications. If a latching connector is required, the DB9 can be used in place of the circular jack to provide +5VDC.

If multiple system voltages are required, for example +5V, -5V, +12V, and/or -12V, these voltages can be supplied through J13 as well. The +5V and +12V are controlled by the CPU's ATX power circuit, while the -5V and -12V are connected directly to the PC/104 bus pins.

J13 can also be used with a DC/DC power supply, such as Diamond Systems' Jupiter-MM modules, in applications where the supply voltage is different from the required +5V. In this scenario, the input voltage is fed to the DB9 and routed to the power supply with cable connected between the supply and connector J5 or J12 on the bottom side of the panel board.

J5 is used when the power is to be routed from the output of the power supply directly onto the PC/104 bus through the PC/104 bus connectors on the power supply. In this application use the 2-wire power cable no. 698011. This cable contains a blue positive wire and a black negative wire. Connect the blue wire to the + screw terminal on the JMM power supply input connector and connect the black wire to the – terminal. Either J4 or J5 on the JMM board may be used for the power connection.

J12 is used when the supply voltages are intended to be switched by the ATX circuit on Prometheus. In this application the input and output of the power supply are connected to J12. The +5V and +12V are controlled by the ATX function, while the -5V and -12V are connected directly to the PC/104 bus pins.

1	-12V In
2	-5V In
3	Ground
4	+5V In
5	+5V In
6	+12V In
7	Ground
8	Power Input
9	Ground
10	Shutdown/ATX

J12 pinout (to/from DC/DC power supply)

1	Power Switch
2	Power Input
3	+12V In
4	+5V In
5	Ground
6	Power Input
7	Shutdown
8	+5V In
9	Ground

J13 pinout (user connection)

23.6 Speaker and Miscellaneous Connector

J3 is used for optional connection of an auxiliary speaker or control switches.

The panel board contains a miniature speaker which is enabled by default. To enable this speaker, install a jumper across pins 11 and 13 of J3 (default setting). If a different speaker is desired, or if no speaker is desired, remove the jumper.

To connect an auxiliary speaker, connect the speaker across pins 7-8 (for a speaker with a 2-pin 2-position housing) or across pins 7-13 (for a speaker with a 2-pin 4-position housing when the two wires are on the two end positions of the housing).

External momentary switches may be connected to J3 to control power or reset. For power, connect the switch between pins 1 and 2 of J3. For reset, connect the switch between pins 3 and 4. Each switch operates by connecting the selected control signal to ground.

To lock out the keyboard and mouse ports on the panel board, install a jumper across pins 5-6.

To disable the ATX power function, connect a jumper across pins 12 and 14 on J3.

An auxiliary switched +5V pin is provided on J3 for customer application. In addition the unswitched power may be used on this header to power a panel light or other customer circuit, with the current limited to 1A.

Ground	1	2	Power Switch
Ground	3	4	Reset Switch
Ground	5	6	Keyboard/Mouse Lockout
+5VDC Unswitched	7	8	Speaker
+5VDC Switched	9	10	N/C
Internal Speaker	11	12	Ground
Speaker	13	14	ATX Disable

J3 Pinout

23.7 Watchdog Timer

J9 may be used to connect an external watchdog timer circuit to the CPU. For watchdog timer programming information, see page 20 and the ZFx86 Training Manual included in the Documents folder of the Prometheus CD.

1	Ground
2	Watchdog In
3	Watchdog Out

J9 Pinout

23.8 Installation

The panel board includes a hardware kit containing spacers of various sizes along with screws and nuts. There are three sizes of spacers: 7mm (0.276”), 14mm (0.551”), and 0.600”. All hardware for assembling the stack and mounting it to the enclosure front panel is #4-40 thread.

The Pandora enclosure includes an additional hardware kit of #6-32 screws for assembling the front and back panels to the enclosure body. Refer to the assembly drawings provided with the panel board for proper assembly of the PC/104 stack and Pandora enclosure.

The panel board connects to the following headers on the Prometheus CPU:

J3 Main I/O
J4 Ethernet
J5 USB
J6 Watchdog timer
J11 Input power
J14 Data acquisition (-EA models)

To install the panel board onto the Prometheus CPU board, first remove any jumpers on J6 of the CPU (upper right corner) since these will interfere with the mating header on the bottom of the panel board.

Insert the four 7mm male/female hex spacers into the holes on top of the panel board and fix them in place with the four 14mm female/female hex spacers below. Then plug the panel board onto the connectors of the CPU board, being careful to align all the connectors properly. Note that there are mating connectors on all 4 edges of the board for the –EA (analog I/O) version, and connectors on 3 sides for the -E (no analog I/O) version.

When the boards are properly mated, the 80-pin high-density connectors on the right edges of the boards will seat completely, while the pin headers on the other sides will show a slight gap. This is normal and does not cause any problem with reliable connections on these connectors. If you do not install the 14mm spacers between the two boards, you will still be able to mate the two boards satisfactorily, but they will be slightly tilted, since the high-density connector has a slightly larger board-to-board distance than the other pin headers.

The board stack may be mounted inside the Pandora enclosure in one of two ways. The stack may “hang” from the front panel, or it may be mounted to both the front and rear panel. The assembly drawings included with the Pandora enclosure show both options. The stack mounts to the front panel with four #4 flat head screws that install onto the four spacers on the top of the panel board as well as 14 #4 screwlocks that connect to the 7 Dsub connectors on the panel board.

Finally select one of the two options for fixing the bottom of the stack. Either install four #4 pan head screws on the bottom of the CPU board into the four spacers between it and the panel board, or attach the four 0.6” male/female round PC/104 spacers on the bottom of the board and then install four #4 flat head screws through the case’s rear panel into the PC/104 spacers.

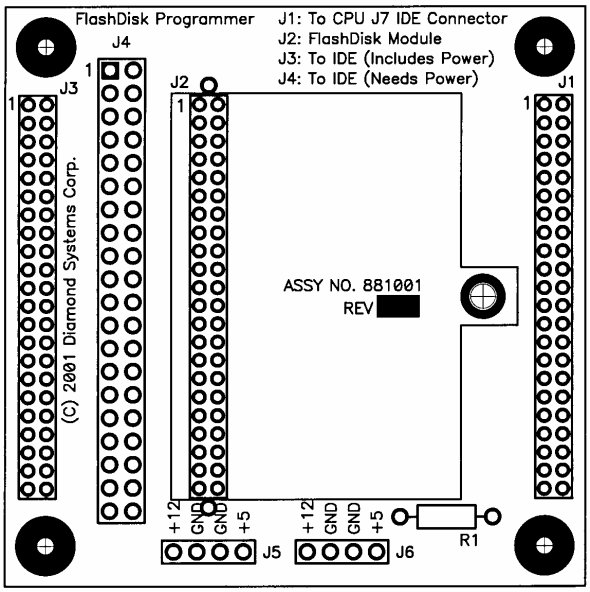
24. FLASH DISK PROGRAMMER BOARD

The Flash Disk Programmer Board accessory model no. **ACC-IDEEXT** may be used for several purposes. Its primary purpose is to enable the simultaneous connection of both a flashdisk module and a standard IDE hard drive or CD-ROM drive to allow file transfers to/from the flashdisk. This operation is normally done at system setup. The board can also be used to enable the simultaneous connection of two drives to the CPU.

J1 connects to the IDE connector on Prometheus with a 44-pin ribbon cable (Diamond Systems' part no. **698004**). Both 40-pin .1" spacing (J4) and 44-pin 2mm spacing (J3) headers are provided for the external hard drive or CD-ROM drive. A dedicated connector (J2) is provided for the flashdisk module. Any two devices may be connected simultaneously using this board with proper master / slave jumper configurations on the devices.

The Flash Disk Programmer Board comes with a 44-wire cable no. (DSC no. **698004**) and a 40-wire cable no. (DSC no. **C-40-18**) for connection to external drives. The flashdisk module is sold separately.

The 44-pin connector (J1, J2, and J3) and mating cable carry power, but the 40-pin connector (J4) and mating cable do not. J5 and J6 on the accessory board may be used to provide power to a 44-pin device attached to the board when the board is attached to a PC via a 40-pin cable. These headers are compatible with the floppy drive power connector on a standard PC internal power cable.



***ACC-IDEEXT** FlashDisk Programmer Board*

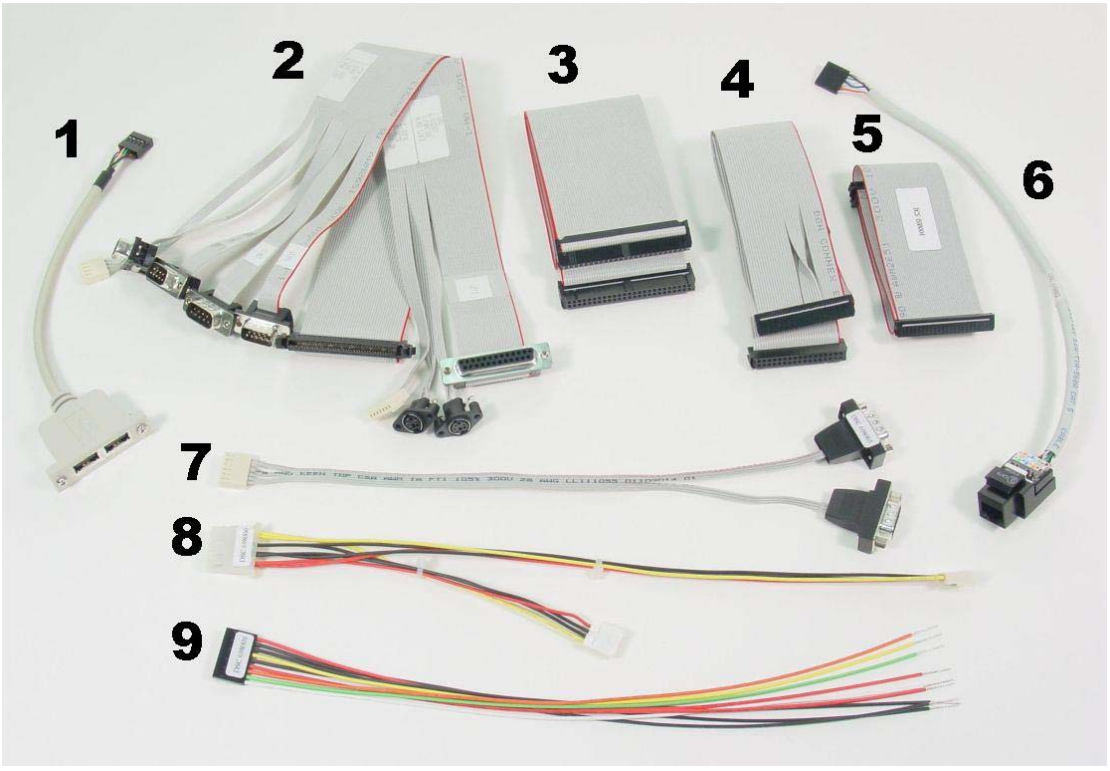
25. I/O CABLES

When the panel I/O board PNL-Z32 is used, no cabling or wiring is required to operate the CPU (unless you want to connect to an external IDE drive or floppy drive). However for custom installations as well as development, Diamond Systems offers a cable kit no. **C-PRZ-KIT** with 9 cables to connect to all I/O headers on the board. Some cables are also available separately.

The mating cable for each I/O connector is listed in Chapter 4.

NOTE: When the multi-I/O cable C-PRZ-01 or any other cable is connected to serial ports 1 or 2, the serial port signals must terminate to another board, or interference problems may occur that will slow down the performance of your CPU.

Photo No.	Cable No.	Description
2	C-PRZ-01	80-wire / 2-cable breakout cable assembly with serial, parallel, PS/2 mouse/keyboard, power, reset, speaker, & LED connectors
6	C-PRZ-02	6-wire Ethernet cable with panel-mount RJ-45 connector
3	C-50-18	50-wire data acquisition cable
5	698004	44-wire IDE cable for 1 or 2 drives
7	698005	6-wire auxiliary serial port cable
8	698006	4-wire output power cable for external drives
4	698008	34-wire floppy cable for 1 or two drives
9	698009	9-wire input power cable with stripped/tinned leads for connection to external power source
1	698012	Dual USB cable



Cable Kit C-PRZ-KIT

26. VGA ACCESSORY BOARD

The Prometheus development kit ships with a PC/104 VGA module from Arcom Control Systems, model no. **AIM-104-VGA-CRT-OEM**. The Diamond Systems part no. for this board is **ACC-VGA-02**.

The VGA board has several configuration jumpers, LK1 – LK3. Their functions are described in the board's documentation. For proper operation with Prometheus, jumper LK1 must be out.

The VGA output connector on the Arcom board is a 16-pin connector labeled PL5, located on the left edge of the board. When used with the Diamond Systems panel board model PNL-Z32-E / EA, this connector connects to the 10-pin VGA input header J25 on the panel board using Diamond Systems cable no. **698013**. The pinout of this cable is shown below. Each row represents one wire on the cable.

PL5 pin no.	PL5 Signal	J25 pin no.	J25 Signal
1	Red	1	Red
2	Red Return	2	Ground
3	Green	3	Green
4	*Not connected*	4	Ground
5	Blue	5	Blue
6	Green Return	6	Ground
7	*Not connected*	-	*Not connected*
8	*Not connected*	8	PCB shield
9	Blue Return	-	*Not connected*
10	Ground	-	*Not connected*
11	Ground	-	*Not connected*
12	H Sync	7	H Sync
13	*Not connected*	-	*Not connected*
14	V Sync	9	V Sync
15, 16	*Not connected*	-	*Not connected*

To connect PL5 directly to a VGA monitor with a high-density DB15 connector, use the multicolor ribbon cable supplied with the video board. This cable has the following pinout:

PL5 pin no.	DB15F pin no.	Signal
1	1	Red
2	6	Red Return
3	2	Green
4	4	*No Function*
5	3	Blue
6	7	Green Return
7	9	*No Function*
8	11	*No Function*
9	8	Blue Return
10	5	Ground
11	10	Ground
12	13	H Sync
13	12	*No Function*
14	14	V Sync
15	15	*No Function*
16	-	*No Wire*

27. MOUNTING PROMETHEUS ON A BASEBOARD

Prometheus is designed to allow installation upside down onto a custom baseboard. The CPU board may be thought of as a "macro-component" when used in this way. All the key I/O headers on the board face up and are at an even height, allowing the board to be turned over and mounted onto a base board. A mechanical drawing showing locations of mating connectors on the baseboard is shown on the following page.

The board-to-board mounting height for this application is 14mm (.551"). Spacers for this application can be purchased from many suppliers of metric hardware. Standard spacers with metric length will have metric threads (for example M3 x 0.5). Diamond Systems can supply a custom-designed 14mm aluminum hex male/female spacer with #4-40 threads (DSC part no. 684045).

Using the board in this manner eliminates all connecting cables for most applications. All connections except IDE, floppy drive, and switched power output are accessible through the vertical I/O headers on the board. If you need to use IDE, floppy, or switched power output, you will need to use cables to access the corresponding I/O headers.

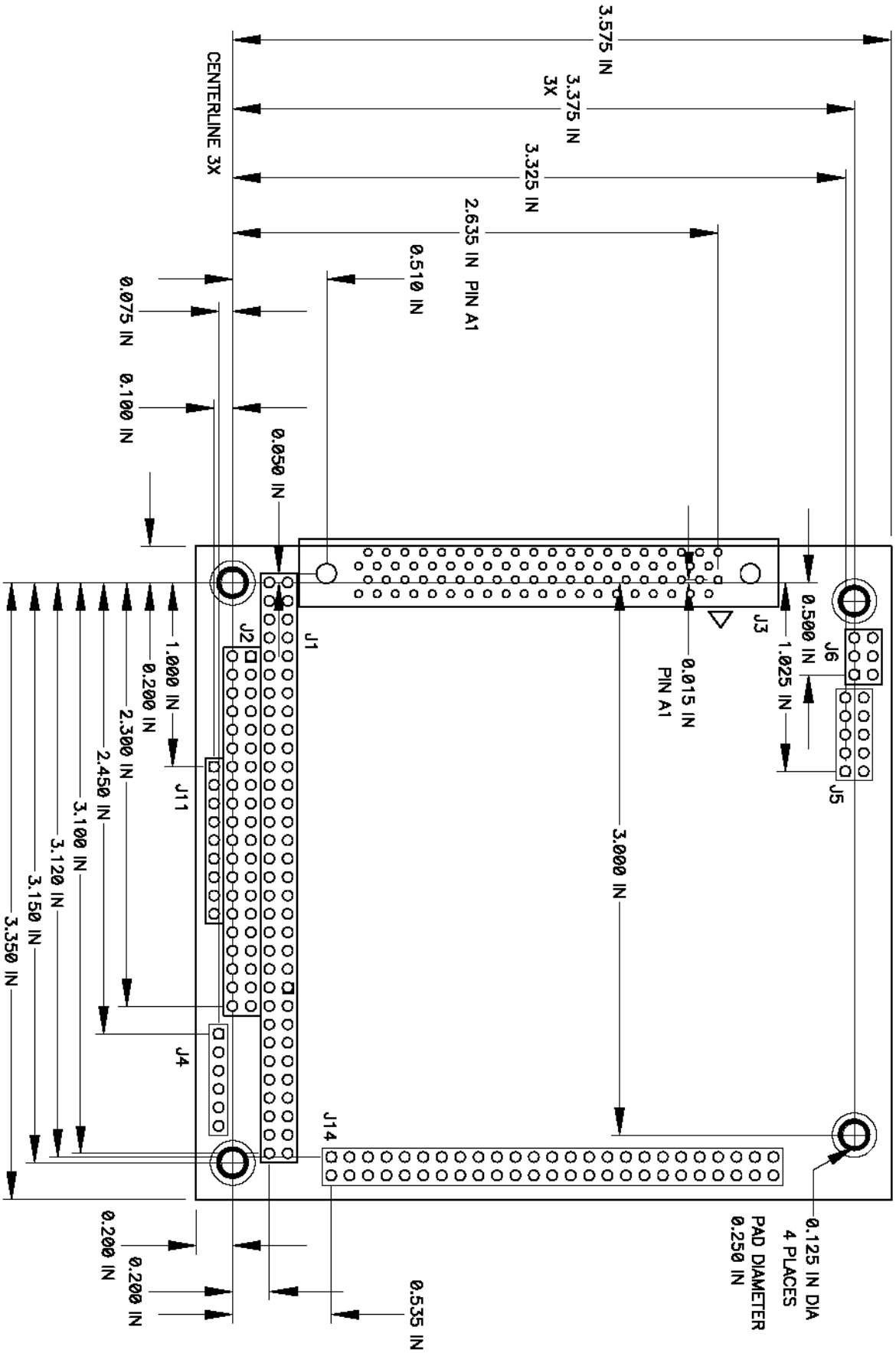
The following is a list of I/O headers that mate with the corresponding vertical-mount I/O headers on Prometheus:

Prometheus Connector	Manufacturer	Manufacturer Part No.
J1	Generic	.1" dual row pin header, 2x32
J2	Generic	.1" dual row pin header, 2x20
J3	3M / Robinson Nugent	P50-080S-R1-TG
J4	G-LINKS	PSPH1-1X6GOB11.05-2.3
	Samtec	ESQ-106-12-G-S
J5	G-LINKS	PSPH1-2X5GOB11.05-2.3
	Samtec	ESQ-105-12-G-D
J6	G-LINKS	PSPH1-2X3GOB11.05-2.3
	Samtec	ESQ-103-12-G-D
J11	G-LINKS	PSPH1-1X9GOB11.05-2.3
	Samtec	ESQ-109-12-G-S
J14	G-LINKS	PSPH1-2X25GOB11.05-2.3
	Samtec	ESQ-125-12-G-D

Website information:

G-Links (Taiwan)	www.g-links.com.tw
Samtec	www.samtec.com
3M	www.3m.com/us/electronics_mfg/interconnects/

Note: The -12- in the Samtec part numbers above indicates standard insertion force components. This may be replaced by -37- for low insertion force components. Because of the number and location of the mating headers, the effort to remove the Prometheus from a mating board is significant and requires careful effort. Therefore low-insertion force components may be preferred.



28. PC/104 MECHANICAL DRAWING

The following drawing is from the PC/104 specification. This document may be downloaded from www.pc104.org or from www.diamondsystems.com/support/techliterature.