



**CY7C1146V18, CY7C1157V18  
CY7C1148V18, CY7C1150V18**

# 18-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)

## Features

- 18 Mbit density (2M x 8, 2M x 9, 1M x 18, 512K x 36)
- 300 MHz to 375 MHz clock for high bandwidth
- 2-Word burst for reducing address bus frequency
- Double Data Rate (DDR) interfaces (data transferred at 750 MHz) at 375 MHz
- Read latency of 2.0 clock cycles
- Two input clocks (K and  $\bar{K}$ ) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and  $\bar{CQ}$ ) simplify data capture in high-speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- Core  $V_{DD} = 1.8V \pm 0.1V$ ; IO  $V_{DDQ} = 1.4V$  to  $V_{DD}$ <sup>[1]</sup>
- HSTL inputs and Variable drive HSTL output buffers
- Available in 165-Ball FBGA package (13 x 15 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1-compatible test access port
- Delay Lock Loop (DLL) for accurate data placement

## Configurations

**With Read Cycle Latency of 2.0 cycles:**

- CY7C1146V18 – 2M x 8
- CY7C1157V18 – 2M x 9
- CY7C1148V18 – 1M x 18
- CY7C1150V18 – 512K x 36

## Selection Guide

Description	375 MHz	333 MHz	300 MHz	Unit
Maximum Operating Frequency	375	333	300	MHz
Maximum Operating Current	1020	920	850	mA

## Functional Description

The CY7C1146V18, CY7C1157V18, CY7C1148V18, and CY7C1150V18 are 1.8V Synchronous Pipelined SRAMs equipped with DDR-II+ architecture. The DDR-II+ consists of an SRAM core with advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and  $\bar{K}$ . Read data is driven on the rising edges of K and  $\bar{K}$ . Each address location is associated with two 8-bit words (CY7C1146V18) or 9-bit words (CY7C1157V18) or 18-bit words (CY7C1148V18) or 36-bit words (CY7C1150V18) that burst sequentially into or out of the device.

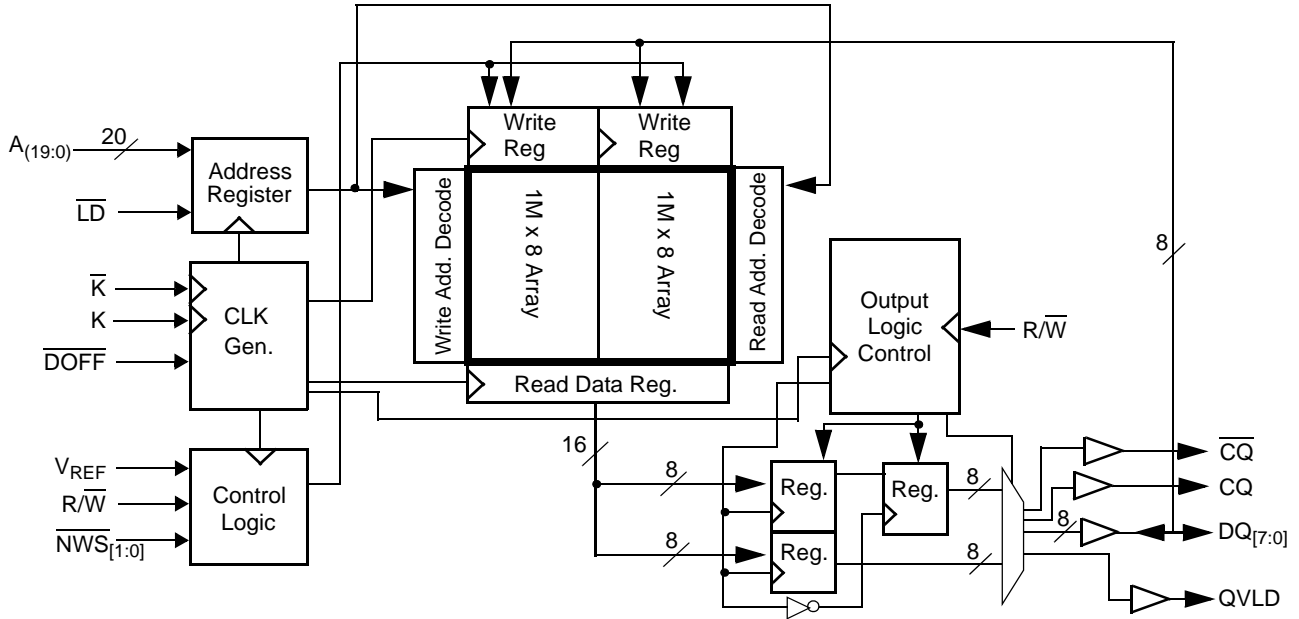
Asynchronous inputs include output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/ $\bar{CQ}$ , eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

All synchronous inputs pass through input registers controlled by the K or  $\bar{K}$  input clocks. All data outputs pass through output registers controlled by the K or  $\bar{K}$  input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

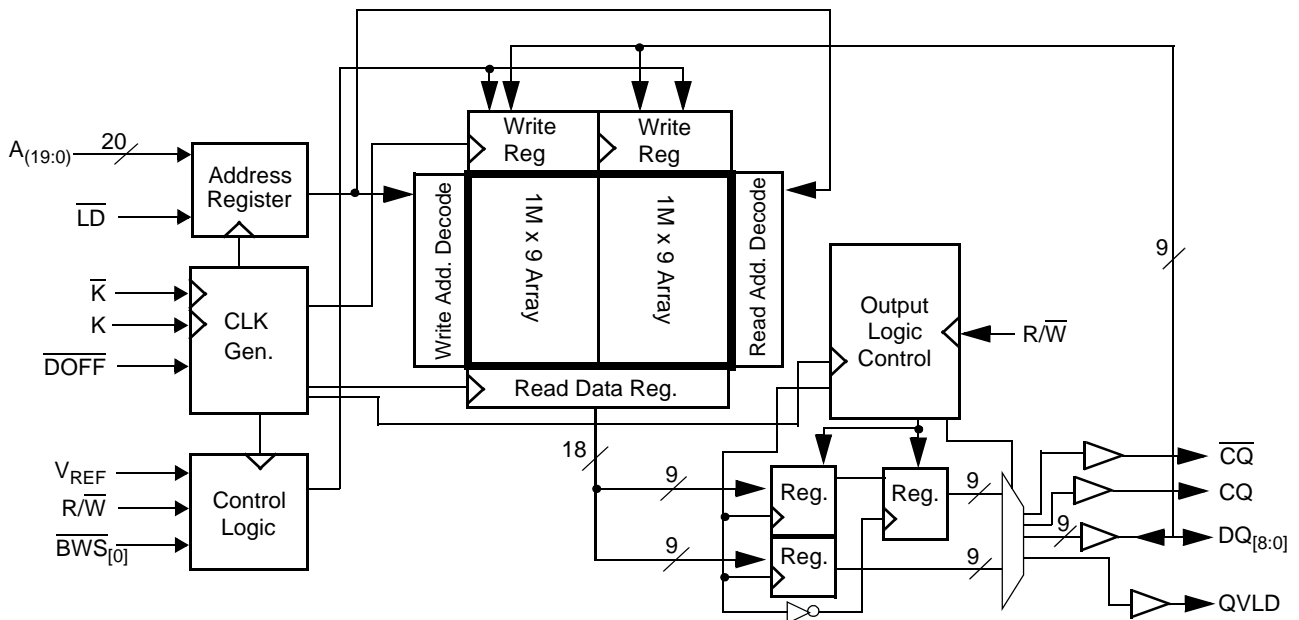
### Note

1. The QDR consortium specification for  $V_{DDQ}$  is  $1.5V \pm 0.1V$ . The Cypress QDR devices exceed the QDR consortium specification and are capable of supporting  $V_{DDQ} = 1.4V$  to  $V_{DD}$ .

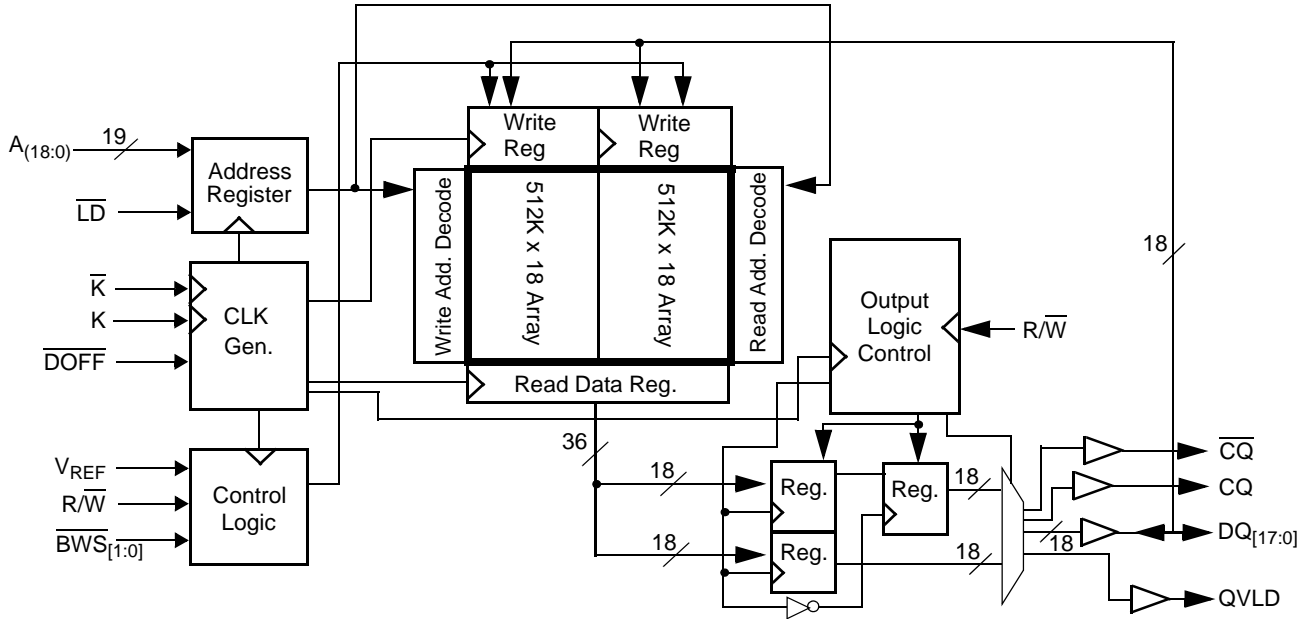
### Logic Block Diagram (CY7C1146V18)



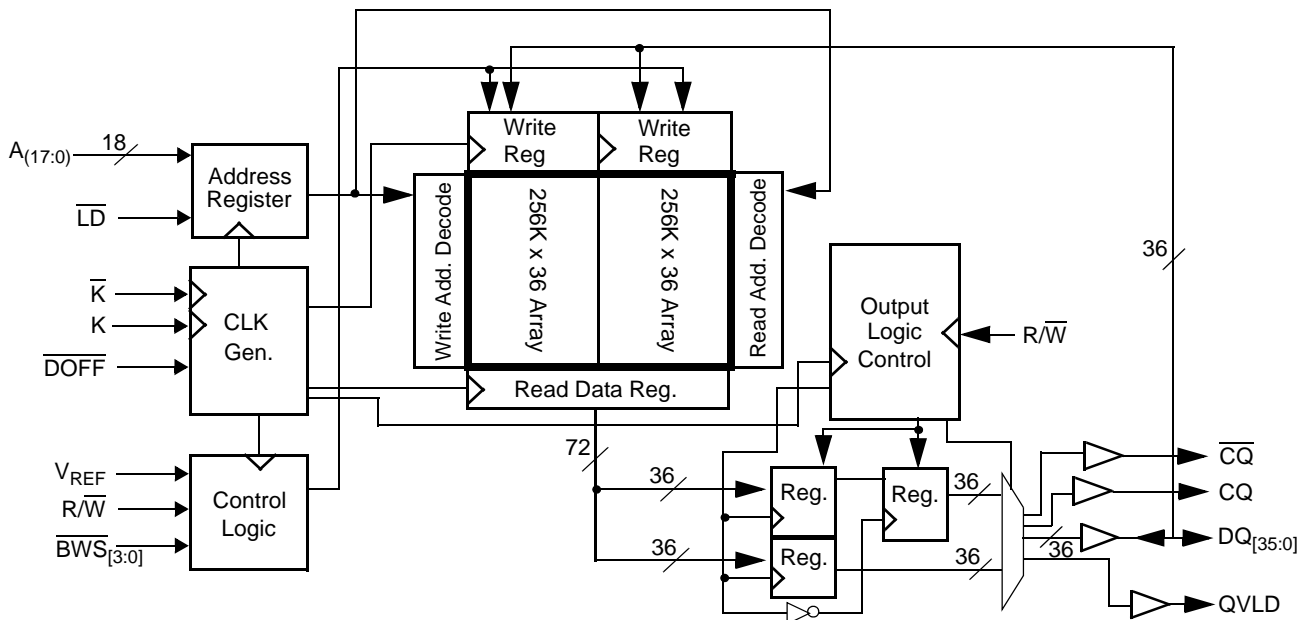
### Logic Block Diagram (CY7C1157V18)



### Logic Block Diagram (CY7C1148V18)



### Logic Block Diagram (CY7C1150V18)



## Pin Configurations

### 165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

#### CY7C1146V18 (2M x 8)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/72M	A	$\overline{\text{R/W}}$	$\overline{\text{NWS}}_1$	$\overline{\text{K}}$	NC/144M	$\overline{\text{LD}}$	A	NC/36M	CQ
<b>B</b>	NC	NC	NC	A	NC/288M	K	$\overline{\text{NWS}}_0$	A	NC	NC	DQ3
<b>C</b>	NC	NC	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>D</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>E</b>	NC	NC	DQ4	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	DQ2
<b>F</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>G</b>	NC	NC	DQ5	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>H</b>	$\overline{\text{DOFF}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQ1	NC
<b>K</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>L</b>	NC	DQ6	NC	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	DQ0
<b>M</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>N</b>	NC	NC	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>P</b>	NC	NC	DQ7	A	A	QVLD	A	A	NC	NC	NC
<b>R</b>	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

#### CY7C1157V18 (2M x 9)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/72M	A	$\overline{\text{R/W}}$	NC	$\overline{\text{K}}$	NC/144M	$\overline{\text{LD}}$	A	NC/36M	CQ
<b>B</b>	NC	NC	NC	A	NC/288M	K	$\overline{\text{BWS}}_0$	A	NC	NC	DQ3
<b>C</b>	NC	NC	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>D</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>E</b>	NC	NC	DQ4	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	DQ2
<b>F</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>G</b>	NC	NC	DQ5	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>H</b>	DOFF	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQ1	NC
<b>K</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>L</b>	NC	DQ6	NC	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	DQ0
<b>M</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>N</b>	NC	NC	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>P</b>	NC	NC	DQ7	A	A	QVLD	A	A	NC	NC	DQ8
<b>R</b>	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

**Pin Configurations** (continued)

**165-Ball FBGA (13 x 15 x 1.4 mm) Pinout**

**CY7C1148V18 (1M x 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/72M	A	$\text{R}/\overline{\text{W}}$	$\overline{\text{BWS}}_1$	$\overline{\text{K}}$	NC/144M	$\overline{\text{LD}}$	A	NC/36M	CQ
<b>B</b>	NC	DQ9	NC	A	NC/288M	K	$\overline{\text{BWS}}_0$	A	NC	NC	DQ8
<b>C</b>	NC	NC	NC	$V_{\text{SS}}$	A	NC	A	$V_{\text{SS}}$	NC	DQ7	NC
<b>D</b>	NC	NC	DQ10	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	NC	NC
<b>E</b>	NC	NC	DQ11	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	NC	DQ6
<b>F</b>	NC	DQ12	NC	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	DQ5
<b>G</b>	NC	NC	DQ13	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	NC
<b>H</b>	$\overline{\text{DOFF}}$	$V_{\text{REF}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{REF}}$	ZQ
<b>J</b>	NC	NC	NC	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	DQ4	NC
<b>K</b>	NC	NC	DQ14	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	DQ3
<b>L</b>	NC	DQ15	NC	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	NC	DQ2
<b>M</b>	NC	NC	NC	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	DQ1	NC
<b>N</b>	NC	NC	DQ16	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	NC	NC	NC
<b>P</b>	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
<b>R</b>	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

**CY7C1150V18 (512K x 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/144M	NC/36M	$\text{R}/\overline{\text{W}}$	$\overline{\text{BWS}}_2$	$\overline{\text{K}}$	$\overline{\text{BWS}}_1$	$\overline{\text{LD}}$	A	NC/72M	CQ
<b>B</b>	NC	DQ27	DQ18	A	$\overline{\text{BWS}}_3$	K	$\overline{\text{BWS}}_0$	A	NC	NC	DQ8
<b>C</b>	NC	NC	DQ28	$V_{\text{SS}}$	A	NC	A	$V_{\text{SS}}$	NC	DQ17	DQ7
<b>D</b>	NC	DQ29	DQ19	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	NC	DQ16
<b>E</b>	NC	NC	DQ20	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	DQ15	DQ6
<b>F</b>	NC	DQ30	DQ21	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	DQ5
<b>G</b>	NC	DQ31	DQ22	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	DQ14
<b>H</b>	$\overline{\text{DOFF}}$	$V_{\text{REF}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{REF}}$	ZQ
<b>J</b>	NC	NC	DQ32	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	DQ13	DQ4
<b>K</b>	NC	NC	DQ23	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	DQ12	DQ3
<b>L</b>	NC	DQ33	DQ24	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	NC	DQ2
<b>M</b>	NC	NC	DQ34	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	DQ11	DQ1
<b>N</b>	NC	DQ35	DQ25	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	NC	NC	DQ10
<b>P</b>	NC	NC	DQ26	A	A	QVLD	A	A	NC	DQ9	DQ0
<b>R</b>	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

## Pin Definitions

Pin Name	IO	Pin Description
DQ <sub>[x:0]</sub>	Input Output-Synchronous	<b>Data Input Output Signals.</b> Inputs are sampled on the rising edge of K and $\bar{K}$ clocks when write operations are valid. These pins drive out the requested data when a read operation is active. Valid data is driven out on the rising edge of both the K and $\bar{K}$ clocks when read operations are active. When read access is deselected, Q <sub>[x:0]</sub> are automatically tri-stated. CY7C1146V18 – DQ <sub>[7:0]</sub> CY7C1157V18 – DQ <sub>[8:0]</sub> CY7C1148V18 – DQ <sub>[17:0]</sub> CY7C1150V18 – DQ <sub>[35:0]</sub>
$\bar{LD}$	Input-Synchronous	<b>Synchronous Load.</b> This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of two data. $\bar{LD}$ must meet the setup and hold times around edge of K.
$\overline{NWS}_0, \overline{NWS}_1,$	Input-Synchronous	<b>Nibble Write Select 0, 1 – Active LOW. (CY7C1146V18 Only)</b> Sampled on the rising edge of the K and $\bar{K}$ clocks when the write operation is active. It is used to select the nibble that is written into the device. $\overline{NWS}_0$ controls D <sub>[3:0]</sub> and $\overline{NWS}_1$ controls D <sub>[7:4]</sub> . All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select causes the corresponding nibble of data to be ignored and not written into the device.
$\overline{BWS}_0, \overline{BWS}_1, \overline{BWS}_2, \overline{BWS}_3$	Input-Synchronous	<b>Byte Write Select 0, 1, 2, and 3 – Active LOW.</b> Sampled on the rising edge of the K and $\bar{K}$ clocks when the Write operation is active. It is used to select the byte that is written into the device when the current portion of the write operation is active. Bytes not written remain unaltered. CY7C1157V18 – $\overline{BWS}_0$ controls D <sub>[8:0]</sub> CY7C1148V18 – $\overline{BWS}_0$ controls D <sub>[8:0]</sub> , and $\overline{BWS}_1$ controls D <sub>[17:9]</sub> CY7C1148V18 – $\overline{BWS}_0$ controls D <sub>[8:0]</sub> , $\overline{BWS}_1$ controls D <sub>[17:9]</sub> , $\overline{BWS}_2$ controls D <sub>[26:18]</sub> , and $\overline{BWS}_3$ controls D <sub>[35:27]</sub> . All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select causes the corresponding byte of data to be ignored and not written into the device.
A	Input-Synchronous	<b>Address Inputs.</b> Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2M x 8 (two arrays each of 1M x 8) for CY7C1146V18, 2M x 9 (two arrays each of 1M x 9) for CY7C1157V18, 1M x 18 (two arrays each of 512K x 18) for CY7C1148V18, and 512K x 36 (two arrays each of 256K x 18) for CY7C1150V18. All the address inputs are ignored when the appropriate port is deselected.
R/ $\bar{W}$	Input-Synchronous	<b>Synchronous Read/Write Input.</b> When $\bar{LD}$ is LOW, this input designates the access type (read when R/ $\bar{W}$ is HIGH, write when R/ $\bar{W}$ is LOW) for loaded address. R/ $\bar{W}$ must meet the setup and hold times around edge of K.
QVLD	Valid Output Indicator	<b>Valid Output Indicator.</b> The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\bar{CQ}$ .
K	Input-Clock	<b>Positive Input Clock Input.</b> The rising edge of K is used to capture synchronous inputs to the device and to drive out data through Q <sub>[x:0]</sub> when in single clock mode. All accesses are initiated on the rising edge of K.
$\bar{K}$	Input-Clock	<b>Negative Input Clock Input.</b> $\bar{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through Q <sub>[x:0]</sub> when in single clock mode.
CQ	Clock Output	<b>Synchronous Echo Clock Outputs.</b> This is a free running clock and is synchronized to the input clock (K) of the DDR-II+. The timings for the echo clocks are shown in the “Switching Characteristics” on page 22.
$\bar{CQ}$	Clock Output	<b>Synchronous Echo Clock Outputs.</b> This is a free running clock and is synchronized to the input clock ( $\bar{K}$ ) of the DDR-II+. The timings for the echo clocks are shown in the “Switching Characteristics” on page 22.
ZQ	Input	<b>Output Impedance Matching Input.</b> This input is used to tune the device outputs to the system data bus impedance. CQ, $\bar{CQ}$ , and Q <sub>[x:0]</sub> output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, connect this pin directly to V <sub>DDQ</sub> , which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

**Pin Definitions** (continued)

Pin Name	IO	Pin Description
DOFF	Input	<b>DLL Turn Off – Active LOW.</b> Connecting this pin to ground turns off the DLL inside the device. The timings in the DLL turned off operation are different from those listed in this data sheet. For normal operation, connect this pin to a pull up through a 10 K $\Omega$ or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, operate the device at a frequency of up to 167 MHz with DDR-I timing.
TDO	Output	<b>TDO for JTAG.</b>
TCK	Input	<b>TCK Pin for JTAG.</b>
TDI	Input	<b>TDI Pin for JTAG.</b>
TMS	Input	<b>TMS Pin for JTAG.</b>
NC	N/A	<b>Not Connected to the Die.</b> Tie to any voltage level.
NC/36M	N/A	<b>Not Connected to the Die.</b> Tie to any voltage level.
NC/72M	N/A	<b>Not Connected to the Die.</b> Tie to any voltage level.
NC/144M	N/A	<b>Not Connected to the Die.</b> Tie to any voltage level.
NC/288M	N/A	<b>Not Connected to the Die.</b> Tie to any voltage level.
V <sub>REF</sub>	Input-Reference	<b>Reference Voltage Input.</b> Static input used to set the reference level for HSTL inputs, Outputs, and AC measurement points.
V <sub>DD</sub>	Power Supply	<b>Power Supply Inputs to the Core of the Device.</b>
V <sub>SS</sub>	Ground	<b>Ground for the Device.</b>
V <sub>DDQ</sub>	Power Supply	<b>Power Supply Inputs for the Outputs of the Device.</b>

## Functional Overview

The CY7C1146V18, CY7C1157V18, CY7C1148V18, and CY7C1150V18 are synchronous pipelined Burst SRAMs equipped with a DDR interface.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input and output timings refer to the rising edge of the Input clocks (K/K).

All synchronous data inputs ( $D_{[x:0]}$ ) pass through input registers controlled by the rising edge of the input clocks (K/K). All synchronous data outputs ( $Q_{[x:0]}$ ) pass through output registers controlled by the rising edge of the input clocks (K/K) as well.

All synchronous control ( $R/\overline{W}$ ,  $\overline{LD}$ ,  $\overline{BWS}_{[0:x]}$ ) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1148V18 is described in the following sections. The same basic descriptions apply to CY7C1146V18, CY7C1157V18, and CY7C1150V18.

### Read Operations

The CY7C1148V18 is organized internally as a single array of 1M x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/W HIGH and LD LOW at the rising edge of the positive input clock (K). The address presented to Address inputs are stored in the read address register. Following the next two K clock rise the corresponding 18-bit word of data from this address location is driven onto the  $Q_{[17:0]}$  using K as the output timing reference. On the subsequent rising edge of K the next 18-bit data word from the address location generated by the burst counter is driven onto the  $Q_{[17:0]}$ . The requested data is valid 0.45 ns from the rising edge of the input clock (K/K). To maintain the internal logic, each read access must be enabled to complete. Initiate read accesses on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C1148V18 first completes the pending read transactions. Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the positive Input clock (K). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

### Write Operations

Write operations are initiated by asserting  $R/\overline{W}$  LOW and  $\overline{LD}$  LOW at the rising edge of the positive input clock (K). The address presented to Address inputs is stored in the write address register. On the following K clock rise the data presented to  $D_{[17:0]}$  is latched and stored into the 18-bit Write Data register provided  $\overline{BWS}_{[1:0]}$  are both asserted active. On the subsequent rising edge of the Negative Input Clock ( $\overline{K}$ ) the information presented to  $D_{[17:0]}$  is also stored into the Write Data register provided  $\overline{BWS}_{[1:0]}$  are both asserted active. The 36 bits of data is then written into the memory array at the specified location. Initiate write accesses on every rising edge of the positive input clock (K). This pipelines the data flow such that 18 bits of data transfers into the device on every rising edge of the input clocks (K and  $\overline{K}$ ).

When write access is deselected, the device ignores all inputs after the pending write operations are completed.

### Byte Write Operations

Byte Write operations are supported by the CY7C1148V18. A write operation is initiated as described in the [Write Operations](#). The bytes that are written are determined by  $\overline{BWS}_0$  and  $\overline{BWS}_1$  which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Select input when the data portion of a write enables the data presented to be latched and written into the device. Deasserting the Byte Write Select input when the data portion of a write enables the data stored in the device for that byte to remain unaltered. Use this feature to simplify read/modify/write operations to a Byte Write operation.

### Double Data Rate Operation

The CY7C1148V18 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. The CY7C1148V18 requires two No Operation (NOP) cycle when transitioning from a read to a write cycle. At higher frequencies, some applications may require a third NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a Posted Write.

If a Read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

### Depth Expansion

Depth expansion requires replicating the  $\overline{LD}$  control signal for each bank. All other control signals can be common between banks as appropriate.

### Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and  $V_{SS}$  to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of  $\pm 15\%$  is between 175 $\Omega$  and 350 $\Omega$ , with  $V_{DDQ} = 1.5V$ . The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

### Echo Clocks

Echo clocks are provided on the DDR-II+ to simplify data capture on high-speed systems. Two echo clocks are generated by the DDR-II+. CQ is referenced with respect to K and  $\overline{CQ}$  is referenced with respect to  $\overline{K}$ . These are free-running clocks and are synchronized to the Input clock of the DDR-II+. The timings for the echo clocks are shown in the ["Switching Characteristics"](#) on page 22.

### Valid Data Indicator (QVLD)

QVLD is provided on the DDR-II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR-II+ device along with Data output. This signal is also edge-aligned with the



echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

**DLL**

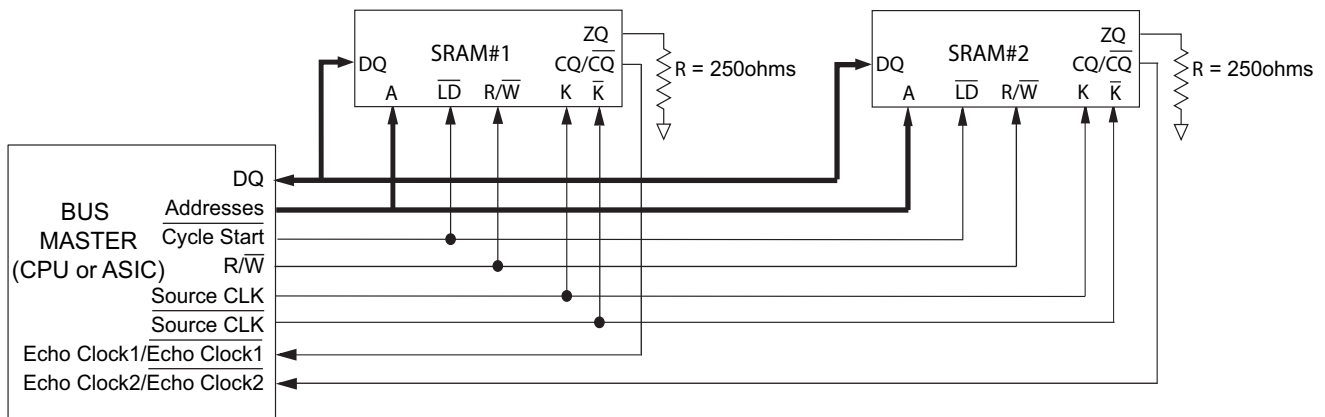
These chips utilize a Delay Lock Loop (DLL) that is designed to function between 120 MHz and the specified maximum clock frequency. The DLL may be disabled by applying ground to the DOFF pin. When the DLL is turned off, the device behaves in

DDR-I mode (with 1.0 cycle latency and a longer access time). For more information, refer to the application note, "DLL Considerations in QDRII/DDRII/QDRII+/DDRII+". The DLL can also be reset by slowing or stopping the input clocks K and  $\bar{K}$  for a minimum of 30 ns. However, it is not necessary for the DLL to be reset in order to lock to the desired frequency. During Power up, when the DOFF is tied HIGH, the DLL gets locked after 2048 cycles of stable clock.

**Application Example**

Figure 1 shows two DDR-II+ used in an application.

**Figure 1. Application Example**



**Truth Table**

The truth table for the CY7C1146V18, CY7C1157V18, CY7C1148V18, and CY7C1150V18 follows. [3, 4, 5, 6, 7, 8]

Operation	K	$\bar{LD}$	$\bar{R/W}$	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on consecutive K and $\bar{K}$ rising edges.	L – H	L	L	D(A) at K (t + 1) $\uparrow$	D(A + 1) at $\bar{K}$ (t + 1) $\uparrow$
Read Cycle: (2.0 cycle latency) Load address; wait two cycle; read data on consecutive K and $\bar{K}$ rising edges.	L – H	L	H	Q(A) at K (t + 2) $\uparrow$	Q(A + 1) at $\bar{K}$ (t + 2) $\uparrow$
NOP: No Operation	L – H	H	X	High-Z	High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

**Notes**

- The above application shows two DDR-II+ used.
- X = "Don't Care," H = Logic HIGH, L = Logic LOW,  $\uparrow$  represents rising edge.
- Device powers up deselected and the outputs in a tri-state condition.
- "A" represents address location latched by the devices when transaction was initiated and A + 1 represents the addresses sequence in the burst.
- "t" represents the cycle at which a Read/Write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the "t" clock cycle.
- Data inputs are registered at K and  $\bar{K}$  rising edges. Data outputs are delivered on K and  $\bar{K}$  rising edges.
- It is recommended that K =  $\bar{K}$  = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

## Write Cycle Descriptions

The write cycle descriptions of CY7C1146V18 and CY7C1148V18 follows. [3, 9]

$\overline{BWS}_0$ / NWS <sub>0</sub>	$\overline{BWS}_1$ / NWS <sub>1</sub>	K	$\overline{K}$	Comments
L	L	L – H	–	When the Data portion of a write sequence is active: CY7C1146V18 – both nibbles (D <sub>[7:0]</sub> ) are written into the device. CY7C1148V18 – both bytes (D <sub>[17:0]</sub> ) are written into the device.
L	L	–	L – H	When the Data portion of a write sequence is active: CY7C1146V18 – both nibbles (D <sub>[7:0]</sub> ) are written into the device. CY7C1148V18 – both bytes (D <sub>[17:0]</sub> ) are written into the device.
L	H	L – H	–	When the Data portion of a write sequence is active: CY7C1146V18 – only the lower nibble (D <sub>[3:0]</sub> ) is written into the device, D <sub>[7:4]</sub> remains unaltered. CY7C1148V18 – only the lower byte (D <sub>[8:0]</sub> ) is written into the device, D <sub>[17:9]</sub> remains unaltered.
L	H	–	L – H	When the Data portion of a write sequence is active: CY7C1146V18 – only the lower nibble (D <sub>[3:0]</sub> ) is written into the device, D <sub>[7:4]</sub> remains unaltered. CY7C1148V18 – only the lower byte (D <sub>[8:0]</sub> ) is written into the device, D <sub>[17:9]</sub> remains unaltered.
H	L	L – H	–	When the Data portion of a write sequence is active: CY7C1146V18 – only the upper nibble (D <sub>[7:4]</sub> ) is written into the device, D <sub>[3:0]</sub> remains unaltered. CY7C1148V18 – only the upper byte (D <sub>[17:9]</sub> ) is written into the device, D <sub>[8:0]</sub> remains unaltered.
H	L	–	L – H	When the Data portion of a write sequence is active: CY7C1146V18 – only the upper nibble (D <sub>[7:4]</sub> ) is written into the device, D <sub>[3:0]</sub> remains unaltered. CY7C1148V18 – only the upper byte (D <sub>[17:9]</sub> ) is written into the device, D <sub>[8:0]</sub> remains unaltered.
H	H	L – H	–	No data is written into the devices when this portion of a write operation is active.
H	H	–	L – H	No data is written into the devices when this portion of a write operation is active.

The write cycle descriptions of CY7C1146V18 follows. [3, 9]

$\overline{BWS}_0$	K	$\overline{K}$	Comments
L	L – H	–	When the Data portion of a write sequence is active, the single byte (D <sub>[8:0]</sub> ) is written into the device.
L	–	L – H	When the Data portion of a write sequence is active, the single byte (D <sub>[8:0]</sub> ) is written into the device.
H	L – H	–	No data is written into the device when this portion of a write operation is active.
H	–	L – H	No data is written into the device when this portion of a write operation is active.

### Note

9. Is based on a Write cycle was initiated in accordance with the Write Cycle Description Truth Table. Alter  $\overline{BWS}_0$ ,  $\overline{BWS}_1$ ,  $\overline{BWS}_2$ , and  $\overline{BWS}_3$  on different portions of a Write cycle, as long as the setup and hold requirements are achieved.

The write cycle descriptions of CY7C1148V18 follows, [3, 9]

$\overline{BWS}_0$	$\overline{BWS}_1$	$\overline{BWS}_2$	$\overline{BWS}_3$	K	$\overline{K}$	Comments
L	L	L	L	L – H	–	When the Data portion of a write sequence is active, all four bytes (D <sub>[35:0]</sub> ) are written into the device.
L	L	L	L	–	L – H	When the Data portion of a write sequence is active, all four bytes (D <sub>[35:0]</sub> ) are written into the device.
L	H	H	H	L – H	–	When the Data portion of a write sequence is active, only the lower byte (D <sub>[8:0]</sub> ) is written into the device. D <sub>[35:9]</sub> remains unaltered.
L	H	H	H	–	L – H	When the Data portion of a write sequence is active, only the lower byte (D <sub>[8:0]</sub> ) is written into the device. D <sub>[35:9]</sub> remains unaltered.
H	L	H	H	L – H	–	When the Data portion of a write sequence is active, only the byte (D <sub>[17:9]</sub> ) is written into the device. D <sub>[8:0]</sub> and D <sub>[35:18]</sub> remains unaltered.
H	L	H	H	–	L – H	When the Data portion of a write sequence is active, only the byte (D <sub>[17:9]</sub> ) is written into the device. D <sub>[8:0]</sub> and D <sub>[35:18]</sub> remains unaltered.
H	H	L	H	L – H	–	When the Data portion of a write sequence is active, only the byte (D <sub>[26:18]</sub> ) is written into the device. D <sub>[17:0]</sub> and D <sub>[35:27]</sub> remains unaltered.
H	H	L	H	–	L – H	When the Data portion of a Write sequence is active, only the byte (D <sub>[26:18]</sub> ) is written into the device. D <sub>[17:0]</sub> and D <sub>[35:27]</sub> remains unaltered.
H	H	H	L	L – H	–	When the Data portion of a write sequence is active, only the byte (D <sub>[35:27]</sub> ) is written into the device. D <sub>[26:0]</sub> remains unaltered.
H	H	H	L	–	L – H	When the Data portion of a write sequence is active, only the byte (D <sub>[35:27]</sub> ) is written into the device. D <sub>[26:0]</sub> remains unaltered.
H	H	H	H	L – H	–	No data is written into the device when this portion of a write operation is active.
H	H	H	H	–	L – H	No data is written into the device when this portion of a write operation is active.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard 1149.1-2001. The TAP operates using JEDEC standard 1.8V IO logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

### Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and connect to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For more information on loading the instruction register, see the “TAP Controller State Diagram” on page 14. TDI is internally pulled up and unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSb) on any register.

### Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Select only one register at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### Instruction Register

Serially load three-bit instructions into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in “TAP Controller Block Diagram” on page 15. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

#### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. Use the EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions to capture the contents of the Input and Output ring.

The “Boundary Scan Order” on page 18 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSb of the register is connected to TDI, and the LSb is connected to TDO.

#### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the “Identification Register Definitions” on page 17.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail in the following section.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. When this state is active, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is supplied a test logic reset state.

### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is supplied when the Update IR state is active.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that when the Capture-DR state is active, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required — that is, while data captured is shifted out, shift in the preloaded data.

### BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

#### EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit 47. When this scan cell, called the "extest output bus tri-state", is latched into the preload register the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

Set this bit by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, when the Shift-DR state is active. When the Update-DR is active, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

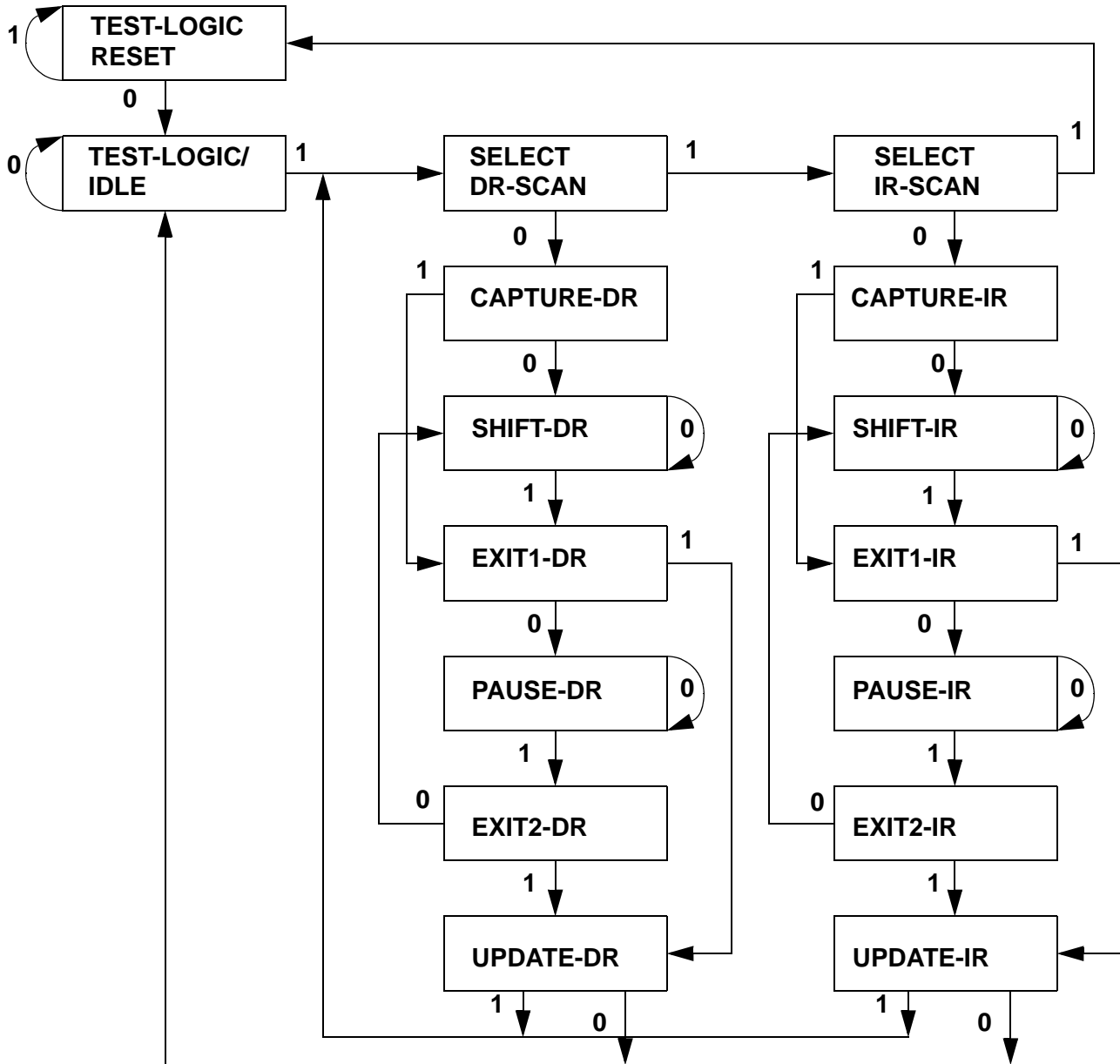
#### Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

Figure 2 shows the tap controller state diagram. [10]

Figure 2. Tap Controller State Diagram

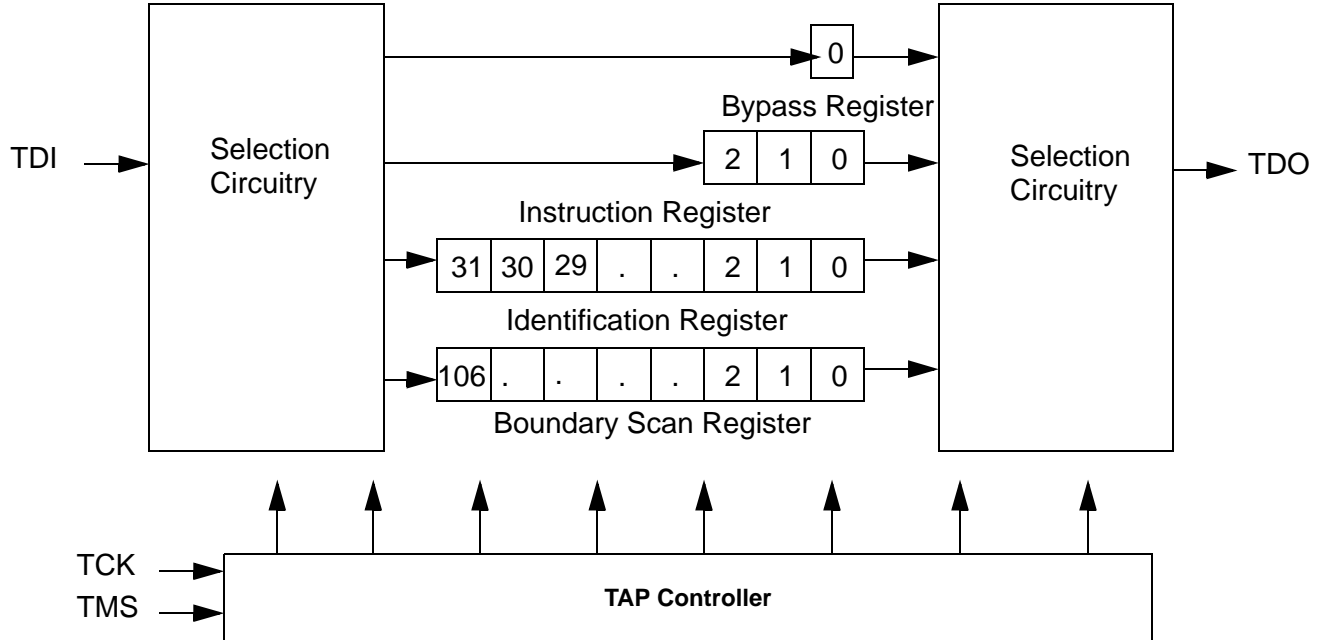


**Note**

10. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

## TAP Controller Block Diagram

Figure 3. Tap Controller Block Diagram



## TAP Electrical Characteristics

The Tap Electrical Characteristics table over the operating range follows. [11, 12, 13]

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2.0 mA	1.4		V
V <sub>OH2</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA	1.6		V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>OL2</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		0.65 V <sub>DD</sub>	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.35 V <sub>DD</sub>	V
I <sub>X</sub>	Input and Output Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	-5	5	μA

### Notes

11. These characteristics pertain to the TAP inputs (TMS, TCK, TDI, and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
12. Overshoot: V<sub>IH(AC)</sub> ≤ V<sub>DDQ</sub> + 0.35V (Pulse width less than t<sub>CYC/2</sub>), Undershoot: V<sub>IL(AC)</sub> ≥ -0.3V (Pulse width less than t<sub>CYC/2</sub>).
13. All voltage referenced to ground.

## TAP AC Switching Characteristics

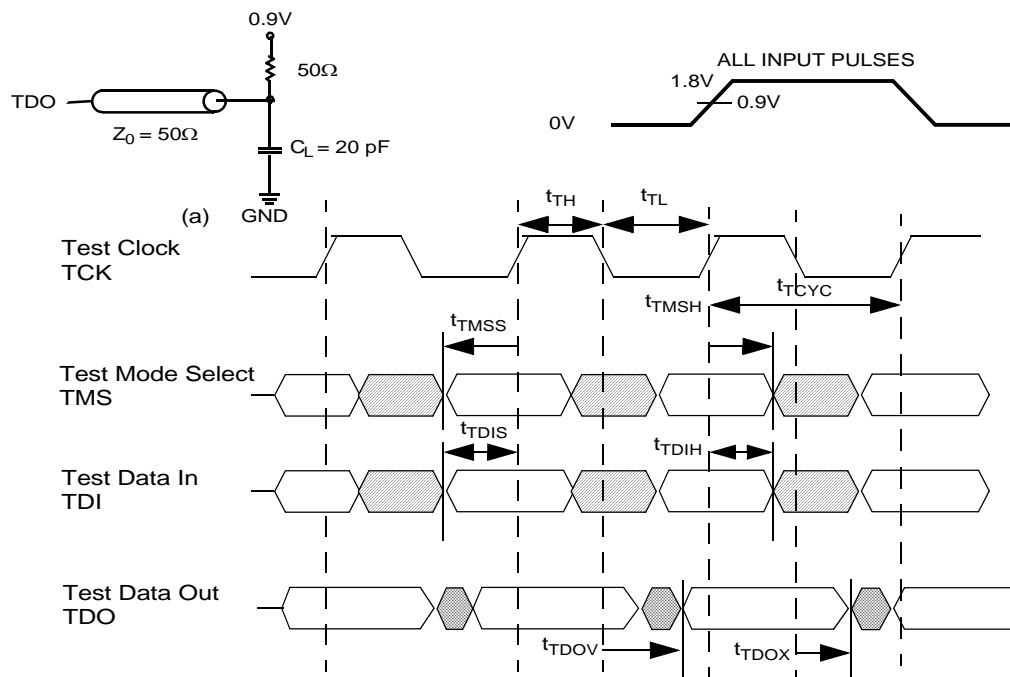
The Tap AC Switching Characteristics table over the operating range follows. [14, 15]

Parameter	Description	Min	Max	Unit
$t_{TCYC}$	TCK Clock Cycle Time	50		ns
$t_{TF}$	TCK Clock Frequency		20	MHz
$t_{TH}$	TCK Clock HIGH	20		ns
$t_{TL}$	TCK Clock LOW	20		ns
<b>Setup Times</b>				
$t_{TMSS}$	TMS Setup to TCK Clock Rise	5		ns
$t_{TDIS}$	TDI Setup to TCK Clock Rise	5		ns
$t_{CS}$	Capture Setup to TCK Rise	5		ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK Clock Rise	5		ns
$t_{TDIH}$	TDI Hold after Clock Rise	5		ns
$t_{CH}$	Capture Hold after Clock Rise	5		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		10	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns

## TAP Timing and Test Condition

The Tap Timing and Test Conditions for the CY7C1146V18, CY7C1157V18, CY7C1148V18, and CY7C1150V18 follows. [15]

Figure 4. TAP Timing and Test Conditions



### Notes

- $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.
- Test conditions are specified using the load in TAP AC test conditions.  $t_R/t_F = 1$  ns



### Identification Register Definitions

Instruction Field	Value				Description
	CY7C1146V18	CY7C1157V18	CY7C1148V18	CY7C1150V18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010111100000101	11010111100001101	11010111100010101	11010111100100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

### Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

### Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the Input Output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

**Boundary Scan Order**

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J

Bit #	Bump ID
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	Internal
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A

Bit #	Bump ID
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	1H
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F

Bit #	Bump ID
81	3G
82	2G
83	1J
84	2J
85	3K
86	3J
87	2K
88	1K
89	2L
90	3L
91	1M
92	1L
93	3N
94	3M
95	1N
96	2M
97	3P
98	2N
99	2P
100	1P
101	3R
102	4R
103	4P
104	5P
105	5N
106	5R

### Power Up Sequence in DDR-II+ SRAM

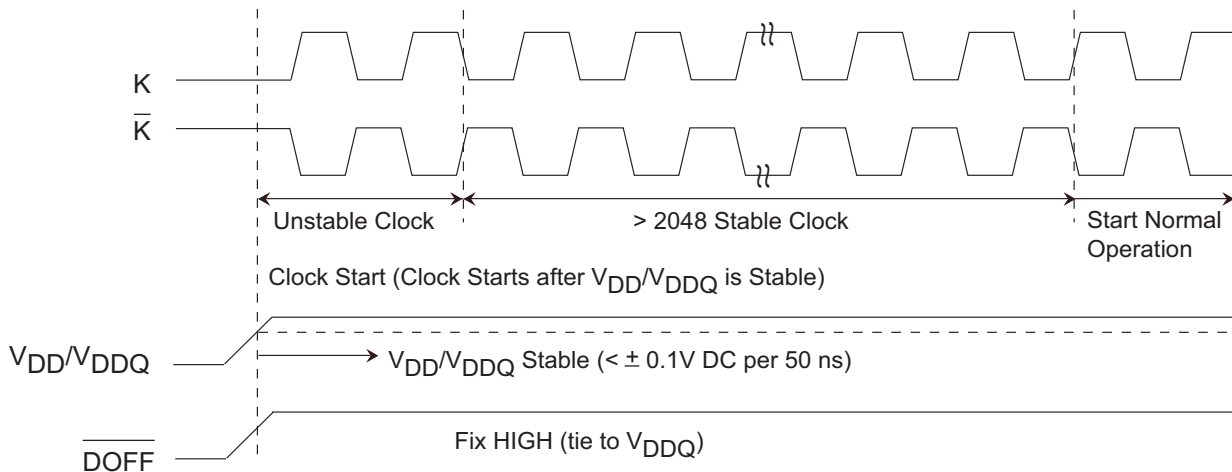
During Power Up, when the  $\overline{\text{DOFF}}$  is tied HIGH, the DLL gets locked after 2048 cycles of stable clock. DDR-II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

### Power Up Sequence

- Apply power with  $\overline{\text{DOFF}}$  tied HIGH (All other inputs can be HIGH or LOW)
  - Apply  $V_{\text{DD}}$  before  $V_{\text{DDQ}}$
  - Apply  $V_{\text{DDQ}}$  before  $V_{\text{REF}}$  or at the same time as  $V_{\text{REF}}$
- Provide stable power and clock (K,  $\overline{\text{K}}$ ) for 2048 cycles to lock the DLL.

### Power Up Waveforms

Figure 5. Power Up Waveforms



### DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as  $t_{\text{KC Var}}$
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 2048 cycles stable clock to relock to the desired clock frequency.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C  
 Ambient Temperature with Power Applied -55°C to + 125°C  
 Supply Voltage on V<sub>DD</sub> Relative to GND ..... -0.5V to + 2.9V  
 Supply Voltage on V<sub>DDQ</sub> Relative to GND ..... -0.5V to + V<sub>DD</sub>  
 DC Applied to Outputs in High-Z ..... -0.5V to V<sub>DDQ</sub> + 0.3V  
 DC Input Voltage<sup>[12]</sup> ..... -0.5V to V<sub>DD</sub> + 0.3V

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage (MIL-STD-883, M 3015).... >2001V  
 Latch up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub> <sup>[16]</sup>	V <sub>DDQ</sub> <sup>[16]</sup>
Commercial	0°C to +70°C	1.8 ± 0.1V	1.4V to V <sub>DD</sub>
Industrial	-40°C to +85°C		

## Electrical Characteristics

The DC Electrical Characteristics over the operating range follows. <sup>[13]</sup>

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Power Supply Voltage		1.7	1.8	1.9	V
V <sub>DDQ</sub>	IO Supply Voltage		1.4	1.5	V <sub>DD</sub>	V
V <sub>OH</sub>	Output HIGH Voltage	Note 17	V <sub>DDQ</sub> /2 - 0.12		V <sub>DDQ</sub> /2 + 0.12	V
V <sub>OL</sub>	Output LOW Voltage	Note 18	V <sub>DDQ</sub> /2 - 0.12		V <sub>DDQ</sub> /2 + 0.12	V
V <sub>OH(LOW)</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, Nominal Impedance	V <sub>DDQ</sub> - 0.2		V <sub>DDQ</sub>	V
V <sub>OL(LOW)</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, Nominal Impedance	V <sub>SS</sub>		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>REF</sub> + 0.1		V <sub>DDQ</sub> + 0.15	V
V <sub>IL</sub>	Input LOW Voltage		-0.15		V <sub>REF</sub> - 0.1	V
I <sub>X</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-2		2	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-2		2	μA
V <sub>REF</sub>	Input Reference Voltage <sup>[19]</sup>	Typical Value = 0.75V	0.68	0.75	0.95	V
I <sub>DD</sub> <sup>[20]</sup>	V <sub>DD</sub> Operating Supply	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>max</sub> = 1/t <sub>CYC</sub>	300 MHz		850	mA
			333 MHz		920	mA
			375 MHz		1020	mA
I <sub>SB1</sub>	Automatic Power Down Current	Max V <sub>DD</sub> , Both Ports Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> f = f <sub>max</sub> = 1/t <sub>CYC</sub> , Inputs Static	300 MHz		250	mA
			333 MHz		260	mA
			375 MHz		290	mA

## AC Input Requirements

Over the operating range<sup>[12]</sup>

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage		V <sub>REF</sub> + 0.2	-	V <sub>DDQ</sub> + 0.24	V
V <sub>IL</sub>	Input LOW Voltage		-0.24	-	V <sub>REF</sub> - 0.2	V

### Notes

16. Power up: I<sub>S</sub> based on a linear ramp from 0V to V<sub>DD(min)</sub> within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.
17. Outputs are impedance controlled. I<sub>OH</sub> = -(V<sub>DDQ</sub>/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
18. Outputs are impedance controlled. I<sub>OL</sub> = (V<sub>DDQ</sub>/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
19. V<sub>REF</sub> (min) = 0.68V or 0.46 V<sub>DDQ</sub>, whichever is larger, V<sub>REF</sub> (max) = 0.95V or 0.54 V<sub>DDQ</sub>, whichever is smaller.
20. The operation current is calculated with 50% read cycle and 50% write cycle.

## Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 1.8\text{V}$ $V_{DDQ} = 1.5\text{V}$	5	pF
$C_{CLK}$	Clock Input Capacitance		6	pF
$C_O$	Output Capacitance		7	pF

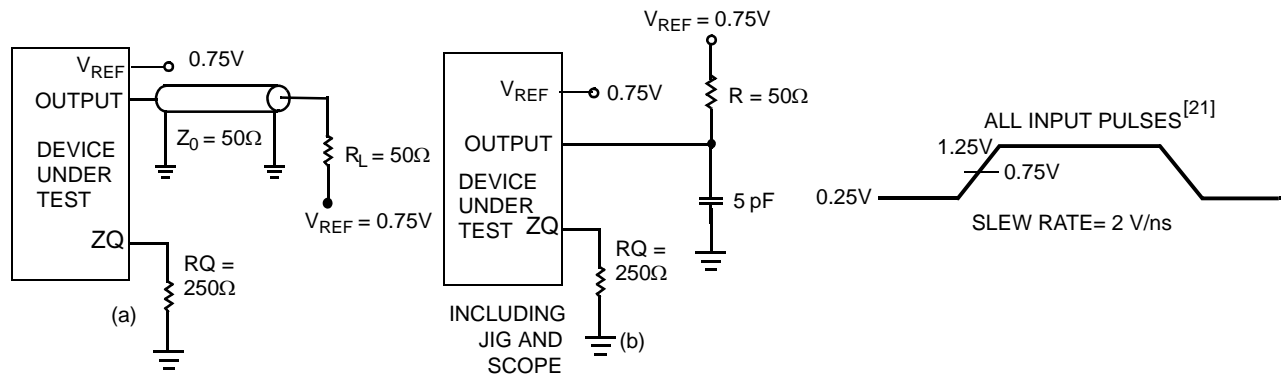
## Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
$\Theta_{JA}$	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	17.2	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (junction to case)		4.15	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 6. AC Test loads and Waveforms



### Note

21. Unless otherwise noted, test conditions are based upon a signal transition time of 2V/ns, timing reference levels of 0.75V,  $V_{REF} = 0.75\text{V}$ ,  $R_Q = 250\Omega$ ,  $V_{DDQ} = 1.5\text{V}$ , input pulse levels of 0.25V to 1.25V, and output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance shown in (a) of AC Test Loads.

## Switching Characteristics

Over the operating range [21, 22]

Cypress Parameter	Consortium Parameter	Description	375 MHz		333 MHz		300 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>POWER</sub>		V <sub>DD</sub> (Typical) to the first Access <sup>[23]</sup>	1	–	1	–	1	–	ms
t <sub>CYC</sub>	t <sub>KHKH</sub>	K Clock Cycle Time	2.66	8.40	3.0	8.40	3.3	8.40	ns
t <sub>KH</sub>	t <sub>KHKL</sub>	Input Clock (K/ $\bar{K}$ ) HIGH	0.425	–	0.425	–	0.425	–	t <sub>CYC</sub>
t <sub>KL</sub>	t <sub>KLKH</sub>	Input Clock (K/ $\bar{K}$ ) LOW	0.425	–	0.425	–	0.425	–	t <sub>CYC</sub>
t <sub>KH<math>\bar{K}</math>H</sub>	t <sub>KH<math>\bar{K}</math>H</sub>	K Clock Rise to $\bar{K}$ Clock Rise (rising edge to rising edge)	1.13	–	1.28	–	1.40	–	ns
<b>Setup Times</b>									
t <sub>SA</sub>	t <sub>AVKH</sub>	Address Setup to K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t <sub>SC</sub>	t <sub>IVKH</sub>	Control Setup to K Clock Rise ( $\overline{LD}$ , $\overline{R/W}$ )	0.4	–	0.4	–	0.4	–	ns
t <sub>SCDDR</sub>	t <sub>IVKH</sub>	Double Data Rate Control Setup to Clock (K/ $\bar{K}$ ) Rise ( $\overline{BWS}_0$ , $\overline{BWS}_1$ , $\overline{BWS}_2$ , $\overline{BWS}_3$ )	0.28	–	0.28	–	0.28	–	ns
t <sub>SD</sub>	t <sub>DVKH</sub>	D <sub>[X:0]</sub> Setup to Clock (K/ $\bar{K}$ ) Rise	0.28	–	0.28	–	0.28	–	ns
<b>Hold Times</b>									
t <sub>HA</sub>	t <sub>KHAX</sub>	Address Hold after K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t <sub>HC</sub>	t <sub>KHIX</sub>	Control Hold after K Clock Rise ( $\overline{LD}$ , $\overline{R/W}$ )	0.4	–	0.4	–	0.4	–	ns
t <sub>HCDDR</sub>	t <sub>KHIX</sub>	Double Data Rate Control Hold after Clock (K/ $\bar{K}$ ) Rise ( $\overline{BWS}_0$ , $\overline{BWS}_1$ , $\overline{BWS}_2$ , $\overline{BWS}_3$ )	0.28	–	0.28	–	0.28	–	ns
t <sub>HD</sub>	t <sub>KHDX</sub>	D <sub>[X:0]</sub> Hold after Clock (K/ $\bar{K}$ ) Rise	0.28	–	0.28	–	0.28	–	ns
<b>Output Times</b>									
t <sub>CO</sub>	t <sub>CHQV</sub>	K/ $\bar{K}$ Clock Rise to Data Valid	–	0.45	–	0.45	–	0.45	ns
t <sub>DOH</sub>	t <sub>CHQX</sub>	Data Output Hold after K/ $\bar{K}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	ns
t <sub>CCQO</sub>	t <sub>CHCQV</sub>	K/ $\bar{K}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	ns
t <sub>CQOH</sub>	t <sub>CHCQX</sub>	Echo Clock Hold after K/ $\bar{K}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	ns
t <sub>CQD</sub>	t <sub>CQHCV</sub>	Echo Clock High to Data Valid	–	0.2	–	0.2	–	0.2	ns
t <sub>CQDOH</sub>	t <sub>CQHCV</sub>	Echo Clock High to Data Invalid	–0.2	–	–0.2	–	–0.2	–	ns
t <sub>CQH</sub>	t <sub>CQHCQL</sub>	Output Clock (CQ/ $\bar{CQ}$ ) HIGH <sup>[24]</sup>	0.88	–	1.03	–	1.15	–	ns
t <sub>CQH<math>\bar{CQ}</math>H</sub>	t <sub>CQH<math>\bar{CQ}</math>H</sub>	CQ Clock Rise to $\bar{CQ}$ Clock Rise <sup>[24]</sup> (rising edge to rising edge)	0.88	–	1.03	–	1.15	–	ns
t <sub>CHZ</sub>	t <sub>CHQZ</sub>	Clock (K/ $\bar{K}$ ) Rise to High-Z (Active to High-Z) <sup>[25, 26]</sup>	–	0.45	–	0.45	–	0.45	ns
t <sub>CLZ</sub>	t <sub>CHQX1</sub>	Clock (K/ $\bar{K}$ ) Rise to Low-Z <sup>[25, 26]</sup>	–0.45	–	–0.45	–	–0.45	–	ns
t <sub>QVLD</sub>	t <sub>QVLD</sub>	Echo Clock High to QVLD Valid <sup>[27]</sup>	–0.20	0.20	–0.20	0.20	–0.20	0.20	ns
<b>DLL Timing</b>									
t <sub>KC Var</sub>	t <sub>KC Var</sub>	Clock Phase Jitter	–	0.20	–	0.20	–	0.20	ns
t <sub>KC lock</sub>	t <sub>KC lock</sub>	DLL Lock Time (K)	2048	–	2048	–	2048	–	Cycles
t <sub>KC Reset</sub>	t <sub>KC Reset</sub>	K Static to DLL Reset <sup>[28]</sup>	30	–	30	–	30	–	ns

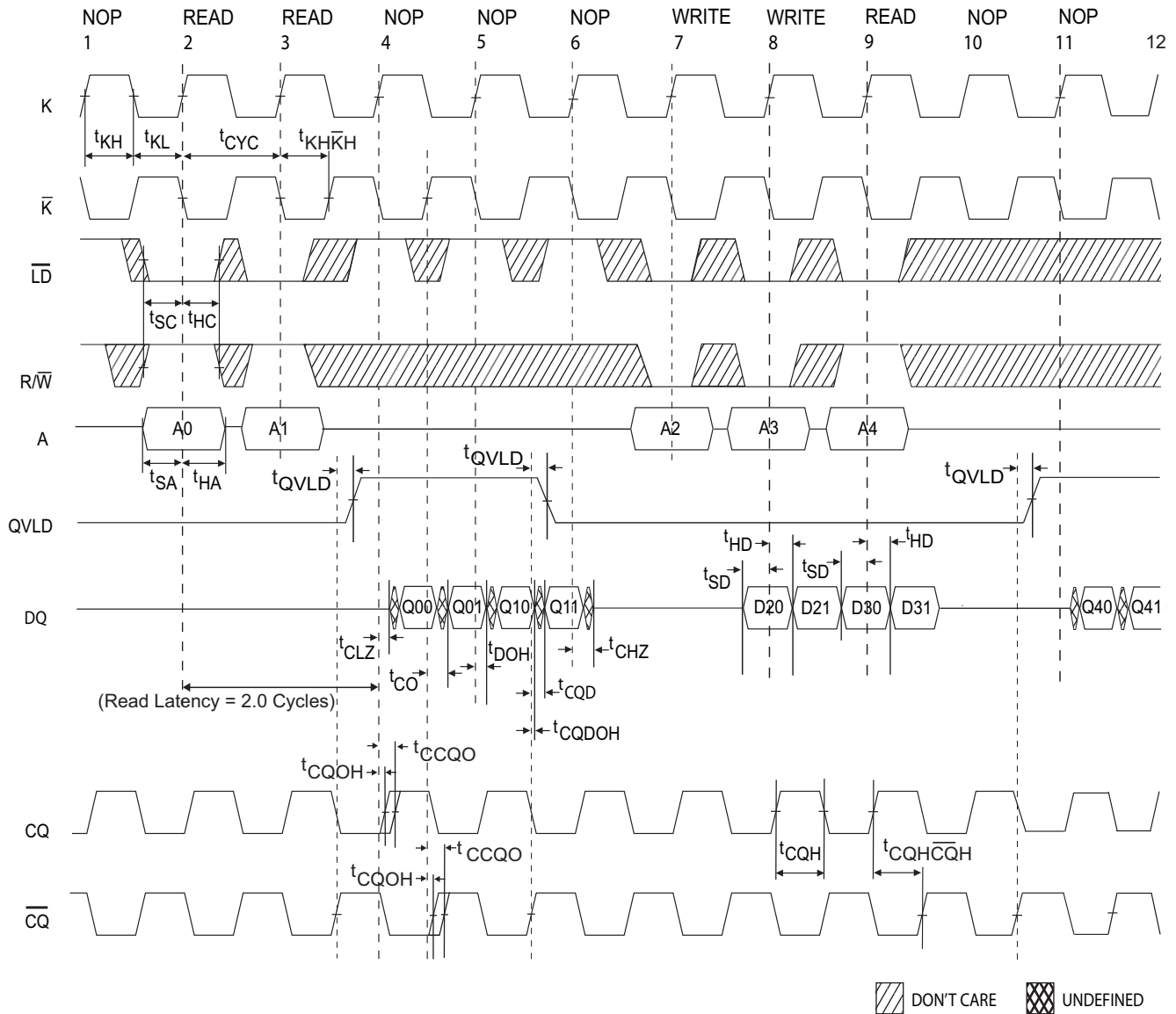
### Notes

22. When a part with a maximum frequency above 300 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
23. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD</sub> minimum initially before a read or write operation can be initiated.
24. These parameters are extrapolated from the input timing parameters (t<sub>KH $\bar{K}$ H</sub> – 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps (t<sub>KC Var</sub>) is already included in the t<sub>KH $\bar{K}$ H</sub>). These parameters are only guaranteed by design and are not tested in production.
25. t<sub>CHZ</sub>, t<sub>CLZ</sub>, are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm$  100 mV from steady-state voltage.
26. At any voltage and temperature t<sub>CHZ</sub> is less than t<sub>CLZ</sub> and t<sub>CHZ</sub> less than t<sub>CO</sub>.
27. t<sub>QVLD</sub> spec is applicable for both rising and falling edges of QVLD signal.
28. Hold to >V<sub>IH</sub> or <V<sub>IL</sub>.

## Switching Waveforms

### Read/Write/Deselect Sequence

Figure 7. Waveform for 2.0 Cycle Read Latency<sup>[29, 30, 31]</sup>



#### Notes

29. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1.

30. Outputs are disabled (High-Z) one clock cycle after a NOP.

31. The third NOP cycle between Read to Write transition is not necessary for correct device operation when Read Latency = 2.0 cycles; however at high frequency operation, it may be required to avoid bus contention.

## Ordering Information

Not all of the speed, package and temperature ranges are available. Contact your local sales representative or visit [www.cypress.com](http://www.cypress.com) for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
375	CY7C1146V18-375BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1157V18-375BZC			
	CY7C1148V18-375BZC			
	CY7C1150V18-375BZC			
	CY7C1146V18-375BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-375BZXC			
	CY7C1148V18-375BZXC			
	CY7C1150V18-375BZXC			
	CY7C1146V18-375BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1157V18-375BZI			
	CY7C1148V18-375BZI			
	CY7C1150V18-375BZI			
	CY7C1146V18-375BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-375BZXI			
	CY7C1148V18-375BZXI			
	CY7C1150V18-375BZXI			
333	CY7C1146V18-333BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1157V18-333BZC			
	CY7C1148V18-333BZC			
	CY7C1150V18-333BZC			
	CY7C1146V18-333BZXC	51-85180	165-Vall Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-333BZXC			
	CY7C1148V18-333BZXC			
	CY7C1150V18-333BZXC			
	CY7C1146V18-333BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1157V18-333BZI			
	CY7C1148V18-333BZI			
	CY7C1150V18-333BZI			
	CY7C1146V18-333BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-333BZXI			
	CY7C1148V18-333BZXI			
	CY7C1150V18-333BZXI			



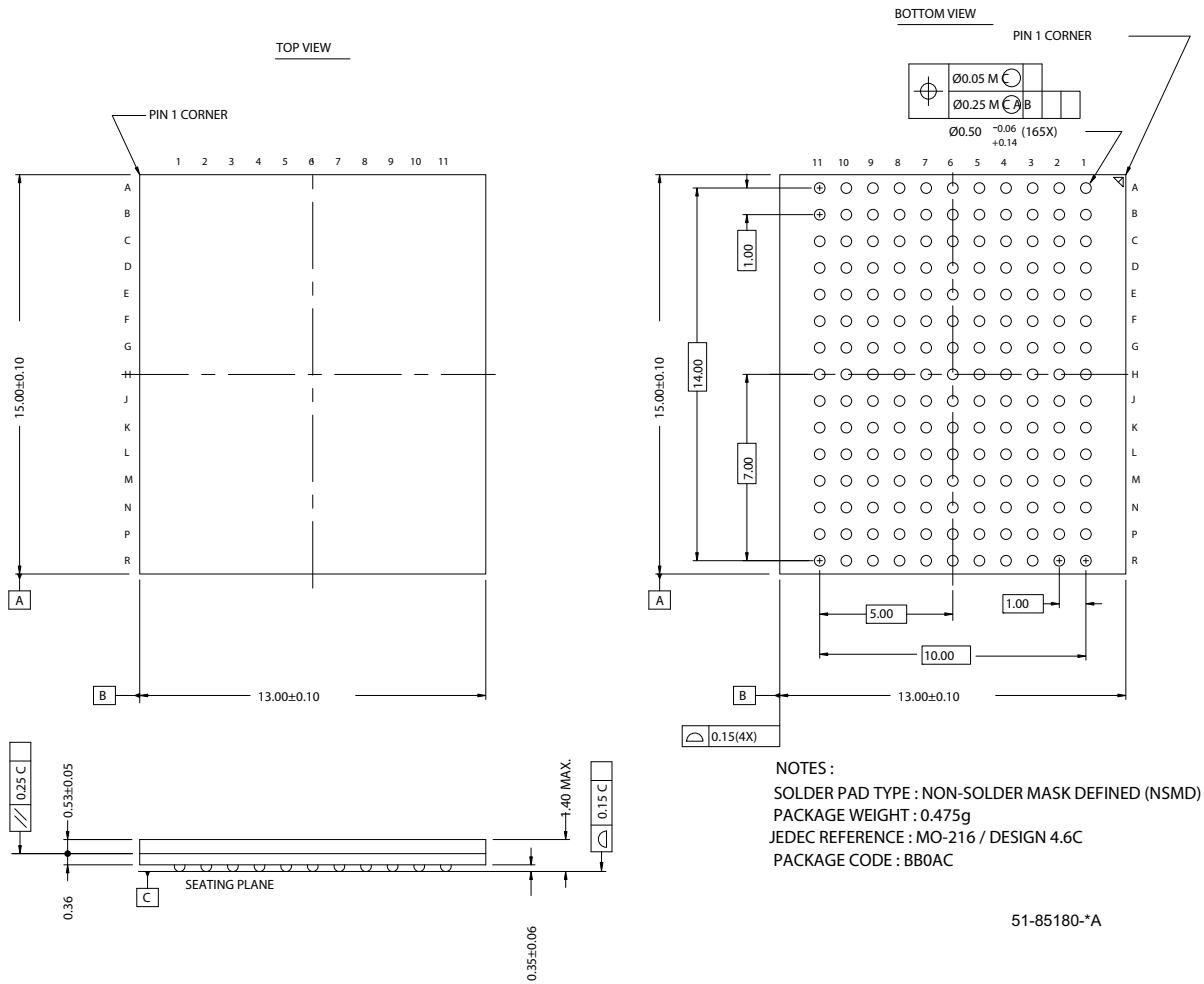
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Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
300	CY7C1146V18-300BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1157V18-300BZC			
	CY7C1148V18-300BZC			
	CY7C1150V18-300BZC			
	CY7C1146V18-300BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-300BZXC			
	CY7C1148V18-300BZXC			
	CY7C1150V18-300BZXC			
300	CY7C1146V18-300BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1157V18-300BZI			
	CY7C1148V18-300BZI			
	CY7C1150V18-300BZI			
	CY7C1146V18-300BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1157V18-300BZXI			
	CY7C1148V18-300BZXI			
	CY7C1150V18-300BZXI			

**Package Diagram**

**Figure 8. 165-Ball FBGA (13 x 15 x 1.4 mm), 51-85180**



## Document History Page

Document Title: CY7C1146V18/CY7C1157V18/CY7C1148V18/CY7C1150V18, 18-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) Document Number: 001-06621				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	430351	See ECN	NXR	New data sheet
*A	461654	See ECN	NXR	Revised the MPNs from CY7C1157BV18 to CY7C1146V18 CY7C1148BV18 to CY7C1157V18 CY7C1150BV18 to CY7C1148V18 Changed $t_{TH}$ and $t_{TL}$ from 40 ns to 20 ns, changed $t_{TMSS}$ , $t_{TDIS}$ , $t_{CS}$ , $t_{TMSH}$ , $t_{TDIH}$ , $t_{CH}$ from 10 ns to 5 ns and changed $t_{TDOV}$ from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power Up waveform
*B	497629	See ECN	NXR	Changed the $V_{DDQ}$ operating voltage to 1.4V to $V_{DD}$ in the Features section, in Operating Range table and in the DC Electrical Characteristics table Added foot note in page 1 Changed the Maximum rating of Ambient Temperature with Power Applied from $-10^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ to $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ Changed $V_{REF}$ (max) spec from 0.85V to 0.95V in the DC Electrical Characteristics table and in the note below the table Updated note 21 to specify Overshoot and Undershoot Spec Updated $\Theta_{JA}$ and $\Theta_{JC}$ values Removed x9 part and its related information Updated foot note 24
*C	1175245	See ECN	VKN/KKVTMP	Converted from preliminary to final Added x8 and x9 parts Updated logic block diagram for x18 and x36 parts Changed $I_{DD}$ values from 794 mA to 1020 mA for 375 MHz, 733 mA to 920 mA for 333 MHz, 685 mA to 850 mA for 300 MHz Changed $I_{SB}$ values from 227 mA to 290 mA for 375 MHz, 212 mA to 260 mA for 333 MHz, 201 mA to 250 mA for 300 MHz Changed $t_{CYC(max)}$ spec to 8.4 ns for all speed bins Changed $\Theta_{JA}$ value from 13.48 $^{\circ}\text{C}/\text{W}$ to 17.2 $^{\circ}\text{C}/\text{W}$ Updated Ordering Information table
*D	2199066	See ECN	VKN/AESA	Added footnote# 20 related to $I_{DD}$

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