# CY7C1034DV33

## 6-Mbit (256K X 24) Static RAM

## Features

- High speed
  - $t_{AA}$ = 10 ns
- Low active power
  - $I_{CC}$ = 175 mA at 10 ns
- Low CMOS standby power
  - $I_{SB2}$ = 25 mA
- Operating voltages of 3.3 ± 0.3V
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$ features
- Available in Pb-free standard 119-Ball PBGA

## Functional Description

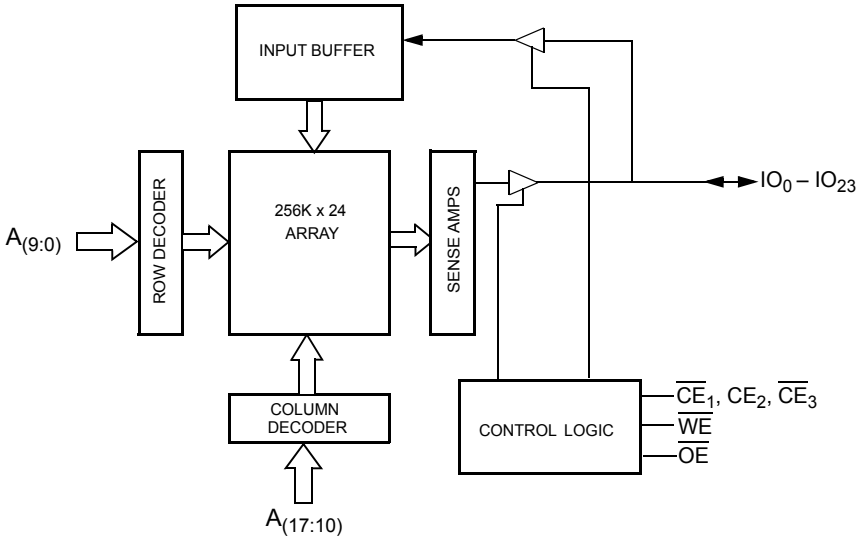
The CY7C1034DV33 is a high performance CMOS static RAM organized as 256K words by 24 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

To write to the device, enable the chip ($\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{CE}_3$ LOW) while forcing the Write Enable ($\overline{WE}$) input LOW.

To read from the device, enable the chip by taking $\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{CE}_3$ LOW, while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. See the Truth Table on page 7 for a complete description of Read and Write modes.

The 24 IO pins ($IO_0$ to $IO_{23}$) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH, $CE_2$ LOW, or $\overline{CE}_3$ HIGH) or when the output enable ($\overline{OE}$) is HIGH during a write operation. ($\overline{CE}_1$ LOW, $CE_2$ HIGH, $\overline{CE}_3$ LOW, and $\overline{WE}$ LOW).

## Logic Block Diagram



## Selection Guide

| Description | –10 | Unit |
|---|---|---|
| Maximum Access Time | 10 | ns |
| Maximum Operating Current | 175 | mA |
| Maximum CMOS Standby Current | 25 | mA |

## Pin Configuration

**Figure 1. 119-Ball PBGA Top View** [1]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | NC | A | A | A | A | A | NC |
| **B** | NC | A | A | $\overline{CE}_1$ | A | A | NC |
| **C** | $IO_{12}$ | NC | $CE_2$ | A | $\overline{CE}_3$ | NC | $IO_0$ |
| **D** | $IO_{13}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_1$ |
| **E** | $IO_{14}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $IO_2$ |
| **F** | $IO_{15}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_3$ |
| **G** | $IO_{16}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $IO_4$ |
| **H** | $IO_{17}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_5$ |
| **J** | NC | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | NC |
| **K** | $IO_{18}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_6$ |
| **L** | $IO_{19}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $IO_7$ |
| **M** | $IO_{20}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_8$ |
| **N** | $IO_{21}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $IO_9$ |
| **P** | $IO_{22}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $IO_{10}$ |
| **R** | $IO_{23}$ | NC | NC | NC | NC | NC | $IO_{11}$ |
| **T** | NC | A | A | $\overline{WE}$ | A | A | NC |
| **U** | NC | A | A | $\overline{OE}$ | A | A | NC |

**Note**
1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on $V_{CC}$ Relative to GND [2] ....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5V to $V_{CC}$ + 0.5V

DC Input Voltage [2] ..... –0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... .....>2001V (MIL-STD-883, Method 3015)

Latch up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40°C to +85°C | 3.3V ± 0.3V |

## DC Electrical Characteristics

Over the operating range

| Parameter | Description | Test Conditions [3] | –10 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ [2] | Input LOW Voltage | | –0.3 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –1 | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, output disabled | –1 | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max, f = $f_{MAX}$ = 1/$t_{RC}$, $I_{OUT}$ = 0 mA CMOS levels | | 175 | mA |
| $I_{SB1}$ | Automatic CE Power Down Current — TTL Inputs | Max $V_{CC}$, $\overline{CE}_1$, $\overline{CE}_3$ ≥ $V_{IH}$, $CE_2$ ≤ $V_{IL}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | 30 | mA |
| $I_{SB2}$ | Automatic CE Power Down Current — CMOS Inputs | Max $V_{CC}$, $\overline{CE}_1$, $\overline{CE}_3$ ≥ $V_{CC}$ – 0.3V, $CE_2$ ≤ 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | | 25 | mA |

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 8 | pF |
| $C_{OUT}$ | IO Capacitance | | 10 | pF |

## Thermal Resistance

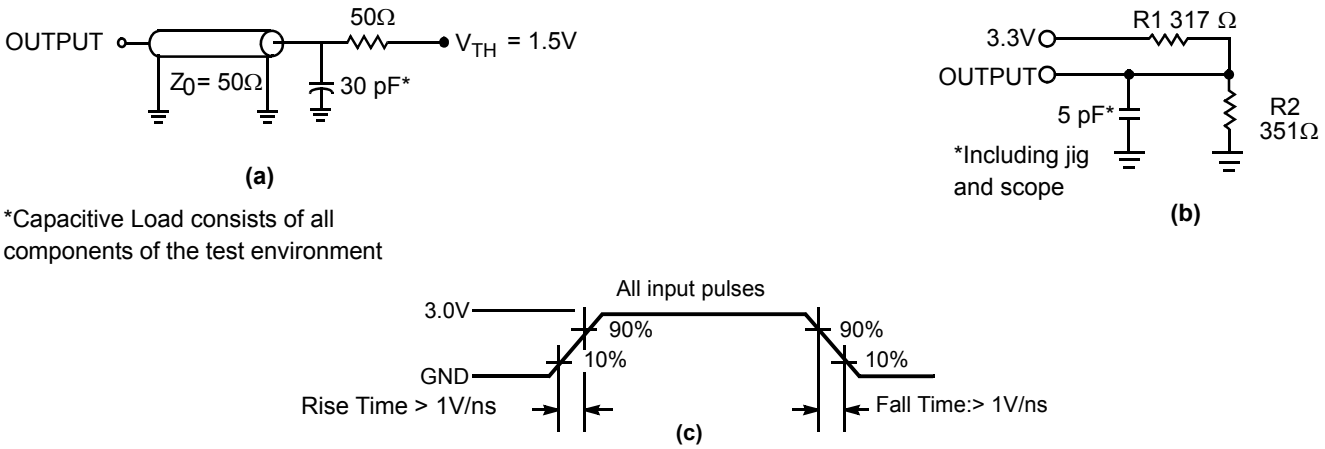
Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | 119-Ball PBGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board | 20.31 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 8.35 | °C/W |

**Notes**

2. $V_{IL}$ (min) = –2.0V and $V_{IH}$(max) = $V_{CC}$ + 2V for pulse durations of less than 20 ns.
3. $\overline{CE}$ refers to a combination of $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$. $\overline{CE}$ is active LOW when $\overline{CE}_1$ is LOW, $CE_2$ is HIGH, and $\overline{CE}_3$ is LOW. $\overline{CE}$ is HIGH when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.

**Figure 2. AC Test Loads and Waveform [4]**




## AC Switching Characteristics

Over the operating range [5]

| Parameter | Description | –10 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{power}$ [6] | $V_{CC}$(Typical) to the First Access | 100 | | µs |
| $t_{RC}$ | Read Cycle Time | 10 | | ns |
| $t_{AA}$ | Address to Data Valid | | 10 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}$ Active LOW to Data Valid [3] | | 10 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 5 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [7] | 1 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [7] | | 5 | ns |
| $t_{LZCE}$ | $\overline{CE}$ Active LOW to Low Z [3, 7] | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ Deselect HIGH to High Z [3, 7] | | 5 | ns |
| $t_{PU}$ | $\overline{CE}$ Active LOW to Power Up [3, 8] | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ Deselect HIGH to Power Down [3, 8] | | 10 | ns |

**Notes**

4. Valid SRAM operation does not occur until the power supplies reach the minimum operating $V_{DD}$ (3.0V). 100 µs ($t_{power}$) after reaching the minimum operating $V_{DD}$, normal SRAM operation begins including reduction in $V_{DD}$ to the data retention ($V_{CCDR}$, 2.0V) voltage.
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading as shown in part a) of the AC Test Loads and Waveform [4], unless specified otherwise.
6. $t_{POWER}$ gives the minimum amount of time that the power supply is at typical $V_{CC}$ values until the first memory access is performed.
7. $t_{HZOE}$, $t_{HZCE}$, $t_{HZWE}$, $t_{LZOE}$, $t_{LZCE}$, and $t_{LZWE}$ are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady state voltage.
8. These parameters are guaranteed by design and are not tested.

## AC Switching Characteristics (continued)

Over the operating range [5]

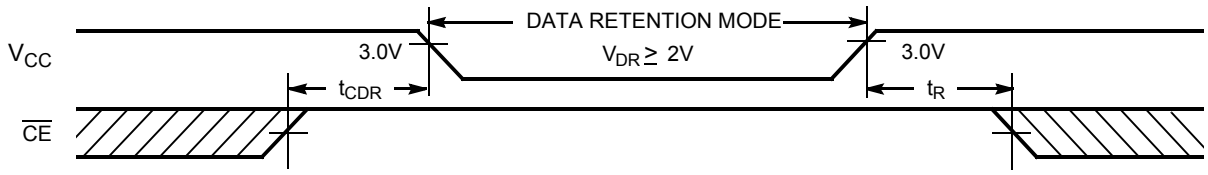
| Parameter | Description | –10 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Write Cycle** [9, 10] | | | | |
| $t_{WC}$ | Write Cycle Time | 10 | | ns |
| $t_{SCE}$ | $\overline{CE}$ Active LOW to Write End [3] | 7 | | ns |
| $t_{AW}$ | Address Setup to Write End | 7 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 7 | | ns |
| $t_{SD}$ | Data Setup to Write End | 5.5 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [7] | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [7] | | 5 | ns |

## Data Retention Characteristics

Over the operating range

| Parameter | Description | Conditions [3] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2 | | | V |
| $I_{CCDR}$ | Data Retention Current9 | $V_{CC} = 2V$, $\overline{CE_1}$, $\overline{CE_3} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | | 25 | mA |
| $t_{CDR}$ [11] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$ [12] | Operation Recovery Time | | $t_{RC}$ | | | ns |

**Figure 3. Data Retention Waveform**




**Notes**

9. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ LOW, $CE_2$ HIGH, $\overline{CE_3}$ LOW, and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ must be LOW to initiate a write and the transition of any of these signals terminates the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [13, 14]

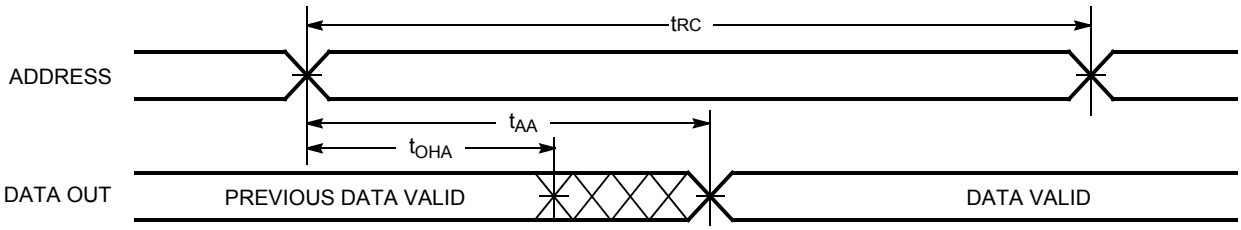



**Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [3, 14, 15]

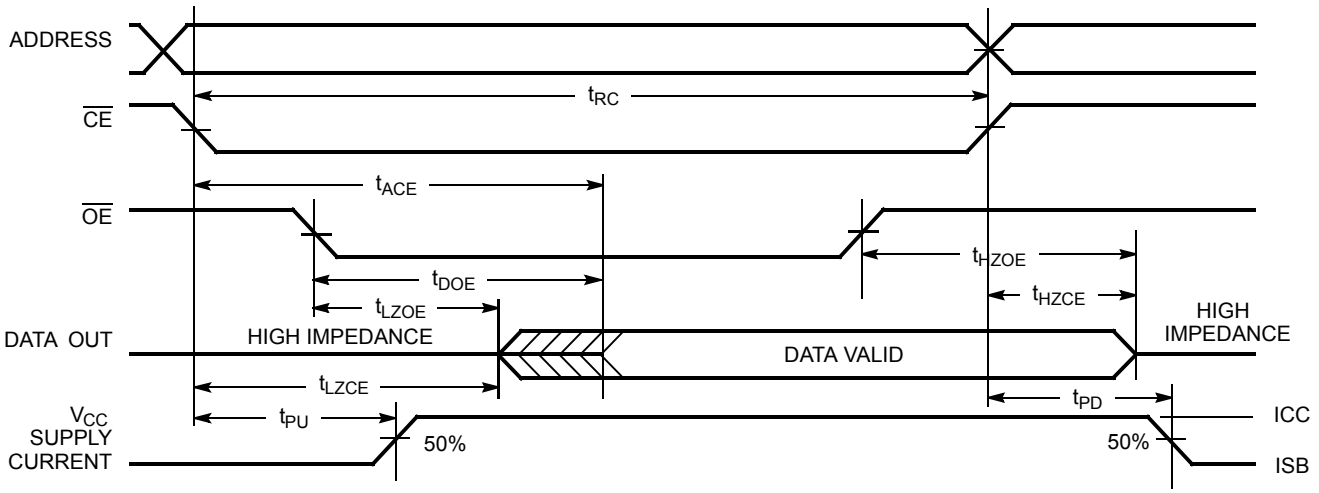
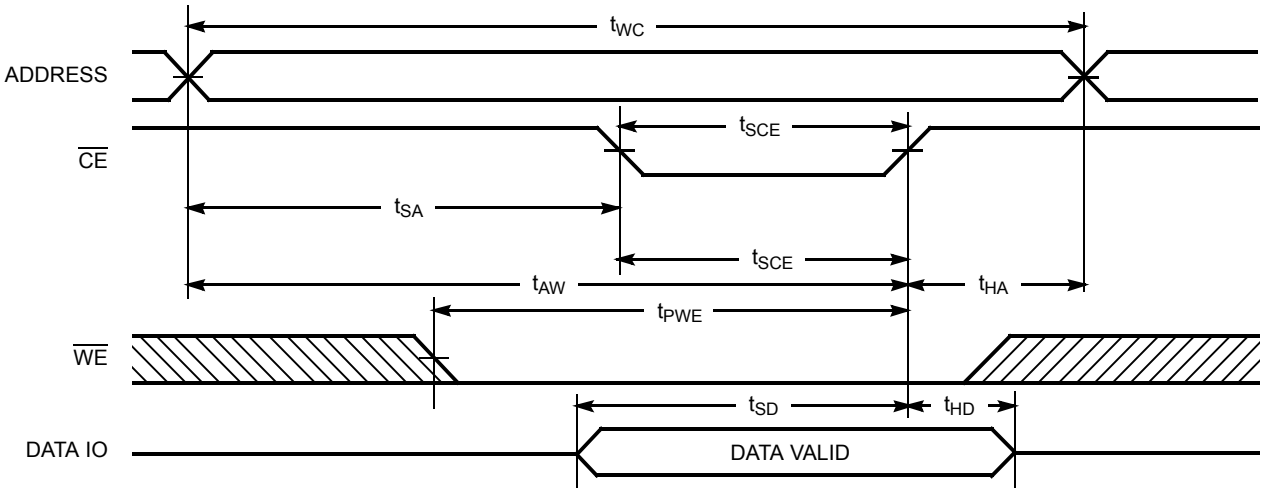



**Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled)** [3, 16, 17]




**Notes**
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid before or similar to $\overline{CE}$ transition LOW.
16. Data IO is high impedance if $\overline{OE}$ = $V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [3, 16, 17]**

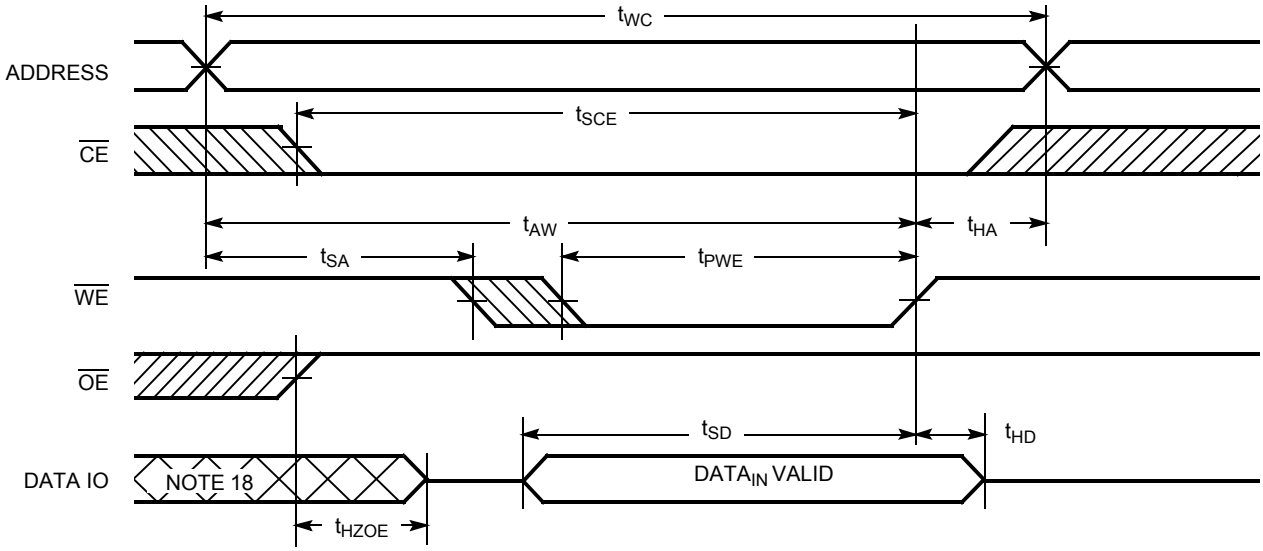
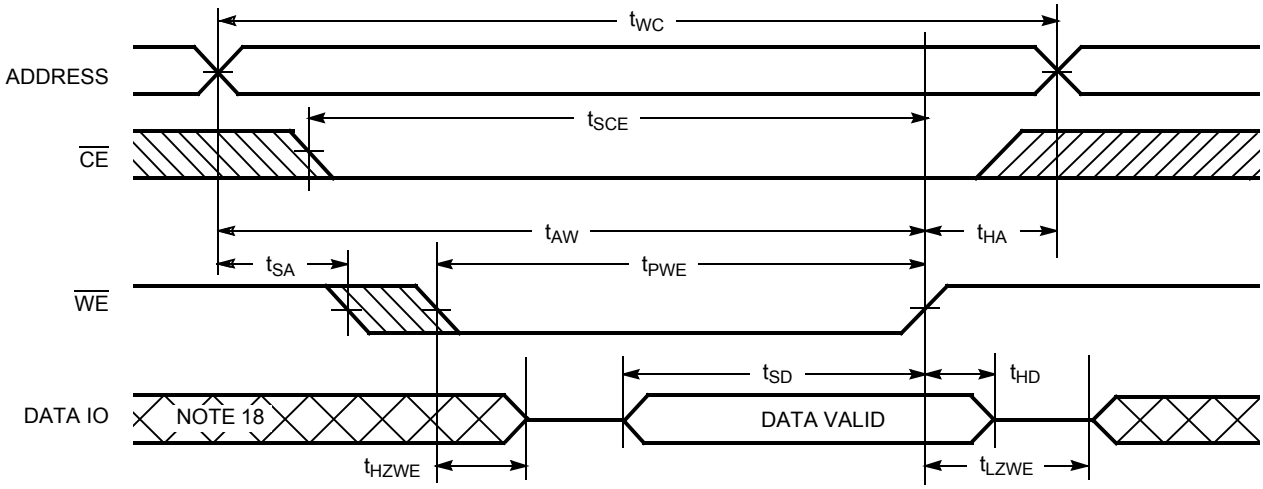



**Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [3, 17]**




## Truth Table

| $\overline{CE_1}$ | $CE_2$ | $\overline{CE_3}$ | $\overline{OE}$ | $\overline{WE}$ | $IO_0 – IO_{23}$ | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Power Down | Standby ($I_{SB}$) |
| X | L | X | X | X | High Z | Power Down | Standby ($I_{SB}$) |
| X | X | H | X | X | High Z | Power Down | Standby ($I_{SB}$) |
| L | H | L | L | H | Full Data Out | Read | Active ($I_{CC}$) |
| L | H | L | X | L | Full Data In | Write | Active ($I_{CC}$) |
| L | H | L | H | H | High Z | Selected, Outputs Disabled | Active ($I_{CC}$) |

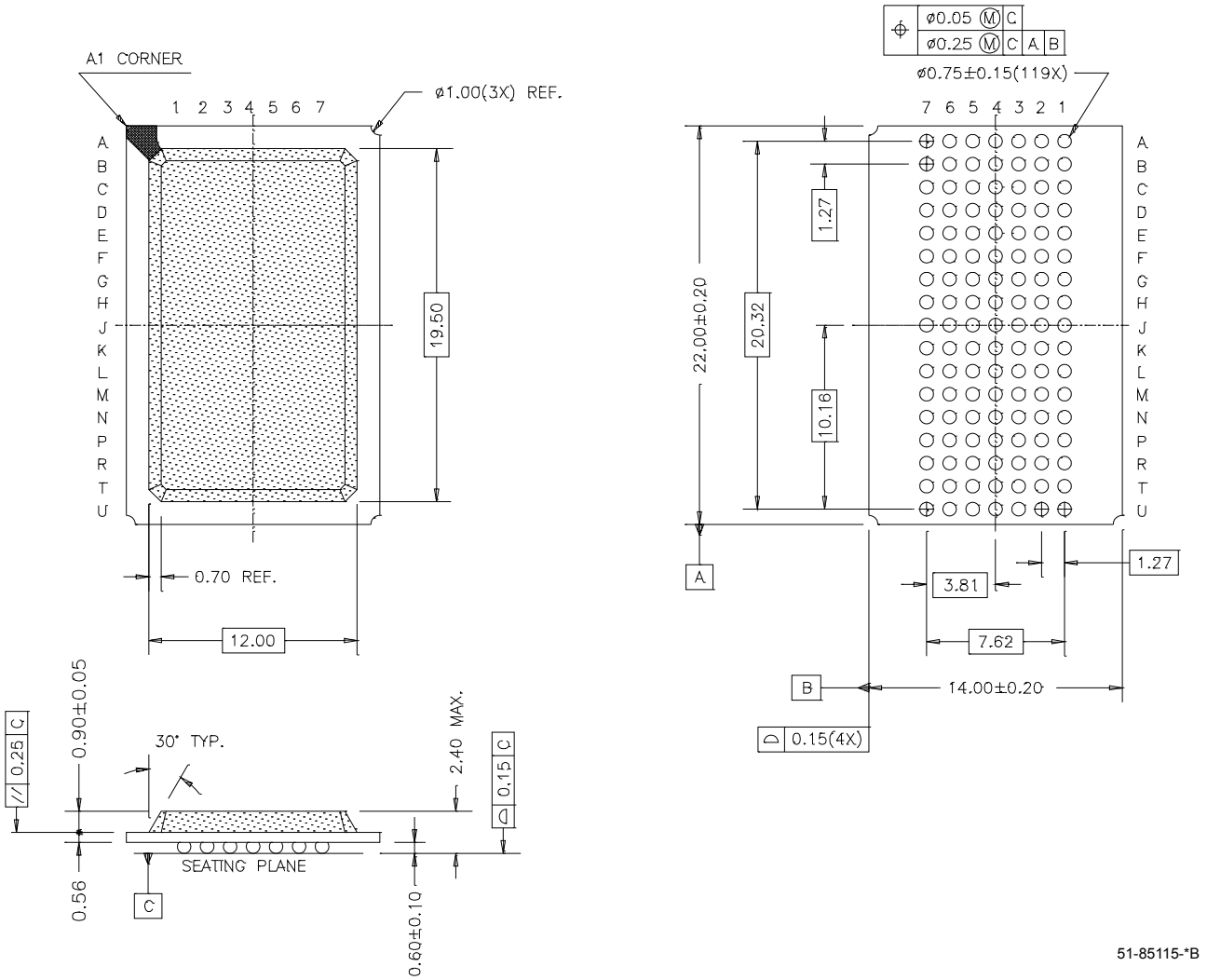
**Note**
18. During this period, the IOs are in the output state and input signals are not applied.

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C1034DV33-10BGXI | 51-85115 | 119-Ball Plastic Ball Grid Array (14 x 22 x 2.4 mm) (Pb-Free) | Industrial |

## Package Diagram

**Figure 9. 119-Ball PBGA (14 x 22 x 2.4 mm)**



## Document History Page

| Document Title: CY7C1034DV33 6-Mbit (256K X 24) Static RAM<br>Document Number: 001-08351 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 469517 | NXR | See ECN | New data sheet |
| *A | 499604 | NXR | See ECN | Added note 1 for NC pins<br>Changed $I_{CC}$ specification from 150 mA to 185 mA<br>Updated Test Condition for $I_{CC}$ in DC Electrical Characteristics table<br>Added note for $t_{ACE}$, $t_{LZCE}$, $t_{HZCE}$, $t_{PU}$, $t_{PD}$, $t_{SCE}$ in AC Switching Characteristics Table on page 4 |
| *B | 1462586 | VKN/SFV | See ECN | Converted from preliminary to final<br>Updated block diagram<br>Changed $I_{CC}$ specification from 185 mA to 225 mA<br>Updated thermal specs |
| *C | 2644842 | VKN/PYRS | 01/23/09 | Replaced Commercial range with the Industrial<br>Replaced 8 ns speed with 10 ns |

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