CY62148ESL MoBL®

4-Mbit (512K x 8) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 2.2V to 3.6V and 4.5V to 5.5V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 32-pin STSOP package

Functional Description

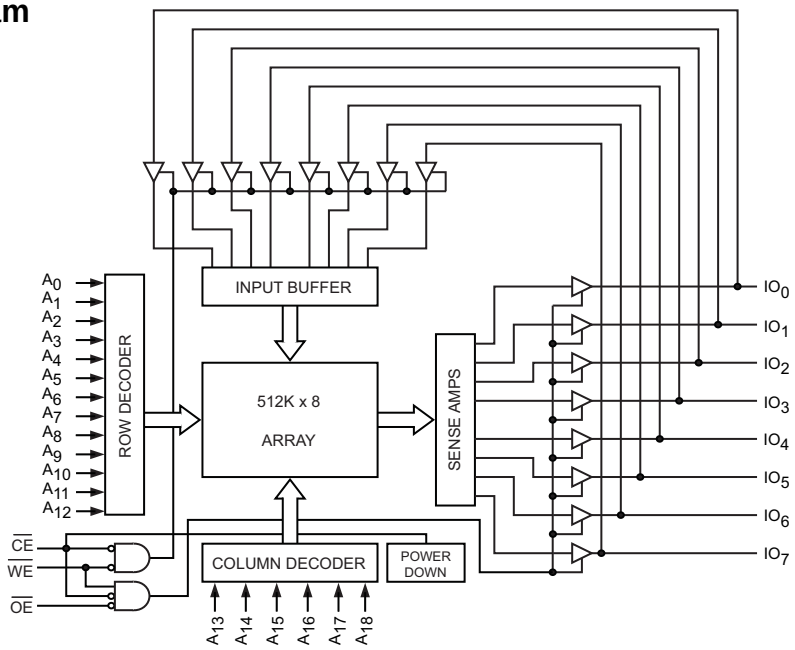
The CY62148ESL is a high performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight IO pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



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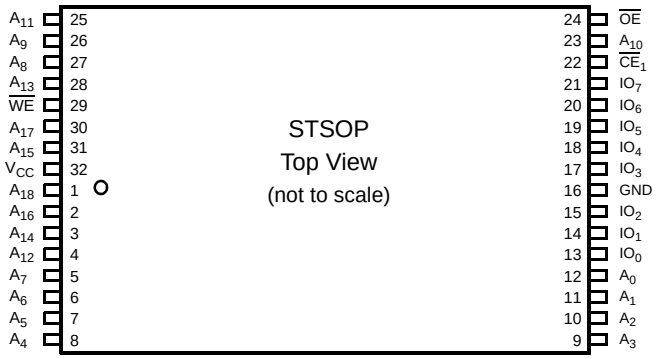
Pin Configuration

Figure 1. 32-Pin STSOP (Top View)



Product Portfolio

Product	Range	V_{CC} Range (V) [1]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1 MHz		f = f_{max}			
				Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62148ESL	Industrial	2.2V to 3.6V and 4.5V to 5.5V	55	2	2.5	15	20	1	7

Notes
1. Data sheet specifications are not guaranteed for V_{CC} in the range of 3.6V to 4.5V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to 6.0V

DC Voltage Applied to Outputs in High-Z State [3, 4] .....–0.5V to 6.0V

DC Input Voltage [3, 4] .....–0.5V to 6.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62148ESL	Industrial	–40°C to +85°C	2.2V to 3.6V, and 4.5V to 5.5V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [2]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4			
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4			
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA			0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA			0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1 mA			0.4	
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$		1.8		V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2		V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2		V_{CC} + 0.5	
V_{IL} [6]	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$		–0.3		0.4	V
		$2.7 \le V_{CC} \le 3.6$		–0.3		0.6	
		$4.5 \le V_{CC} \le 5.5$		–0.5		0.6	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1		+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$ I_{OUT} = 0 mA, CMOS levels		15	20	mA
		f = 1 MHz			2	2.5	
I_{SB1}	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$			1	7	µA
I_{SB2}	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0, $V_{CC} = V_{CC(max)}$			1	7	µA

Notes

3. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
4. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Under DC conditions the device meets a V_{IL} of 0.8V (for V_{CC} range of 2.7V to 3.6V and 4.5V to 5.5V) and 0.6V (for V_{CC} range of 2.2V to 2.7V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6V and 0.4V for the above ranges. Refer to AN13470 for details.

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Capacitance

Tested initially and after any design or process changes that may affect these parameters.

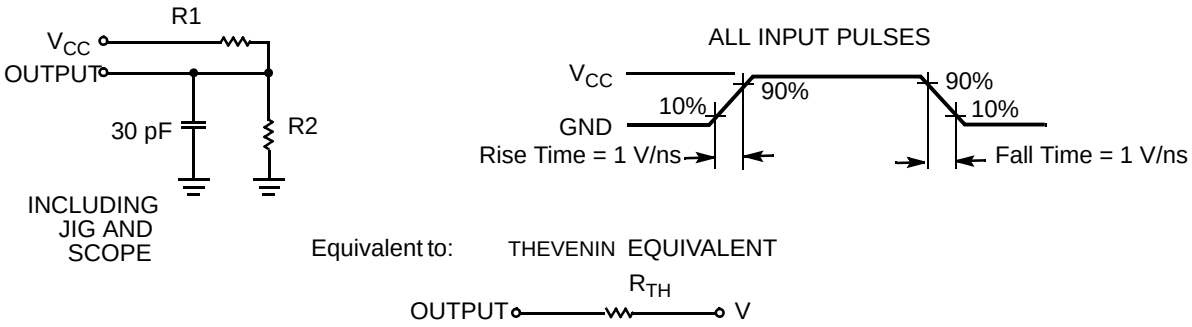
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	STSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two layer printed circuit board	49.02	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		14.07	°C/W

Figure 2. AC Test Loads and Waveforms



Parameters	2.50V	3.0V	5.0V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

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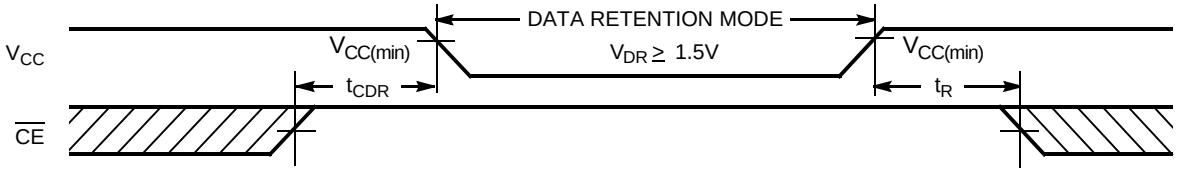
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [2]	Max	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	V_{CC} = 1.5V		1	7	µA
t_{CDR} [7]	Chip Deselect to Data Retention Time			0			ns
t_R [8]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

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Switching Characteristics

Over the Operating Range [9]

Parameter	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [10]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [10, 11]		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [10]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [10, 11]		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Up		55	ns
Write Cycle [12]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		ns
t_{AW}	Address Setup to Write End	40		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [10, 11]		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [10]	10		ns

Notes

9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms on page 4.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

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Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [13, 14]

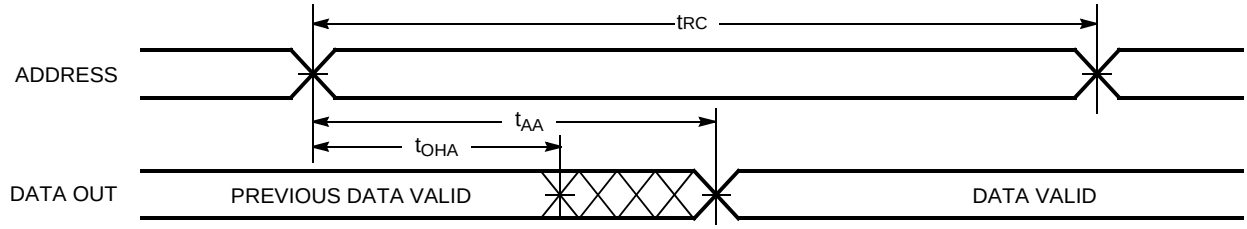


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [14, 15]

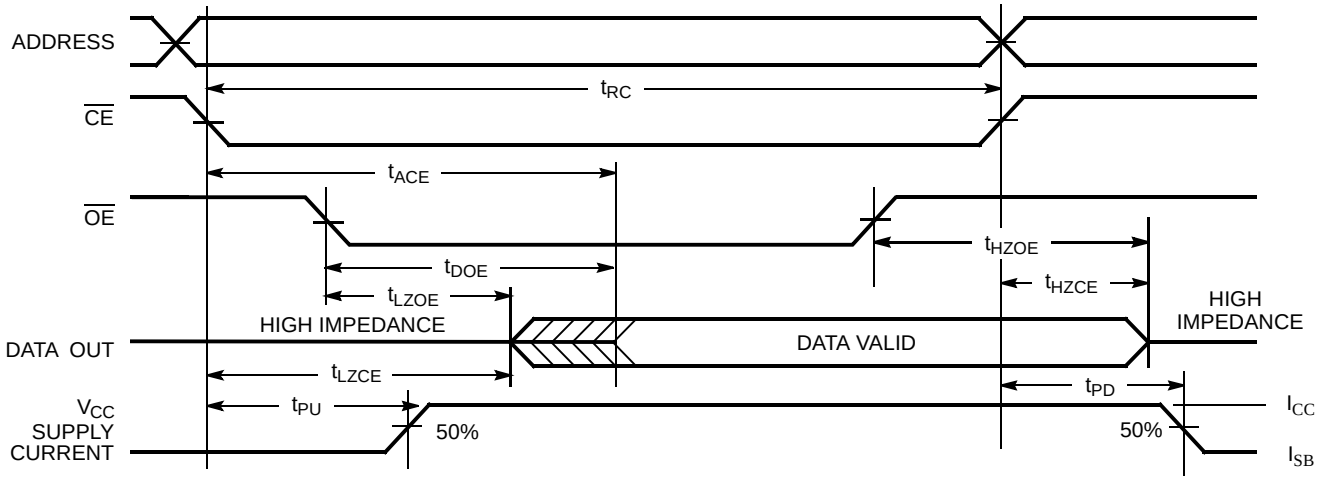
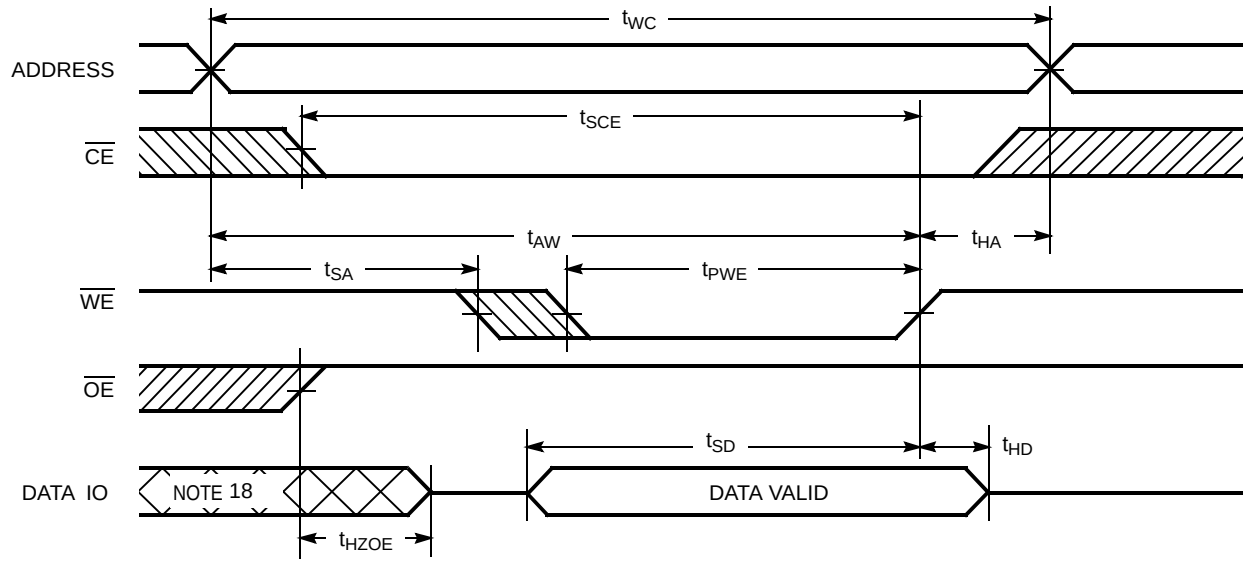


Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [16, 17]



Notes

13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycles.
15. Address valid before or similar to $\overline{CE}$ transition LOW.
16. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
18. During this period, the IOs are in output state. Do not apply input signals.

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Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [16, 17]

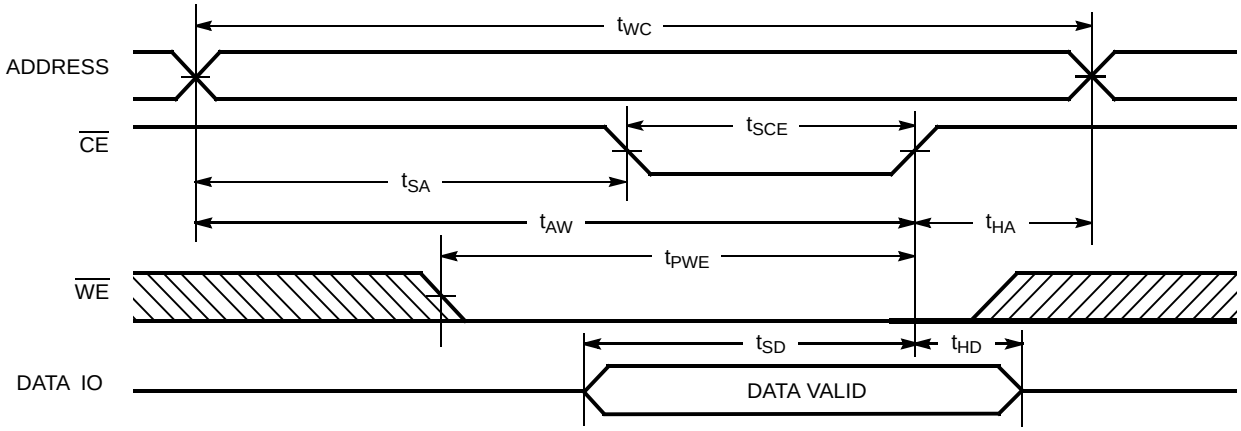
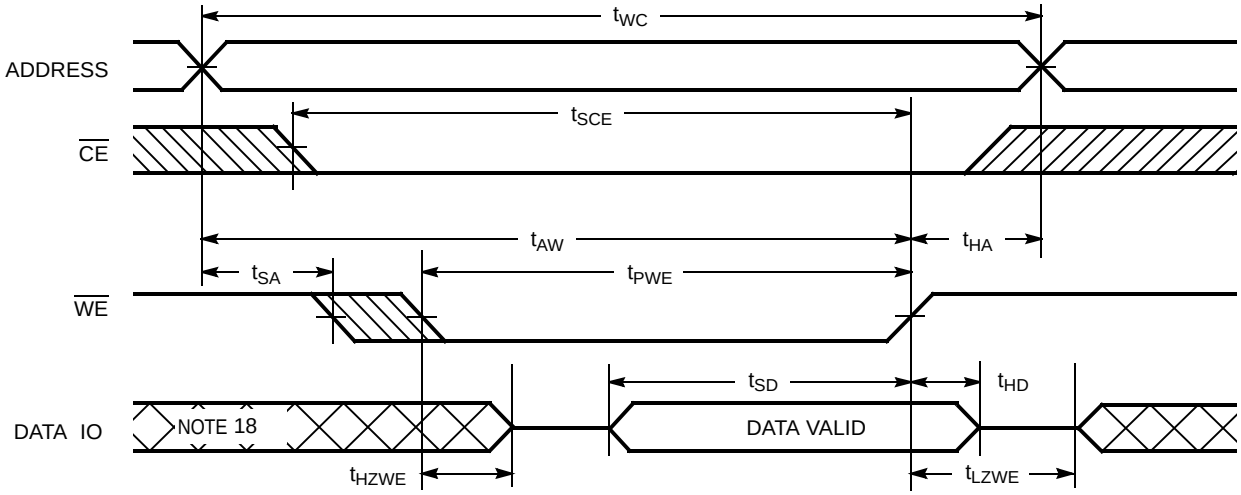


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

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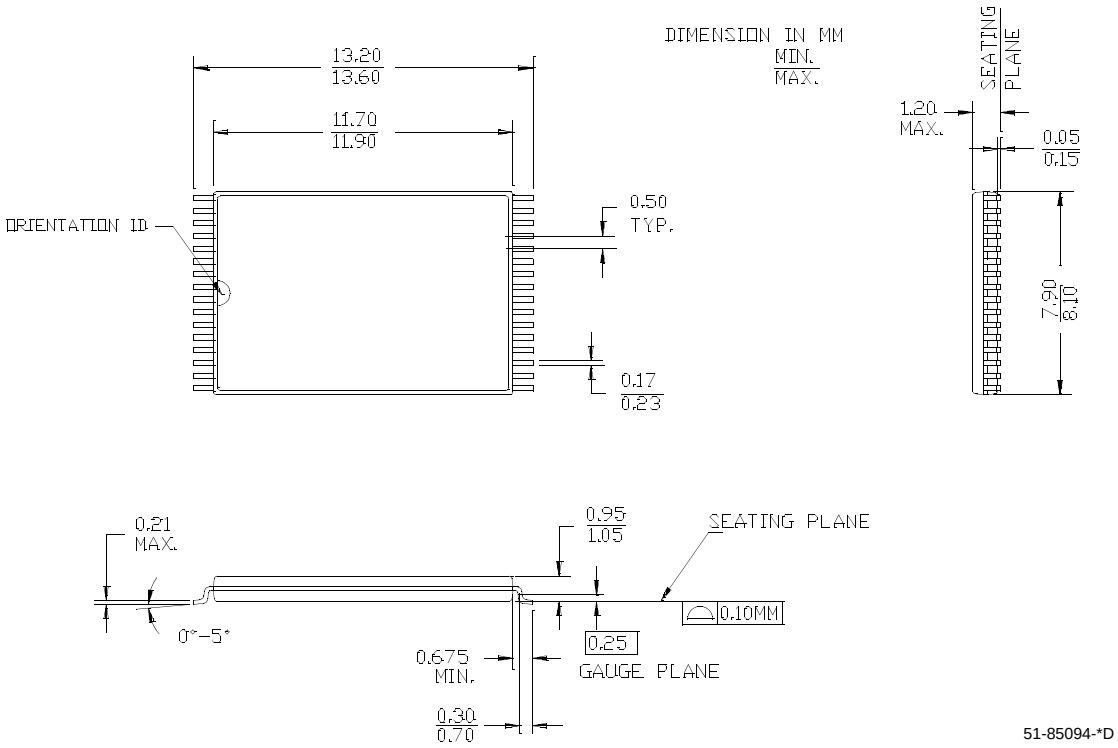
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148ESL-55ZAXI	51-85094	32-Pin STSOP (Pb-Free)	Industrial

Package Diagram

Figure 8. 32-Pin Shrunk Thin Small Outline Package (8 x 13.4 mm), 51-85094



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Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2612938	VKN/PYRS	01/21/09	New data sheet

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