# CY14B256K

## 256 Kbit (32K x 8) nvSRAM with Real Time Clock

### Features

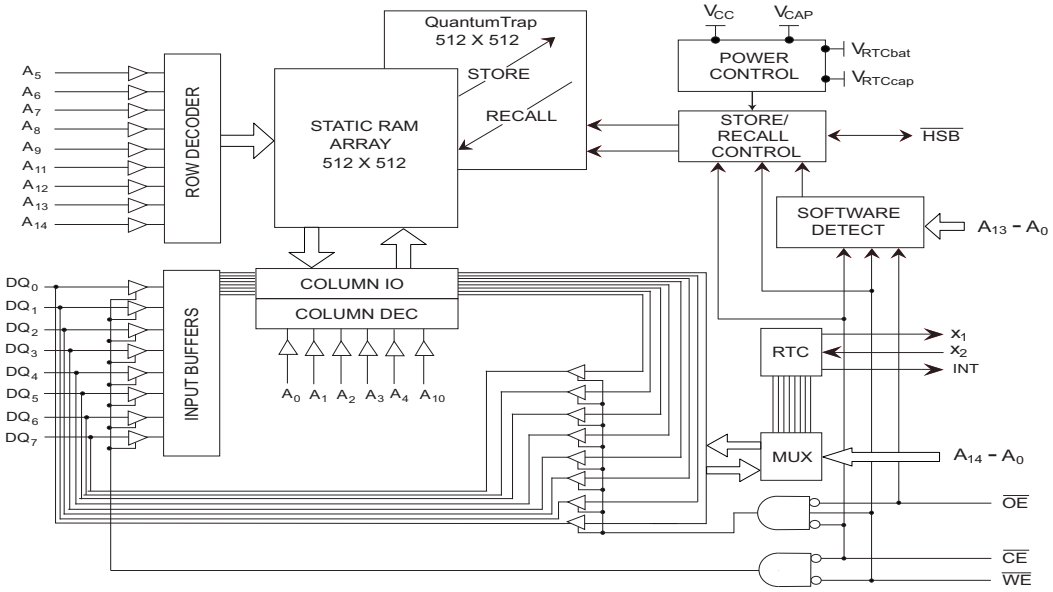
- 25 ns, 35 ns, and 45 ns access times
- Pin compatible with STK17T88
- Data integrity of Cypress nvSRAM combined with full featured Real Time Clock
  - Low power, 350 nA RTC current
  - Capacitor or battery backup for RTC
- Watchdog timer
- Clock alarm with programmable interrupts
- Hands off automatic *STORE* on power down with only a small capacitor
- *STORE* to QuantumTrap™ initiated by software, device pin, or on power down
- *RECALL* to SRAM initiated by software or on power up
- Infinite *READ, WRITE,* and *RECALL* cycles
- High reliability
  - Endurance to 200K cycles
  - Data retention: 20 years at 55°C
- Single 3V operation with tolerance of +20%, -10%
- Commercial and industrial temperature
- 48-Pin SSOP (ROHS compliant)

### Functional Description

The Cypress CY14B256K combines a 256 Kbit nonvolatile static RAM with a full-featured real time clock in a monolithic integrated circuit. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM is read and written an infinite number of times, while independent, nonvolatile data resides in the nonvolatile elements.

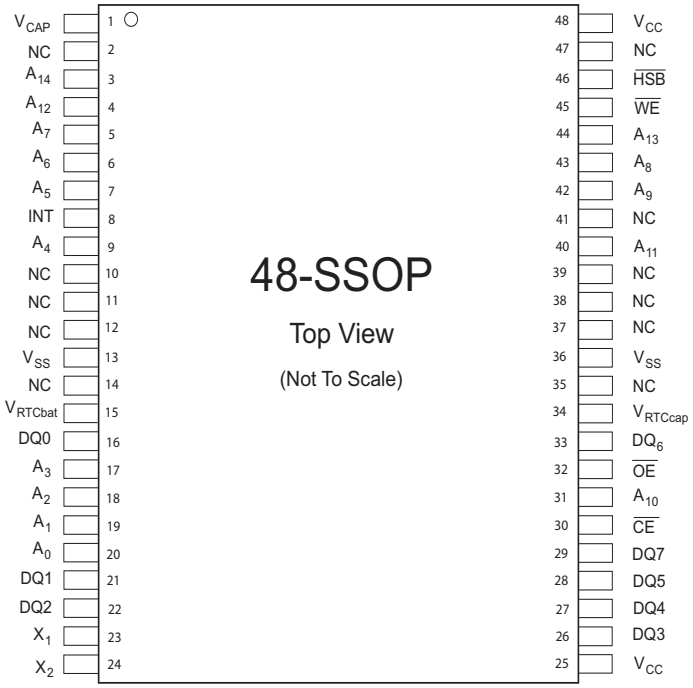
The real time clock function provides an accurate clock with leap year tracking and a programmable high accuracy oscillator. The alarm function is programmable for one time alarms or periodic seconds, minutes, hours, or days. There is also a programmable watchdog timer for process control.

### Logic Block Diagram



## Pin Configurations

**Figure 1. 48-Pin SSOP**




## Pin Definitions

| Pin Name | Alt | IO Type | Description |
|---|---|---|---|
| $A_0$–$A_{14}$ | | Input | **Address Inputs.** Used to select one of the 32,768 bytes of the nvSRAM. |
| DQ0-DQ7 | | Input or Output | **Bidirectional Data IO lines**. Used as input or output lines depending on operation. |
| NC | | No Connect | **No Connects**. This pin is not connected to the die. |
| $\overline{WE}$ | $\overline{W}$ | Input | **Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location. |
| $\overline{CE}$ | $\overline{E}$ | Input | **Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{OE}$ | $\overline{G}$ | Input | **Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ high causes the IO pins to tri-state. |
| $X_1$ | | Output | **Crystal Connection**. Drives crystal on start up. |
| $X_2$ | | Input | **Crystal Connection for 32.768 kHz Crystal**. |
| $V_{RTCcap}$ | | Power Supply | **Capacitor Supplied Backup RTC Supply Voltage**. (Left unconnected if $V_{RTCbat}$ is used) |
| $V_{RTCbat}$ | | Power Supply | **Battery Supplied Backup RTC Supply Voltage**. (Left unconnected if $V_{RTCcap}$ is used) |
| INT | | Output | **Interrupt Output**. It is programmed to respond to the clock alarm, the watchdog timer, and the power monitor. Programmable to either active HIGH (push or pull) or LOW (open drain). |
| $V_{SS}$ | | Ground | **Ground for the Device**. It is connected to ground of the system. |
| $V_{CC}$ | | Power Supply | **Power Supply Inputs to the Device**. |
| $\overline{HSB}$ | | Input or Output | **Hardware Store Busy ($\overline{HSB}$)**. When low, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional). |
| $V_{CAP}$ | | Power Supply | **AutoStore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements. |

## Device Operation

The CY14B256K nvSRAM consists of two functional components paired in the same physical cell. The components are SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14B256K supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations.

See the "Truth Table For SRAM Operations" on page 22 for a complete description of read and write modes.

### SRAM READ

The CY14B256K performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0-14}$ determines which of the 32,752 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of $t_{AA}$ (see the section Figure 8 on page 17). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at $t_{ACE}$ or at $t_{DOE}$, whichever is later (see the section Figure 9 on page 17). The data outputs repeatedly respond to address changes within the $t_{AA}$ access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

### SRAM WRITE

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs are stable before entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common IO pins $DQ_{0-7}$ is written into the memory if the data is valid $t_{SD}$ before the end of a $\overline{WE}$ controlled WRITE or before the end of a $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers $t_{HZWE}$ after $\overline{WE}$ goes LOW.

### AutoStore® Operation

The CY14B256K stores data to nvSRAM using one of the three storage operations:

1. Hardware store activated by $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B256K.

During normal operation, the device draws current from $V_{CC}$ to charge a capacitor connected to the $V_{CAP}$ pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the $V_{CC}$ pin drops below $V_{SWITCH}$, the part automatically disconnects the $V_{CAP}$ pin from $V_{CC}$. A STORE operation is initiated with power provided by the $V_{CAP}$ capacitor.

**Figure 2. AutoStore Mode**

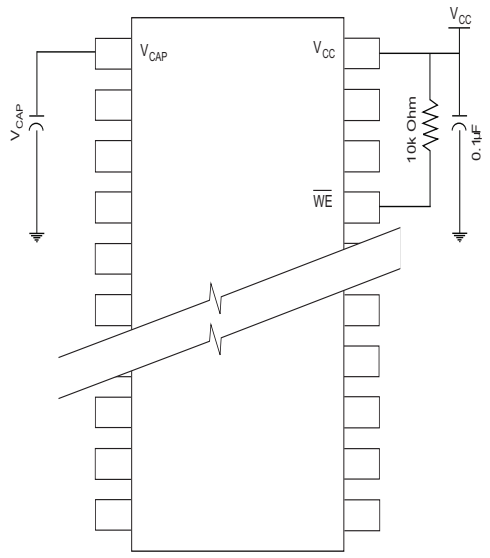



Figure 2 shows the proper connection of the storage capacitor ($V_{CAP}$) for automatic store operation. Refer to DC Electrical Characteristics on page 15 for the size of the $V_{CAP}$. The voltage on the $V_{CAP}$ pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on $\overline{WE}$ to hold it inactive during power up. This pull up is only effective if the $\overline{WE}$ signal is tri-state during power up. Many MPUs tri-state their controls on power up. Verify this when using the pull up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

### Hardware STORE ($\overline{HSB}$) Operation

The CY14B256K provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the CY14B256K conditionally initiates a STORE operation after $t_{DELAY}$. An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition, while the STORE (initiated by any means) is in progress. This pin is externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations, that are in progress when $\overline{HSB}$ is driven low by any means, are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the CY14B256K continues SRAM operations for $t_{DELAY}$. During

$t_{DELAY}$, multiple SRAM READ operations take place. If a WRITE is in progress when HSB is pulled LOW, it allows a time, $t_{DELAY}$, to complete. However, any SRAM WRITE cycles requested after HSB goes LOW are inhibited until HSB returns HIGH.

During any STORE operation, regardless of how it is initiated, the CY14B256K continues to drive the HSB pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the CY14B256K remains disabled until the HSB pin returns HIGH.

If HSB is not used, it is left unconnected.

### Hardware RECALL (Power Up)

During power up or after any low power condition ($V_{CC}$<$V_{SWITCH}$), an internal RECALL request is latched. When $V_{CC}$ again exceeds the sense voltage of $V_{SWITCH}$, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

### Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B256K software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further READs and WRITEs are inhibited untill the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If it intervenes, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with CE controlled READs or OE controlled READs. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important to use READ cycles and not WRITE cycles in the sequence, although it is not necessary that OE be LOW for a valid sequence. After the $t_{STORE}$ cycle time is fulfilled, the SRAM is activated again for READ and WRITE operations.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and then the nonvolatile information is transferred into the SRAM cells. After the $t_{RECALL}$ cycle time, the SRAM is again ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

### Data Protection

The CY14B256K protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when $V_{CC}$ is less than $V_{SWITCH}$.

If the CY14B256K is in a WRITE mode (both CE and WE are low) at power up after a RECALL, or after a STORE, the WRITE is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brown out conditions.

### Noise Considerations

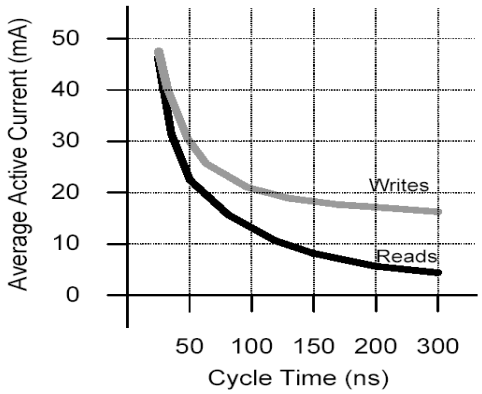
The CY14B256K is a high speed memory and must have a high frequency bypass capacitor of approximately 0.1 µF connected between $V_{CC}$ and $V_{SS}$ using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

## Low Average Active Power

CMOS technology provides the CY14B256K the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 shows the relationship between $I_{CC}$ and READ and/or WRITE cycle time. Worst case current consumption is shown for commercial temperature range, $V_{CC}$ = 3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B256K depends on the following items:

1. 1The duty cycle of chip enable
2. The overall cycle rate for accesses
3. The ratio of READs to WRITEs
4. The operating temperature
5. The $V_{CC}$ level
6. IO loading

**Figure 3. Current versus Cycle Time**




## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration and cold or warm boot status must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- The OSCEN bit in the Calibration register at 0x7FF8 should be set to 1 to preserve battery life when the system is in storage (see Stopping and Starting the Oscillator on page 7).
- The Vcap value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum Vcap value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger Vcap value to make sure there is extra store charge should discuss their Vcap size selection with Cypress.

**Table 1. Mode Selection**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | A13–A0 | Mode | IO | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Not Selected | Output High Z | Standby |
| L | H | L | X | Read SRAM | Output Data | Active |
| L | L | X | X | Write SRAM | Input Data | Active |
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0FC0 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile STORE | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active $I_{CC2}$[1, 2, 3] |
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0C63 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile RECALL | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active[1, 2, 3] |

**Notes**
1. The six consecutive address locations are in the order listed. $\overline{WE}$ is HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 15 address lines on the CY14B256K, only the lower 14 lines are used to control software modes.
3. IO state depends on the state of $\overline{OE}$. The IO table shown is based on $\overline{OE}$ Low.

## Real Time Clock Operation

### nvTIME Operation

The CY14B256K consists of internal registers that contain clock, alarm, watchdog, interrupt, and control functions. RTC registers use the last 16 address locations of the SRAM. Internal double buffering of the clock and the clock and timer information registers prevent accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or clock accuracy of the internal clock while accessing clock data. Clock and Alarm registers store data in BCD format.

The RTC register addresses for CY14B256K range from 0x7FF0 to 0x7FFF. Refer to RTC Register Map[5, 6] on page 11 and Register Map Detail on page 12 for detailed description.

### Clock Operations

The Clock registers maintain time up to 9,999 years in one second increments. The user sets the time to any calendar time and the clock automatically keeps track of days of the week, month, leap years, and century transitions. There are eight registers dedicated to the clock functions that are used to set time with a write cycle and to read time during a read cycle. These registers contain the time of day in BCD format. Bits defined as ‘0’ are currently not used and are reserved for future use by Cypress.

### Reading the Clock

The double buffered RTC register structure reduces the chance of reading incorrect data from the clock. The user should stop internal updates to the CY14B256K time keeping registers before reading clock data, to prevent reading of data in transition. Stopping the internal register updates does not affect clock accuracy.

The updating process is stopped by writing a ‘1’ to the read bit ‘R’ (in the flags register at 0x7FF0), and does not restart until a ‘0’ is written to the read bit. The RTC registers are then read while the internal clock continues to run. After a ‘0’ is written to the read bit (‘R’), all CY14B256K registers are simultaneously updated within 20 ms.

### Setting the Clock

Setting the write bit ‘W’ (in the flags register at 0x7FF0) to a ‘1’ stops updates to the time keeping registers and enables the time to be set. The correct day, date, and time is then written into the registers in 24 hour BCD format. The time written is referred to as the “Base Time”. This value is stored in nonvolatile registers and used in the calculation of the current time. Resetting the write bit to ‘0’ transfers the register values to the actual clock counters, after which the clock resumes normal operation.

### Backup Power

The RTC in the CY14B256K is intended for permanently powered operation. The $V_{RTCcap}$ or $V_{RTCbat}$ pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, $V_{CC}$, fails and drops below $V_{SWITCH}$ the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During backup operation, the CY14B256K consumes a maximum of 300 nanoamps at 2 volts. The user should choose capacitor or battery values according to the application. Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately three times longer.

**Table 2. RTC Backup Time**

| Capacitor Value | Backup Time |
|---|---|
| 0.1F | 72 hours |
| 0.47F | 14 days |
| 1.0F | 30 days |

Using a capacitor has the advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3V lithium is recommended and the CY14B256K sources current only from the battery when the primary power is removed. The battery is not, however, recharged at any time by the CY14B256K. The battery capacity must be chosen for total anticipated cumulative down time required over the life of the system.

### Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x7FF8 controls the enable and disable of the oscillator. This active LOW bit is nonvolatile and is shipped to customers in the “enabled” (set to 0) state. To preserve the battery life when the system is in storage, OSCEN bit must be set to ‘1’. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately 5 seconds (10 seconds maximum) for the oscillator to start.

While system power is off, if the voltage on the backup supply ($V_{RTCcap}$ or $V_{RTCbat}$) falls below their respective minimum level, the oscillator may fail.The CY14B256K has the ability to detect oscillator failure when system power is restored. This is recorded in the OSCF (Oscillator Failed bit) of the Flags register at address 0x7FF0. When the device is powered on ($V_{CC}$ goes above $V_{SWITCH}$), the OSCEN bit is checked for “enabled” status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set to “1”. The system must check for this condition and then write ‘0’ to clear the flag. Note that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see “Setting the Clock” on page 7), which is the value last written to the time keeping registers. The Control or Calibration registers and the OSCEN bit are not affected by the “oscillator failed” condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

To reset OSCF, set the write bit “W” (in the flags register at 0x7FF0) to “1” to enable writes to the Flag register. Write a “0” to the OSCF bit and then reset the write bit to “0” to disable writes.

### Calibrating the Clock

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal and calibration. The crystal oscillators typically have an error of ±20ppm to ±35ppm. However, CY14B256K employs a calibration circuit that improves the accuracy to +1/–2 ppm at 25°C. This implies an error of +2.5 seconds to -5 seconds per month.

The calibration circuit adds or subtracts counts from the oscillator divider circuit to achieve this accuracy. The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in Calibration register at 0x7FF8. The calibration bits occupy the five lower order bits in the Calibration register. These bits are set to represent any value between ‘0’ and 31 in binary form. Bit D5 is a sign bit, where a ‘1’ indicates positive calibration and a ‘0’ indicates negative calibration. Adding counts speeds the clock up and subtracting counts slows the clock down. If a binary ‘1’ is loaded into the register, it corresponds to an adjustment of 4.068 or –2.034 ppm offset in oscillator error, depending on the sign.

Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second shortened by 128 or lengthened by 256 oscillator cycles. If a binary ‘1’ is loaded into the register, only the first two minutes of the 64 minute cycle is modified. If a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, 4.068 or –2.034 ppm of adjustment per calibration step in the Calibration register.

To determine the required calibration, the CAL bit in the Flags register (0x7FF0) must be set to ‘1’. This causes the INT pin to toggle at a nominal frequency of 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20 ppm error. Hence, a decimal value of –10 (001010b) must be loaded into the Calibration register to offset this error.

**Note** Setting or changing the Calibration register does not affect the test output frequency.

To set or clear CAL, set the write bit “W” (in the flags register at 0x7FF0) to “1” to enable writes to the Flag register. Write a value to CAL, and then reset the write bit to “0” to disable writes.

### Alarm

The alarm function compares user programmed values of alarm time and date (stored in the registers 0x7FF1-5) with the corresponding time of day and date values. When a match occurs, the alarm internal flag (AF) is set and an interrupt is generated on INT pin if Alarm Interrupt Enable (AIE) bit is set.

There are four alarm match fields - date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required and therefore, alarm is disabled. Selecting all match bits (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x7FF0 indicates that a date or time match has occurred. The AF bit is set to “1” when a match occurs. Reading the flags or control register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

**Note** CY14B256K requires the alarm match bit for seconds (0x7FF2 - D7) to be set to ‘0’ for proper operation of Alarm Flag and Interrupt.

Alarm registers are not nonvolatile and, therefore, need to be reinitialized by software on power up. To set, clear or enable an alarm, set the ‘W’ bit (in Flags Register - 0x7FF0) to ‘1’ to enable writes to Alarm Registers. After writing the alarm value, clear the ‘W’ bit back to “0” for the changes to take effect.

### Watchdog Timer

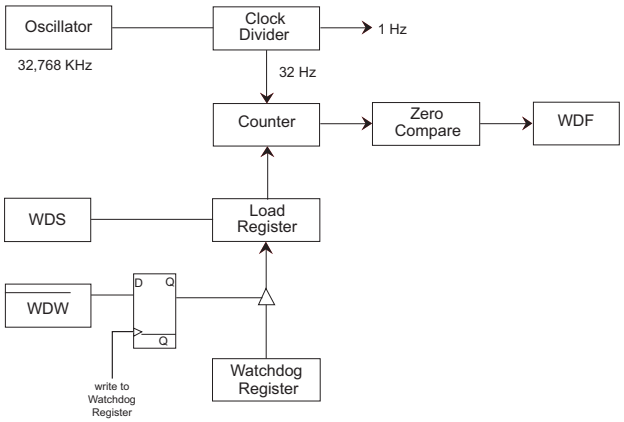
The Watchdog Timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register.

The timer consists of a loadable register and a free running counter. On power up, the watchdog time out value in register 0x7FF7 is loaded into the Counter Load register. Counting begins on power up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to ‘1’. The counter is compared to the terminal value of ‘0’. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the time out interrupt by setting WDS bit to ‘1’ prior to the counter reaching ‘0’. This causes the counter to reload with the watchdog time out value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and WDF flag never occur.

New time out values are written by setting the watchdog write bit to ‘0’. When the WDW is ‘0’, new writes to the watchdog time out value bits D5-D0 are enabled to modify the time out value. When WDW is ‘1’, writes to bits D5-D0 are ignored. The WDW function enables a user to set the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 4. Note that setting the watchdog time out value to ‘0’ disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to time out. The flag is set upon a watchdog time out and cleared when the user reads the Flags or Control registers. If the watchdog time out occurs, the user also enables an optional interrupt source to drive the INT pin.

**Figure 4. Watchdog Timer Block Diagram**




## Power Monitor

The CY14B256K provides a power management scheme with power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low $V_{CC}$ access. The power monitor is based on an internal band gap reference circuit that compares the $V_{CC}$ voltage to $V_{SWITCH}$ threshold.

As described in the "AutoStore® Operation" on page 3, when $V_{SWITCH}$ is reached as $V_{CC}$ decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from $V_{CC}$ to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, read and write operations to nvSRAM are inhibited and the clock functions are not available to the user. The clock continues to operate in the background. The updated clock data is available to the user $t_{HRECALL}$ delay after $V_{CC}$ is restored to the device (see "AutoStore or Power Up RECALL" on page 19).

## Interrupts

The CY14B256K has a Flags register, Interrupt register and Interrupt logic that can signal interrupt to the microcontroller. There are three potential sources for interrupt: watchdog timer, power monitor, and alarm timer. Each of these can be individually enabled to drive the INT pin by appropriate setting in the Interrupt register (0x7FF6). In addition, each has an associated flag bit in the Flags register (0x7FF0) that the host processor uses to determine the cause of the interrupt. The INT pin driver has two bits that specify its behavior when an interrupt occurs.

An Interrupt is raised only if both a flag is raised by one of the three sources and the respective interrupt enable bit in Interrupts register is enabled (set to '1'). After an interrupt source is active, two programmable bits, H/L and P/L, determine the behavior of the output pin driver on INT pin. These two bits are located in the Interrupt register and can be used to drive level or pulse mode output from the INT pin. In pulse mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the level mode, the pin goes to its active polarity until the Flags register is read by the user. This mode is used as an interrupt to a host microcontroller. The control bits are summarized in the following section.

### Interrupt Register

**Watchdog Interrupt Enable - WIE**. When set to '1', the watchdog timer drives the INT pin and an internal flag when a watchdog time out occurs. When WIE is set to '0', the watchdog timer only affects the WDF flag in Flags register.

**Alarm Interrupt Enable - AIE**. When set to '1', the alarm match drives the INT pin and an internal flag. When AIE is set to '0', the alarm match only affects the AF flagin Flags register.

**Power Fail Interrupt Enable - PFE**. When set to '1', the power fail monitor drives the pin and an internal flag. When PFE is set to '0', the power fail monitor only affects the PF flag in Flags register.

**High/Low - H/L**. When set to a '1', the INT pin is active HIGH and the driver mode is push pull. The INT pin drives high only when $V_{CC}$ is greater than $V_{SWITCH}$. When set to a '0', the INT pin is active LOW and the drive mode is open drain. Active LOW (open drain) is operational even in battery backup mode.

**Pulse/Level - P/L**. When set to a '1' and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a '0', the INT pin is driven high or low (determined by H/L) until the Flags or Control register is read.

When an enabled interrupt source activates the INT pin, an external host reads the Flags registers to determine the cause. Remember that all flags are cleared when the register is read. If the INT pin is programmed for Level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the Flags register is read. If the INT pin is used as a host reset, then the Flags or Control register is not read during a reset.

### Flags Register

The Flag register has three flag bits: WDF, AF, and PF, which can be used to generate an interrupt. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts to be informed when a flag is set. These flags are automatically reset once the register is read. The flags register is automatically loaded with the value 00h on power up (except for the OSCF bit. See "Stopping and Starting the Oscillator" on page 7.)

**Figure 5. Interrupt Block Diagram**

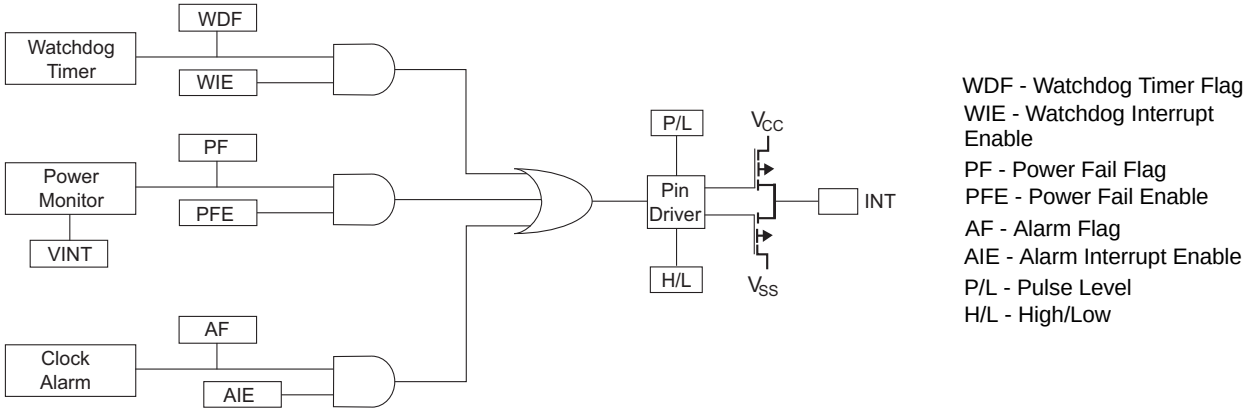
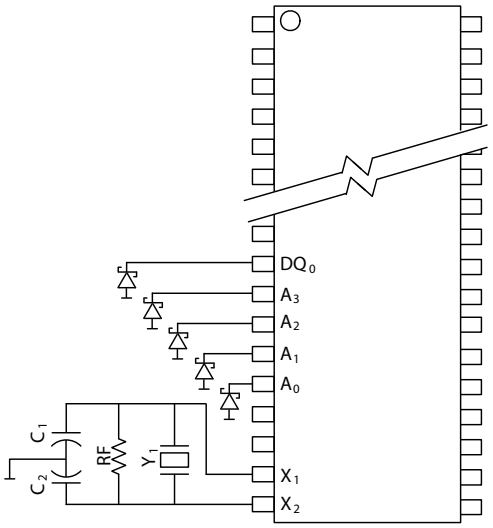



**Figure 6. RTC Recommended Component Configuration**




Recommended Values:
Y1 = 32.768KHz
RF = 10M Ohm
C1 = 0 (install cap footprint, but leave unloaded)
C2 = 56 pF ± 10% (do not vary from this value)

**Note**
4. Schottky diodes, ($V_F$ < 0.4V with $I_F$ at 100mA) are recommended at pins $A_0$ - $A_3$ and $DQ_0$ in applications where undershoot exceeds -0.5V. Please see application note AN49947 for further details.

**Table 3. RTC Register Map**[5, 6]

| Register | BCD Format Data [5] | | | | | | | | Function/Range |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0x7FFF | 10s Years | | | | Years | | | | Years: 00–99 |
| 0x7FFE | 0 | 0 | 0 | 10s Months | Months | | | | Months: 01–12 |
| 0x7FFD | 0 | 0 | 10s Day of Month | | Day Of Month | | | | Day of Month: 01–31 |
| 0x7FFC | 0 | 0 | 0 | 0 | 0 | Day of Week | | | Day of Week: 01–07 |
| 0x7FFB | 0 | 0 | 10s Hours | | Hours | | | | Hours: 00–23 |
| 0x7FFA | 0 | 10s Minutes | | | Minutes | | | | Minutes: 00–59 |
| 0x7FF9 | 0 | 10s Seconds | | | Seconds | | | | Seconds: 00–59 |
| 0x7FF8 | OSCEN (0) | 0 | Cal Sign (0) | Calibration (00000) | | | | | Calibration Values [7] |
| 0x7FF7 | WDS (0) | WDW (0) | WDT (000000) | | | | | | Watchdog [7] |
| 0x7FF6 | WIE (0) | AIE (0) | PFE (0) | 0 | H/L (1) | P/L (0) | 0 | 0 | Interrupts [7] |
| 0x7FF5 | M (1) | 0 | 10s Alarm Date | | Alarm Day | | | | Alarm, Day of Month: 01–31 |
| 0x7FF4 | M (1) | 0 | 10s Alarm Hours | | Alarm Hours | | | | Alarm, Hours: 00–23 |
| 0x7FF3 | M (1) | 10 Alarm Minutes | | | Alarm Minutes | | | | Alarm, Minutes: 00–59 |
| 0x7FF2 | M (1) | 10 Alarm Seconds | | | Alarm, Seconds | | | | Alarm, Seconds: 00–59 |
| 0x7FF1 | 10s Centuries | | | | Centuries | | | | Centuries: 00–99 |
| 0x7FF0 | WDF | AF | PF | OSCF | 0 | CAL (0) | W (0) | R (0) | Flags [7] |

**Note**
5. ( ) designates values shipped from the factory.
6. The unused bits of RTC registers are reserved for future use and should be set to '0'.
7. Is a binary value, not a BCD value.

**Table 4. Register Map Detail**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **0x7FFF** | **Time Keeping - Years** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 10s Years | | | | Years | | | |
| | Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99. | | | | | | | |
| **0x7FFE** | **Time Keeping - Months** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 0 | 0 | 10s Month | Months | | | |
| | Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12. | | | | | | | |
| **0x7FFD** | **Time Keeping - Date** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 0 | 10s Day of Month | | Day of Month | | | |
| | Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for. | | | | | | | |
| **0x7FFC** | **Time Keeping - Day** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 0 | 0 | 0 | 0 | Day of Week | | |
| | Lower nibble (three bits) contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date. | | | | | | | |
| **0x7FFB** | **Time Keeping - Hours** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 0 | 10s Hours | | Hours | | | |
| | Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23. | | | | | | | |
| **0x7FFA** | **Time Keeping - Minutes** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 10s Minutes | | | Minutes | | | |
| | Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59. | | | | | | | |
| **0x7FF9** | **Time Keeping - Seconds** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 0 | 10s Seconds | | | Seconds | | | |
| | Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0–59. | | | | | | | |

**Table 4. Register Map Detail** (continued)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **0X7FF8** | **Calibration/Control** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | OSCEN | 0 | Calibration Sign | Calibration | | | | |
| OSCEN | Oscillator Enable. When set to 1, the oscillator is stopped. When set to 0, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage. | | | | | | | |
| Calibration Sign | Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base. | | | | | | | |
| Calibration | These five bits control the calibration of the clock. | | | | | | | |
| **0x7FF7** | **WatchDog Timer** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | WDS | WDW | WDT | | | | | |
| WDS | Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a 0. | | | | | | | |
| WDW | Watchdog Write Enable. Setting this bit to 1 disables any WRITE to the watchdog timeout value (D5–D0). This allows the user to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to 0 allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in detail in the "Watchdog Timer" on page 8. | | | | | | | |
| WDT | Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 1) to 2 seconds (setting of 3 Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was set to 0 on a previous cycle. | | | | | | | |
| **0x7FF6** | **Interrupt Status/Control** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | WIE | AIE | PFIE | 0 | H/L | P/L | 0 | 0 |
| WIE | Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag. | | | | | | | |
| AIE | Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin and the AF flag. When set to 0, the alarm match only affects the AF flag. | | | | | | | |
| PFIE | Power Fail Enable. When set to 1, the alarm match drives the INT pin and the PF flag. When set to 0, the power fail monitor affects only the PF flag. | | | | | | | |
| 0 | Reserved for future use | | | | | | | |
| H/L | High/Low. When set to 1, the INT pin is driven active HIGH. When set to 0, the INT pin is open drain, active LOW. | | | | | | | |
| P/L | Pulse/Level. When set to 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to 0, the INT pin is driven to an active level (as set by H/L) until the flags register is read. | | | | | | | |
| **0x7FF5** | **Alarm - Day** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | M | 0 | 10s Alarm Date | | Alarm Date | | | |
| | Contains the alarm value for the date of the month and the mask bit to select or deselect the date value. | | | | | | | |
| M | Match. When this bit is set to 0, the date value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value. | | | | | | | |

**Table 4. Register Map Detail** (continued)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **0x7FF4** | **Alarm - Hours** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | M | 10s Alarm Hours | | | Alarm Hours | | | |
| | Contains the alarm value for the hours and the mask bit to select or deselect the hours value. | | | | | | | |
| M | Match. When this bit is set to 0, the hours value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value. | | | | | | | |
| **0x7FF3** | **Alarm - Minutes** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | M | 10s Alarm Minutes | | | Alarm Minutes | | | |
| | Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value. | | | | | | | |
| M | Match. When this bit is set to 0, the minutes value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minutes value. | | | | | | | |
| **0x7FF2** | **Alarm - Seconds** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | M | 10s Alarm Seconds | | | Alarm Seconds | | | |
| | Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value. | | | | | | | |
| M | Match. When this bit is set to 0, the seconds value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the seconds value. | | | | | | | |
| **0x7FF1** | **Time Keeping - Centuries** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | 10s Centuries | | | | Centuries | | | |
| | Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries. | | | | | | | |
| **0x7FF0** | **Flags** | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | WDF | AF | PF | OSCF | 0 | CAL | W | R |
| WDF | Watchdog Timer Flag. This read only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags register is read or on power-up. | | | | | | | |
| AF | Alarm Flag. This read only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags register is read or on power-up. | | | | | | | |
| PF | Power Fail Flag. This read only bit is set to 1 when power falls below the power fail threshold $V_{SWITCH}$. It is cleared to 0 when the Flags register is read or on power-up. | | | | | | | |
| OSCF | Oscillator Fail Flag. Set to 1 on power up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. The user must reset this bit to 0 to clear this condition (Flag). The chip does not clear this flag. This bit survives power cycles. | | | | | | | |
| CAL | Calibration Mode. When set to 1, a 512 Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up. | | | | | | | |
| W | Write Enable: Setting the W bit to 1 freezes updatesof the RTC registers. The user can then write to RTC registers, Alarm registers, Calibration register, Interrupt register and Flags register. Setting the W bit to 0 causes the contents of the RTC registers to be transferred to the time keeping counters if the time has been changed (a new base time is loaded). This bit defaults to 0 on power up. | | | | | | | |
| R | Read Enable: Setting R bit to 1, stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set R bit to 0 to resume clock updates to the holding register. Setting this bit does not require W bit to be set to 1. This bit defaults to 0 on power up. | | | | | | | |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on $V_{CC}$ Relative to GND ..... –0.5V to 4.1V

Voltage Applied to Outputs in High Z State ..... –0.5V to $V_{CC}$ + 0.5V

Input Voltage ..... –0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to $V_{CC}$ + 2.0V

Package Power Dissipation Capability ($T_A$ = 25°C) ..... 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds) ..... +260°C

DC Output Current (1 output at a time, 1s duration) ... 15 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 2.7V to 3.6V |
| Industrial | –40°C to +85°C | 2.7V to 3.6V |

## DC Electrical Characteristics

Over the Operating Range (VCC = 2.7V to 3.6V) [8, 9]

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Average $V_{CC}$ Current | $t_{RC}$ = 25 ns<br>$t_{RC}$ = 35 ns<br>$t_{RC}$ = 45 ns<br>Dependent on output loading and cycle rate. Values obtained without output loads. $I_{OUT}$ = 0 mA. | Commercial | | 65<br>55<br>50 | mA<br>mA |
| | | | Industrial | | 70<br>60<br>55 | mA<br>mA |
| $I_{CC2}$ | Average $V_{CC}$ Current during STORE | All Inputs Do Not Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | 3 | mA |
| $I_{CC3}$ | Average $V_{CC}$ Current at $t_{AVAV}$ = 200 ns, 3V, 25°C Typical | $\overline{WE} \geq (V_{CC} – 0.2V)$. All other inputs cycling.<br>Dependent on output loading and cycle rate.<br>Values obtained without output loads. | | | 10 | mA |
| $I_{CC4}$ | Average $V_{CAP}$ Current during AutoStore Cycle | All Inputs Do Not Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | 3 | mA |
| $I_{SB}$ | $V_{CC}$ Standby Current | $\overline{WE} \geq (V_{CC} – 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} – 0.2V)$.<br>Standby current level after nonvolatile cycle is complete.<br>Inputs are static. f = 0 MHz. | | | 3 | mA |
| $I_{IX}$ | Input Leakage Current | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$ | | -1 | +1 | µA |
| $I_{OZ}$ | Off State Output Leakage Current | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ | | -1 | +1 | µA |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage | | | $V_{SS}$ – 0.5 | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OUT}$ = –2 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OUT}$ = 4 mA | | | 0.4 | V |
| $V_{CAP}$ | Storage Capacitor | Between $V_{CAP}$ pin and $V_{SS}$, 5V Rated | | 17 | 120 | µF |

**Notes**
8. The $\overline{HSB}$ pin has IOUT = –10 µA for VOH of 2.4V, this parameter is characterized but not tested.
9. The INT pin is open drain and does not source or sink current when Interrupt register bit D3 is low.

## Data Retention and Endurance

| Parameter | Description | Min | Unit |
|---|---|---|---|
| $DATA_R$ | Data Retention | 20 | Years |
| $NV_C$ | Nonvolatile STORE Operations | 200 | K |

## Capacitance

These parameters are guaranteed but not tested.

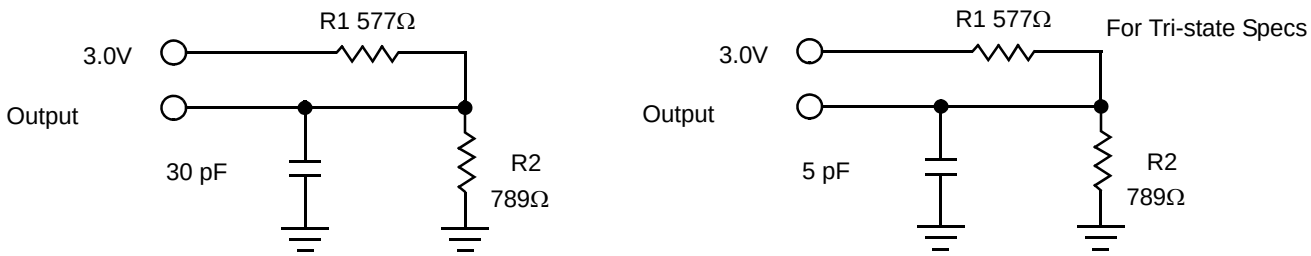
| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 0 to 3.0 V | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

## Thermal Resistance

These parameters are guaranteed but not tested.

| Parameter | Description | Test Conditions | 48-SSOP | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA / JESD51. | 32.9 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 25.56 | °C/W |

**Figure 7. AC Test Loads**




## AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

## AC Switching Characteristics

| Parameter | | Description | 25 ns | | 35 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameter | Alt. Parameter | | Min | Max | Min | Max | Min | Max | |
| **SRAM Read Cycle** | | | | | | | | | |
| $t_{ACE}$ | $t_{ELQV}$ | Chip Enable Access Time | | 25 | | 35 | | 45 | ns |
| $t_{RC}$ [10] | $t_{AVAV}$, $t_{ELEH}$ | Read Cycle Time | 25 | | 35 | | 45 | | ns |
| $t_{AA}$ [11] | $t_{AVQV}$ | Address Access Time | | 25 | | 35 | | 45 | ns |
| $t_{DOE}$ | $t_{GLQV}$ | Output Enable to Data Valid | | 12 | | 15 | | 20 | ns |
| $t_{OHA}$ [11] | $t_{AXQX}$ | Output Hold After Address Change | 3 | | 3 | | 3 | | ns |
| $t_{LZCE}$ [12] | $t_{ELQX}$ | Chip Enable to Output Active | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$ [12] | $t_{EHQZ}$ | Chip Disable to Output Inactive | | 10 | | 13 | | 15 | ns |
| $t_{LZOE}$ [12] | $t_{GLQX}$ | Output Enable to Output Active | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$ [12] | $t_{GHQZ}$ | Output Disable to Output Inactive | | 10 | | 13 | | 15 | ns |
| $t_{PU}$ [13] | $t_{ELICCH}$ | Chip Enable to Power Active | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ [13] | $t_{EHICCL}$ | Chip Disable to Power Standby | | 25 | | 35 | | 45 | ns |

**Figure 8. SRAM Read Cycle 1: Address Controlled** [10, 11, 14]

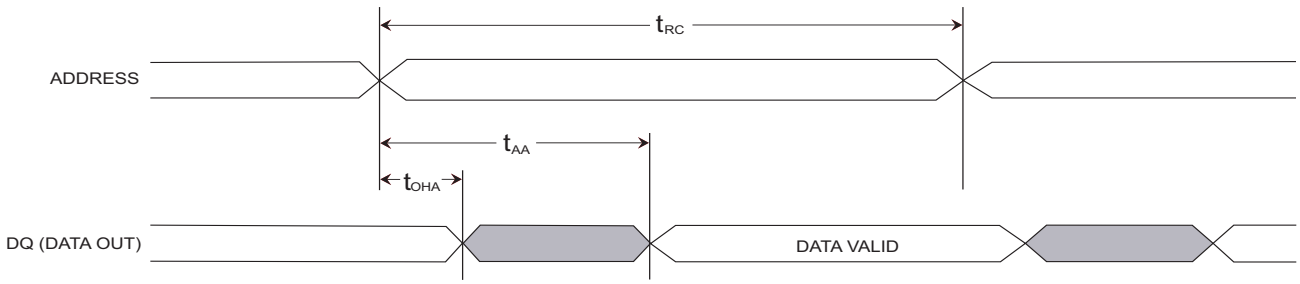
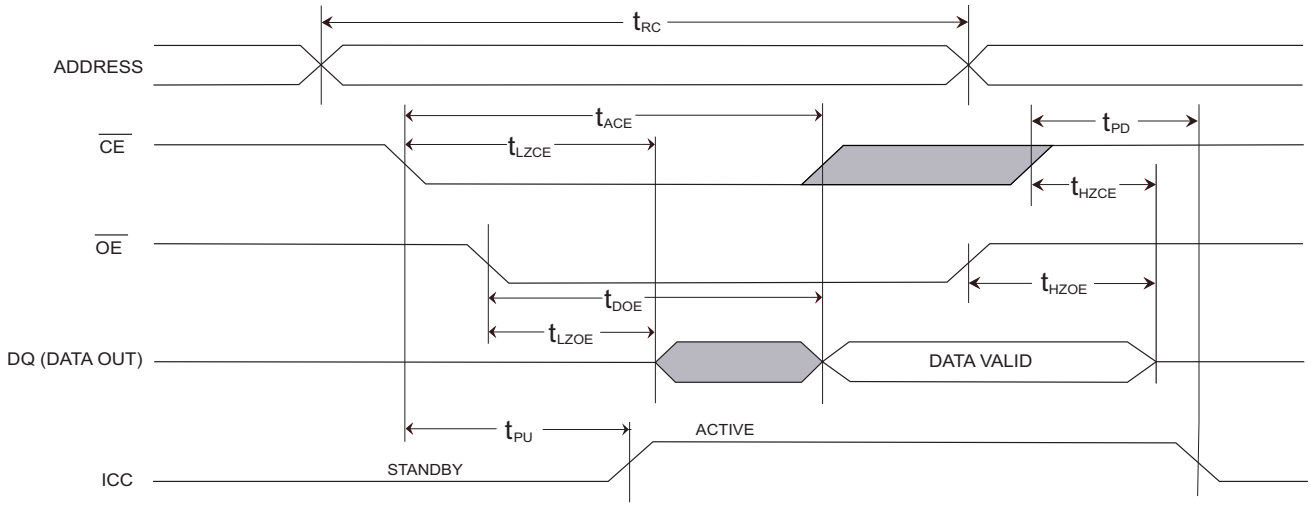



**Figure 9. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled** [10, 14]




**Notes**
10. $\overline{WE}$ is HIGH during SRAM Read Cycles.
11. Device is continuously selected with CE and OE both Low.
12. Measured ±200 mV from steady state output voltage.
13. These parameters are guaranteed by design and are not tested.
14. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

## AC Switching Characteristics (continued)

| Parameter | | Description | 25 ns | | 35 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameter | Alt. Parameter | | Min | Max | Min | Max | Min | Max | |
| **SRAM Write Cycle** | | | | | | | | | |
| $t_{WC}$ | $t_{AVAV}$ | Write Cycle Time | 25 | | 35 | | 45 | | ns |
| $t_{PWE}$ | $t_{WLWH}$, $t_{WLEH}$ | Write Pulse Width | 20 | | 25 | | 30 | | ns |
| $t_{SCE}$ | $t_{ELWH}$, $t_{ELEH}$ | Chip Enable To End of Write | 20 | | 25 | | 30 | | ns |
| $t_{SD}$ | $t_{DVWH}$, $t_{DVEH}$ | Data Setup to End of Write | 10 | | 12 | | 15 | | ns |
| $t_{HD}$ | $t_{WHDX}$, $t_{EHDX}$ | Data Hold After End of Write | 0 | | 0 | | 0 | | ns |
| $t_{AW}$ | $t_{AVWH}$, $t_{AVEH}$ | Address Setup to End of Write | 20 | | 25 | | 30 | | ns |
| $t_{SA}$ | $t_{AVWL}$, $t_{AVEL}$ | Address Setup to Start of Write | 0 | | 0 | | 0 | | ns |
| $t_{HA}$ | $t_{WHAX}$, $t_{EHAX}$ | Address Hold After End of Write | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$ [12, 15] | $t_{WLQZ}$ | Write Enable to Output Disable | | 10 | | 13 | | 15 | ns |
| $t_{LZWE}$ [12] | $t_{WHQX}$ | Output Active After End of Write | 3 | | 3 | | 3 | | ns |

**Figure 10. SRAM Write Cycle 1: $\overline{WE}$ Controlled** [14, 16]

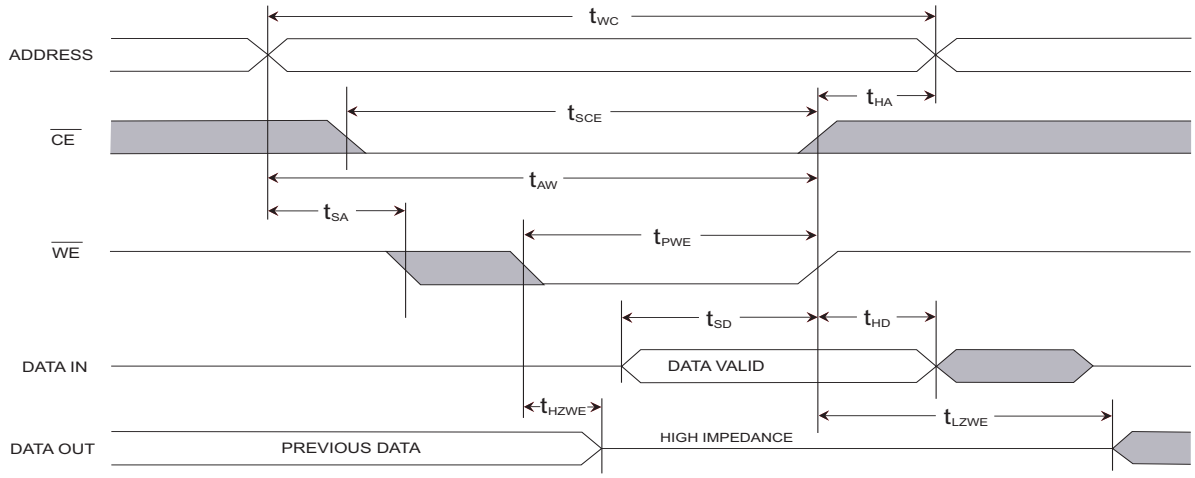
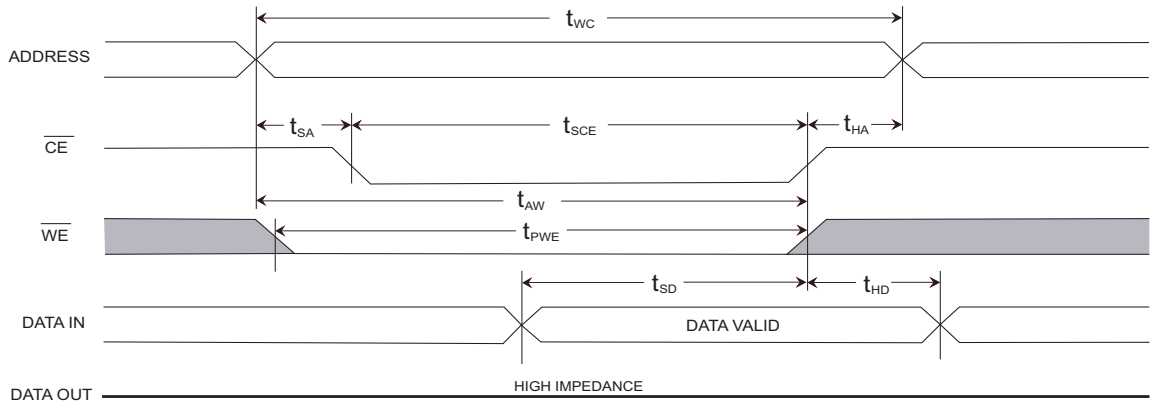



**Figure 11. SRAM Write Cycle 2: $\overline{CE}$ Controlled**

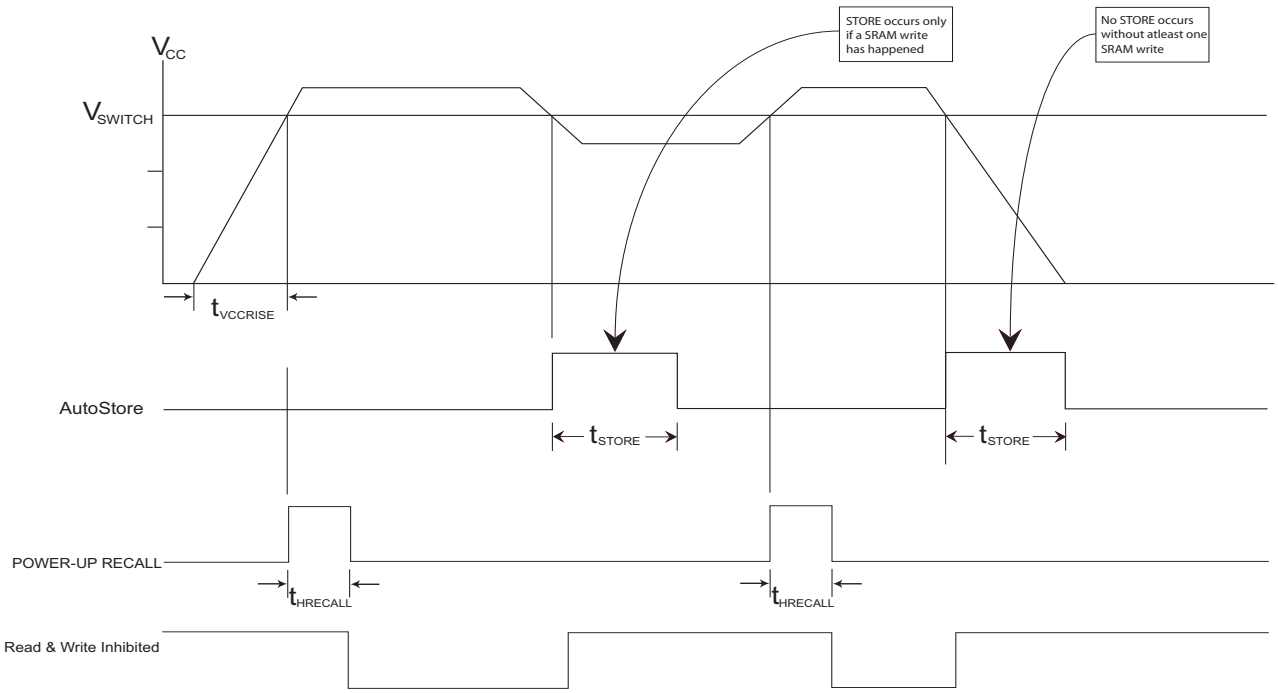



**Notes**
15. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the High Impedance State.
16. $\overline{CE}$ or $\overline{WE}$ are greater than $V_{IH}$ during address transitions.

## AutoStore or Power Up RECALL

| Parameter | Description | | CY14B256K | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{HRECALL}$ [17] | Power Up RECALL Duration | | | 40 | ms |
| $t_{STORE}$ [18, 19] | STORE Cycle Duration | Commercial | | 12.5 | ms |
| | | Industrial | | 15 | ms |
| $V_{SWITCH}$ | Low Voltage Trigger Level | | | 2.65 | V |
| $t_{VCCRISE}$ | VCC Rise Time | | 150 | | µs |

**Figure 12. AutoStore/Power Up RECALL**




**Notes**
17. $t_{HRECALL}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.
18. If an SRAM Write does not taken place since the last nonvolatile cycle, no STORE takes place.
19. Industrial Grade Devices require 15 ms Max.

## Software Controlled STORE/RECALL Cycles [20, 21]

| Parameter | Alt. Parameter | Description | 25 ns | | 35 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | $t_{AVAV}$ | STORE/RECALL Initiation Cycle Time | 25 | | 35 | | 45 | | ns |
| $t_{SA}$ | $t_{AVEL}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{CW}$ | $t_{ELEH}$ | Clock Pulse Width | 20 | | 25 | | 30 | | ns |
| $t_{HA}$ | $t_{EHAX}$ | Address Hold Time | 1 | | 1 | | 1 | | ns |
| $t_{RECALL}$ | | RECALL Duration | | 170 | | 170 | | 170 | µs |

**Figure 13. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [21]**

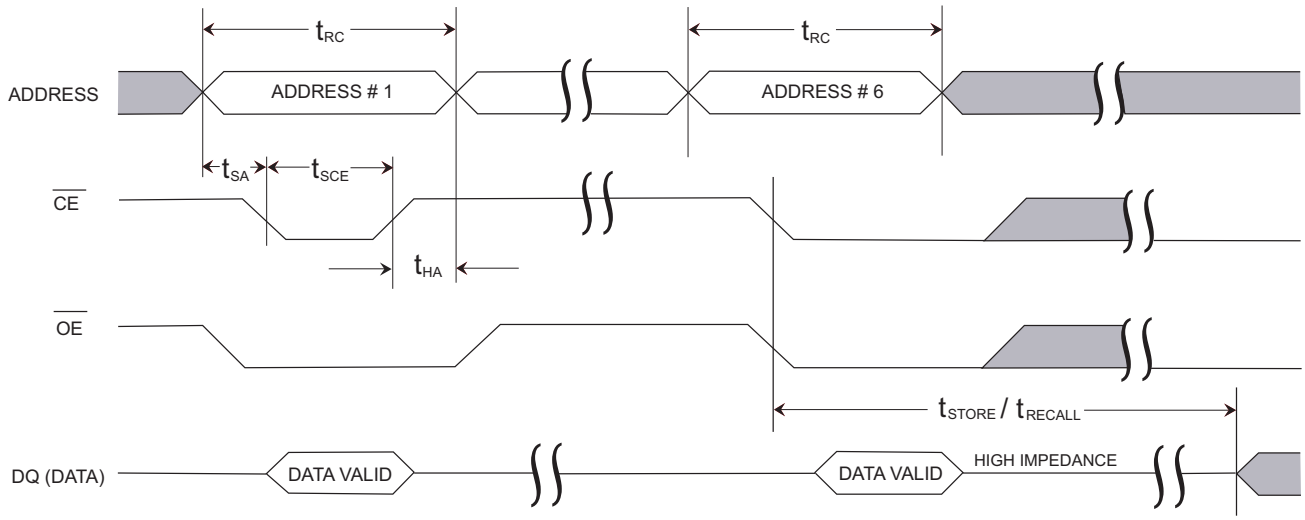
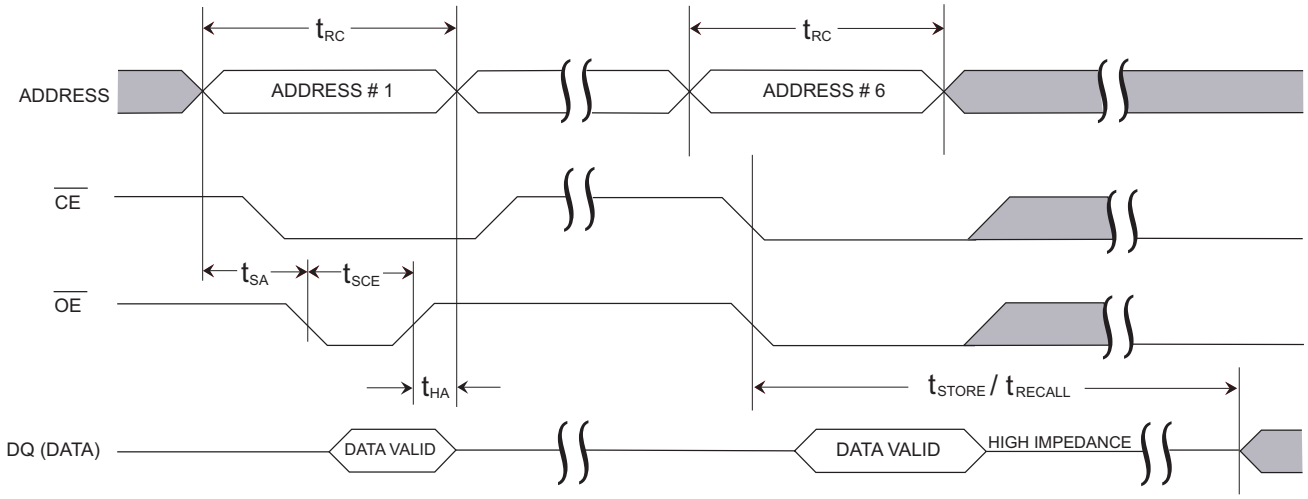



**Figure 14. $\overline{OE}$ Controlled Software STORE/RECALL Cycle [21]**

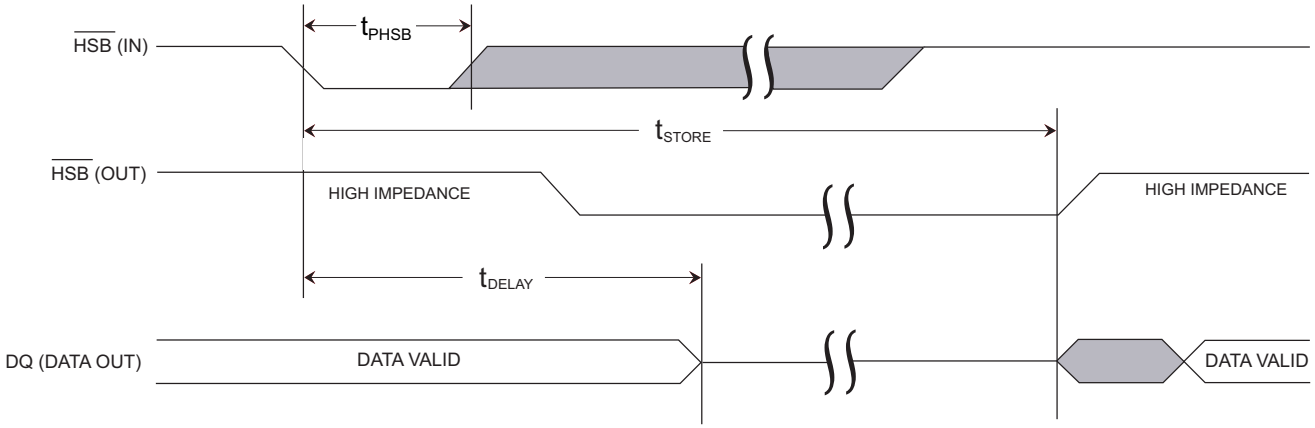



**Notes**
20. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled READs.
21. The six consecutive addresses are read in the order listed in the Mode Selection on page 6. $\overline{WE}$ is HIGH during all six consecutive cycles.

## Hardware STORE Cycle

| Parameter | Alt. Parameter | Description | CY14B256K | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{DELAY}$ [22] | | Time Allowed to Complete SRAM Cycle | 1 | 70 | µs |
| $t_{PHSB}$ | $t_{HLHX}$ | Hardware STORE Pulse Width | 15 | | ns |

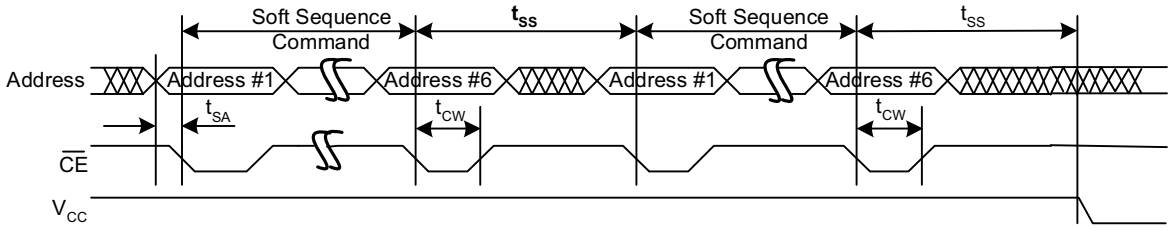
**Figure 15. Hardware STORE Cycle**




## Soft Sequence Commands

| Parameter | Description | CY14B256K | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{SS}$ [23, 24] | Soft Sequence Processing Time | | 70 | µs |

**Figure 16. Soft Sequence Processing** [23, 24]




**Notes**
22. Read and Write cycles in progress before HSB are given this amount of time to complete.
23. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
24. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See specific command.

## RTC Characteristics

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{BAK}$ [25] | RTC Backup Current | | Commercial | | 300 | nA |
| | | | Industrial | | 350 | nA |
| $V_{RTCbat}$ [26] | RTC Battery Pin Voltage | | | 1.8 | 3.3 | V |
| $V_{RTCcap}$ [27] | RTC Capacitor Pin Voltage | | | 1.2 | 2.7 | V |
| tOCS | RTC Oscillator Time to Start | At Min Temperature from Power up or Enable | | | 10 | sec |
| | | At 25°C Temperature from Power up or Enable | | | 5 | sec |

## Truth Table For SRAM Operations

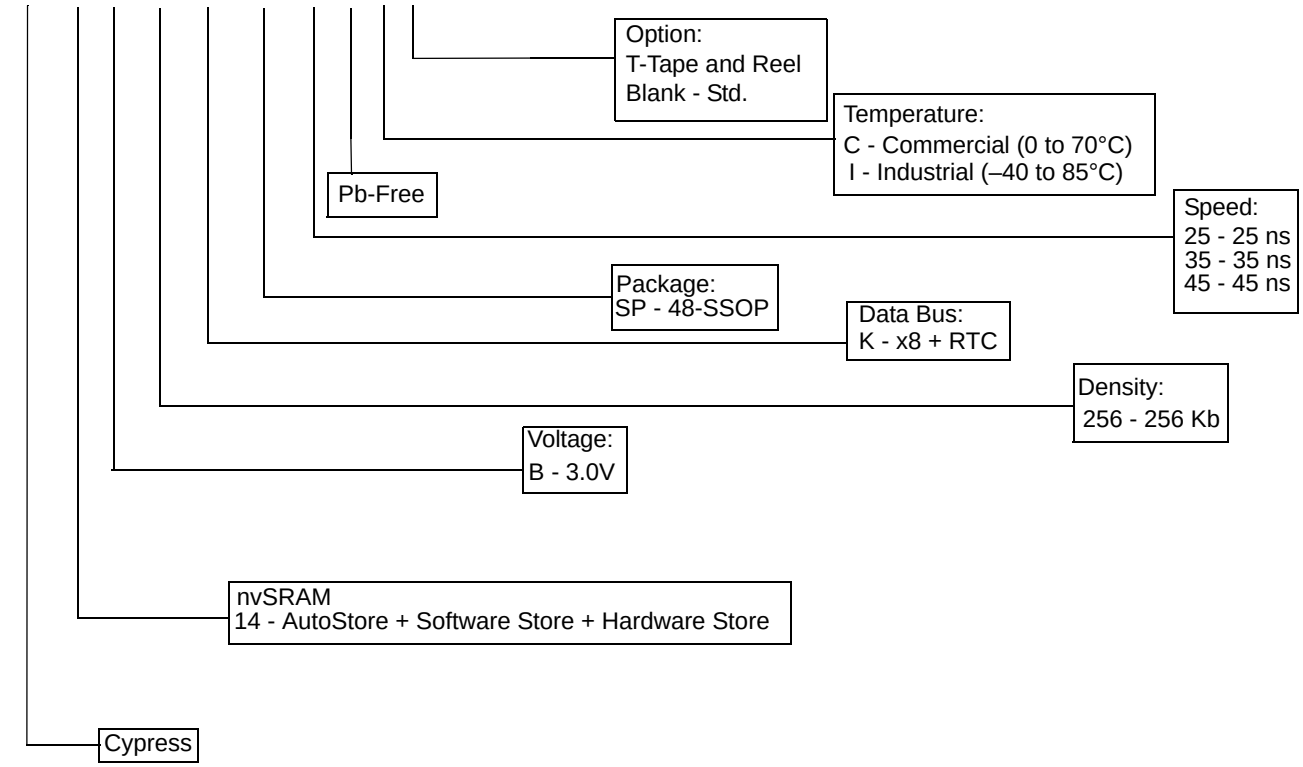
$\overline{HSB}$ should remain HIGH for SRAM Operations.

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs and Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power down | Standby |
| L | H | L | Data Out ($DQ_0$–$DQ_7$); | Read | Active |
| L | H | H | High Z | Output Disabled | Active |
| L | L | X | Data in ($DQ_0$–$DQ_7$); | Write | Active |

**Notes**
25. From either $V_{RTCcap}$ or $V_{RTCbat}$.
26. Typical = 3.0V during normal operation.
27. Typical = 2.4V during normal operation.

## Part Numbering Nomenclature

**CY 14 B 256 K - SP 25 X C T**



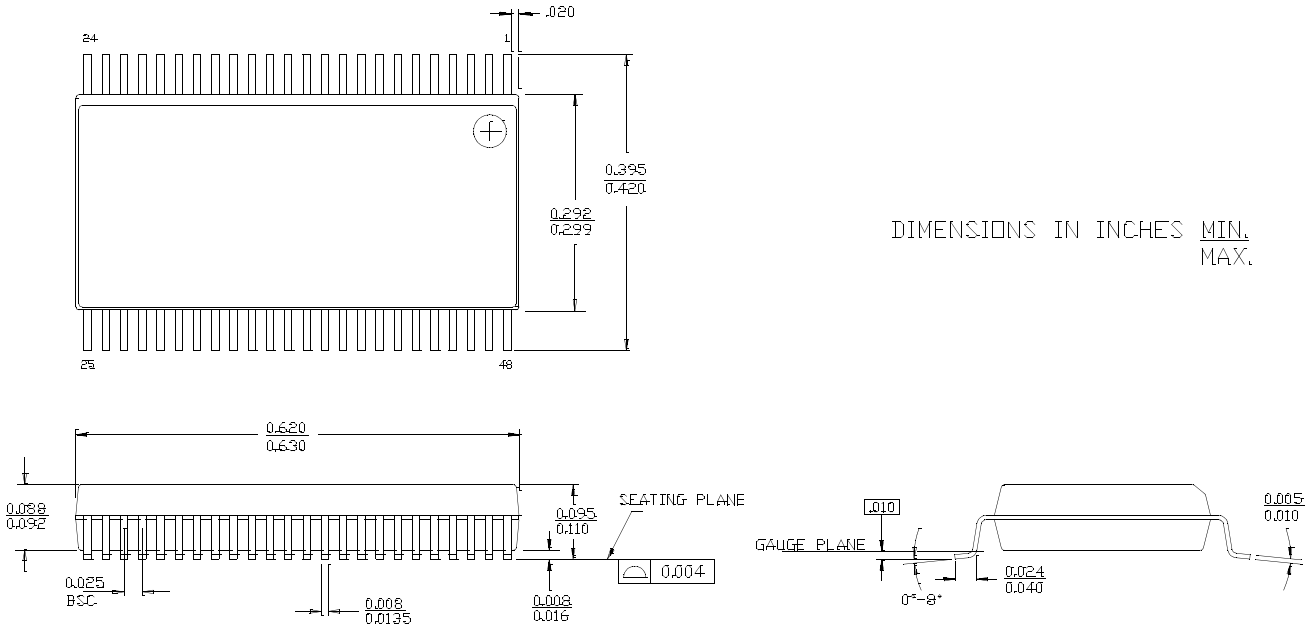
## Ordering Information

All the below mentioned parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 25 | CY14B256K-SP25XC | 51-85061 | 48-pin SSOP | Commercial |
| | CY14B256K-SP25XCT | | | |
| | CY14B256K-SP25XI | 51-85061 | 48-pin SSOP | Industrial |
| | CY14B256K-SP25XIT | | | |
| 35 | CY14B256K-SP35XC | 51-85061 | 48-pin SSOP | Commercial |
| | CY14B256K-SP35XCT | | | |
| | CY14B256K-SP35XI | 51-85061 | 48-pin SSOP | Industrial |
| | CY14B256K-SP35XIT | | | |
| 45 | CY14B256K-SP45XC | 51-85061 | 48-pin SSOP | Commercial |
| | CY14B256K-SP45XCT | | | |
| | CY14B256K-SP45XI | 51-85061 | 48-pin SSOP | Industrial |
| | CY14B256K-SP45XIT | | | |

## Package Diagrams

**Figure 17. 48-Pin Shrunk Small Outline Package (51-85061)**



## Document History Page

| Document Title: CY14B256K 256 Kbit (32K x 8) nvSRAM with Real Time Clock<br>Document Number: 001-06431 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 425138 | TUP | See ECN | New data sheet |
| *A | 437321 | TUP | See ECN | Show data sheet on external Web |
| *B | 471966 | TUP | See ECN | Changed $V_{IH(min)}$ from 2.2V to 2.0V<br>Changed $t_{RECALL}$ from 60 µs to 100 µs<br>Changed Endurance from one million cycles to 500K cycles<br>Changed Data Retention from 100 years to 20 years<br>Added Soft Sequence Processing Time Waveform<br>Updated Part Numbering Nomenclature and Ordering Information<br>Added RTC Characteristics Table<br>Added RTC Recommended Component Configuration |
| *C | 503277 | PCI | See ECN | Changed from “Advance” to “Preliminary”<br>Changed the term “Unlimited” to “Infinite”<br>Changed endurance from 500K cycles to 200K cycles<br>Device operation: Tolerance limit changed from +20% to +15% in the<br>Features Section and Operating Range Table<br>Removed Icc1 values from the DC table for 25 ns and 35 ns industrial grade<br>Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V<br>Added temperature specifications to data retention - 20 years at 55°C<br>Updated Part Nomenclature Table and Ordering Information Table |
| *D | 597004 | TUP | See ECN | Removed $V_{SWITCH(min)}$ specification from AutoStore/Power Up RECALL table<br>Changed $t_{GLAX}$ specification from 20 ns to 1 ns<br>Added $t_{DELAY(max)}$ specification of 70 µs in the Hardware STORE Cycle table<br>Removed $t_{HLBL}$ specification<br>Changed $t_{SS}$ specification from 70 µs(min) to 70 µs(max)<br>Changed $V_{CAP(max)}$ from 57 µF to 120 µF |
| *E | 696097 | VKN | See ECN | Added footnote 7 related to $\overline{HSB}$<br>Added footnote 8 related to INT pin<br>Changed $t_{GLAX}$ to $t_{GHAX}$<br>Removed ABE bit from Interrupt register |
| *F | 1349963 | UHA/SFV | See ECN | Changed from Preliminary to Final<br>Added Note 5 regarding the W bit in the Flag register<br>Updated Ordering Information Table |
| *G | 2483006 | GVCH/PYRS | 05/05/08 | Changed tolerance from +15%, -10% to +20%, -10%<br>Changed Operating voltage range from 2.7V-3.45V to 2.7V-3.6V |

| Document Title: CY14B256K 256 Kbit (32K x 8) nvSRAM with Real Time Clock<br>Document Number: 001-06431 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *H | 2663934 | GVCH/PYRS | 02/24/09 | Updated Features section<br>Updated pin definition of $\overline{WE}$ pin<br>Updated “Reading the clock”, “Backup Power”, “Stopping and starting the Oscillator” and “Alarm” descriptions under RTC operation<br>Modified “Figure 4. RTC Recommended Component Configuration”<br>Added footnote 4<br>Added footnote 6<br>Added default values to RTC Register Map” table<br>Updated flag register description in Register Map Detail” table<br>Added Industrial specs for 25ns and 35ns speed<br>Changed $V_{IH}$ from vcc+0.3 to Vcc+0.5<br>Added “Data Retention and Endurance” table on page 15<br>Added thermal resistance values<br>Added alternate parameters in the AC switching characteristics table<br>Renamed $t_{OH}$ to $t_{OHA}$<br>Changed $t_{HRECALL}$ from 20 to 40ms<br>Changed $t_{RECALL}$ spec from 100µs to 170µs (Including $t_{ss}$ of 70us)<br>Renamed $t_{AS}$ to $t_{SA}$<br>Renamed $t_{GHAX}$ to $t_{HA}$<br>Renamed $t_{HLHX}$ to $t_{PHSB}$<br>Updated Figure 16<br>Added truth table for SRAM operations |

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