E-14

Hardware Technical Reference

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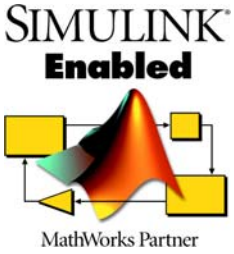
Product Overview:

The Pico families of product are revolutionary embedded platforms. With performance that often exceeds modern microcomputers, a shockingly small form factor, and nominal power consumption that is less than one watt, the Pico family of products takes computing to a whole new level.

The Pico E-14 is based on the revolutionary Virtex-4 chip. This device has the performance and power consumption of a custom chip (ASIC), but is completely reconfigurable! The Pico E-14 EP (Embedded Processor) can be configured with either the FX20 FX40 or FX60 Virtex 4 FPGA.

Advanced users will enjoy the open source development kits that allow absolute control over the hardware. Those who desire a high level programming environment can use Simulink® to implement custom algorithms in hardware with just the click of a button. Impulse C™ support is also included for rapid firmware development in the C programming language. Board support packages are available for operating systems such as Linux or µC/OS.



Pico E-14 EP Quick Reference Datasheet

Core Technologies

- Virtex-4 FPGA
- PowerPC-405 450 MHz (680 DMIPS)
- 256 MB RAM
- 64 MB FPGA Image Flash
- Analog to Digital and Digital to Analog Converters
- Gigabit Ethernet (1000/100/10 Mbps)
- 2 RS-232 Serial Ports
- JTAG Hardware / Software Debugging
- 54-bit High Speed Digital I/O Bus
- 16-bit external digital I/O port
- Standalone operation
- JTAG hardware / software debugging
- Open source

Mechanical Specification

- Cardbus Type II
- Stainless Steel Case
- Temperature Range: 0C to +85C

FPGA Performance

- DES > 16 Gbps / 250M Keys / second
- RC4 > 10 Gbps / 12M Keys / second
- > 16 Billion Multiply and Accumulates / second

Typical Applications

- Application on Card (AOC) systems. Vendors sell their applications packaged with the platform that they run on.
- Hybrid embedded processor / DSP applications
- Encryption / decryption
- Security algorithms and testing
- Software radio component
- Embedded control systems
- Embedded web servers / applications
- Weight and size constrained environments such as UAVs, surveillance systems and environmental monitoring devices.
- Complete development environment for laptop computers. Ideal for rapid prototyping and classroom environments.

Analog Capabilities

- 1 High Speed Analog to Digital
  - 8 Bit @ 105MS/Sec
  - 10 Bit @ 80MS/Sec
- 1 High Speed Digital to Analog
  - 8 Bit @ 210MS/Sec
  - 10 Bit @ 165MS/Sec

Features

- Complete Cardbus host interface capable of bus speeds up to 1 Gbps
- DSP capability of the Virtex-4 FPGA
- Bus interface re-configurable to fit other bus nterface protocols
- Works with Xilinx standard tool set (ISE, EDK, and Platform SDK)
- Works with Starbridge Systems' Viva, a graphical development and modeling tool set designed for parallel computing and IP portability
- Pico Flash utility for FPGA image and software executable management. Runs on Windows, Linux, and Apple Hosts
- Available plug-in for Matlab
- Pico DSP Accelerator / Xilinx System Generator plug-in for Simulink available
- Available complete board support packages for PowerPC embedded computing with Xilinx EDK
- Available port of RTCA DO-178B compliant UCOS-II deterministic / pre-emptive kernel
- Available Linux port
- Available port of Green Hills Integrity RTOS
- Dynamic image swapping: unique design allows for many FPGA images and user software images to be stored on the PICO E-14's flash memory at one time. FPGA and software images are associated (paired). This allows image sets to be swapped dynamically. Applications can store data in SDRAM. This data can then be used by subsequent image sets seamlessly.

Pico E-14 Electrical Specifications

	Minimum	Nominal	Maximum
DC Input Voltage	3.15V	3.3-5.0V	5.5V
Power Consumption			10W*
Recommended Temperature Range	0°C	10°C	70°C
Maximum Allowable Temperature Range	0°C		85°C
Continuous Storage Temperature Range	-50°C	30°C	125°C
Relative Humidity (Non-Condensing)	0%		95%

Note: If the card draws more than 10 watts the power supplies cut off and reset the card

Power Consumption

The graph below has power consumption running Pico Computing's primary boot. The primary boot has everything running on the card, except D/A, A/D, and Ethernet. The lower chart has power consumption numbers for primary boot image with 10/100 and GigaBit ethernet running.

Without Ethernet

	Voltage (V)	Current (A)	Power (W)
FX 20	3.3	0.7	2.31
FX 60	3.3	0.8	2.64

With 10/100 Ethernet

	Voltage (V)	Current (A)	Power (W)
FX 20	3.3	0.8	2.64
FX 60	3.3	1.0	3.3

With GigaBit Ethernet

	Voltage (V)	Current (A)	Power (W)
FX 20	3.3	1.0	3.3
FX 60	3.3	1.3	4.3

NOTE: The CardBus slot is rated to 3.3W, and because of the higher power requirement of the FX 60, we do not recommend running the FX 60 in the laptop.

System Architecture

At the core of the Pico E-14 is a Virtex-4 FPGA. The FPGA can be dynamically configured to perform any number of specialized tasks such as: protocol processing, encryption, or complex mathematical functions. Embedded systems benefit from the integrated Power-PC™ processor available on the EP series cards.

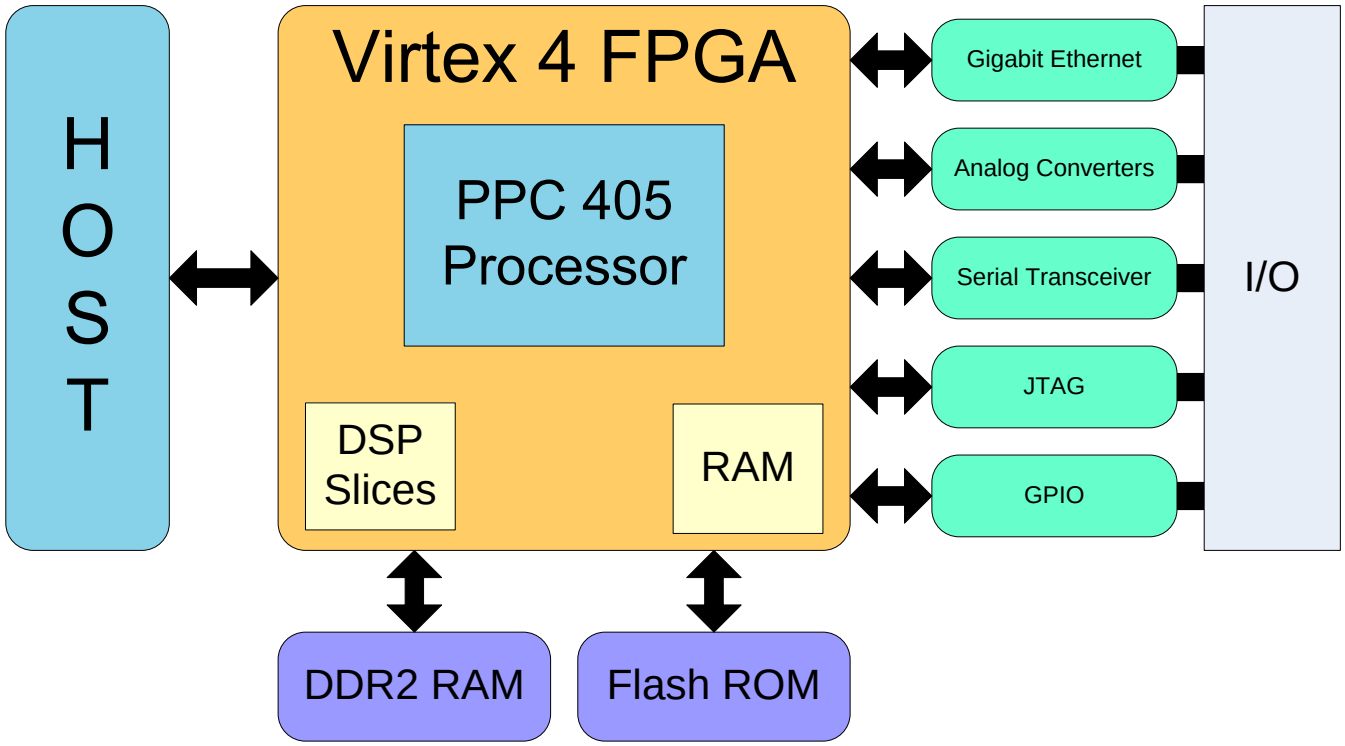


Figure 1

Field Programmable Gate Array

The core of the Pico E-14 is a high performance Virtex-4 FPGA. Included in the FPGA are the FPGA Fabric, a Power-PC ™ processor, ultra high-speed DSP slices and DDR2 RAM.

FPGA Fabric:

The "Fabric" of an FPGA comprises an array of logic elements that can be connected in virtually unlimited patterns. These patterns of logic elements can be used to perform basic mathematical functions such as addition and subtraction, or can be grouped together to perform complex functions like Fast Fourier Transforms. Logic elements can even be connected to create a custom soft processor.

The advantage of the FPGA is that the internal logic can be optimized for a specific application. FPGAs are also able to execute operations in parallel, not being limited by sequential execution like a traditional processor. FPGA operations can be executed in a parallel, pipelined or even an asynchronous manner. The FPGA allows incredible application speed with very low power consumption. Your imagination is really the limit.

DSP Slice:

Embedded within the FPGA are special areas that are designed to facilitate high speed "digital signal processing." These areas are called DSP slices. The DSP slice can be configured in a variety of different ways. For example one DSP slice can be configured to be one tap of an FIR filter. DSP slices are fully pipelined and feature incredible speed. When configured for FIR filtering the DSP slice has a guaranteed performance of 500MHz with a latency of one cycle. An 18x18 multiply and accumulate also runs at 250MHz with a latency of two cycles. Smaller data widths allow higher clock speeds.

FPGA Resources:

Free FPGA Cores	www.opencores.org	repository of free, open source IP cores OPENCORES.ORG
Virtex-4 Website	www.xilinx.com/virtex4	

PowerPC™ Processor

PPC405x3 Processor Introduction:

FPGAs are renowned for their ability to process parallel logic, but they typically have a hard time emulating a high performance processor. To get the best of both worlds the Virtex-4™ features an embedded Power PC Processor. Since the processor shares the same die as the FPGA it seamlessly interfaces with the FPGA fabric.

A new feature of the Vitex-4 FPGA is the addition of an auxiliary processor interface. The APU is the highest speed interface between the Power-PC™ processor and the FPGA fabric. Up to four custom instructions may be implemented in the FPGA, which are accessible from the Power-PC™.

Board support packages are currently available for µC/OS, Linux and Integrity. Board support source code is available open source under the GPL.

CPLD TurboLoader

A CPLD (Complex Programmable Logic Device) is a smaller version of an FPGA (described above) with permanent Flash storage built in. The Pico E-14 contains one CPLD that loads and reconfigures the FPGA. The Pico firmware guide describes how to access the CPLD Image Manager.

CPLD Resources:

Xilinx CPLD Website	www.xilinx.com/cpld

Tri-Mode Ethernet Interface

The Pico E-14 features the Marvell Alaska series 88E1111 tri-mode Ethernet transceiver. On EP series parts the MAC (Middle access controller) is implemented on the FPGA die. On LO series parts the MAC must be implemented in firmware. Communication between the MAC and PHY takes place over an industry standard MII/GMII interface.

The Ethernet transceiver features 10/100/1000 full/half duplex operation. It will automatically configure the physical interface on the fly for crossover or straight through operation. The PHY can even automatically correct for common wiring mistakes. The PHY has a built in Time Domain Reflectometer that can diagnose cable problems and pinpoint their distance away from the transceiver.

In contrast to the Pico E-12, the Ethernet interface on the Pico E-14 is magnetically isolated allowing direct connections to an industry standard hub or switch.

The Marvell 88E1111 is the only chip on the Pico E-14 that requires an NDA for access to the datasheets. If you are interested in some of the advanced features not supported by the native driver, contact Pico Computing for assistance in obtaining an NDA from Marvell. Users are warned not to contact Marvell directly.

Ethernet Resources:

Marvell 88E1111 Webpage	http://www.marvell.com/products/transceivers/singleport/88e1111.jsp

Flash Memory

The Pico E-14 comes equipped with at least 64 megabytes of Flash ROM. The Flash ROM is divided into 512 sectors that can be erased independently. Most of the space on the ROM is reserved for the user.

The Flash ROM's address bus can be controlled by either the TurboLoader or the FPGA, but not both. During power-up or reboot, the TurboLoader is in control of the Flash ROM Address bus. At all other times the FPGA is in control of the address bus.

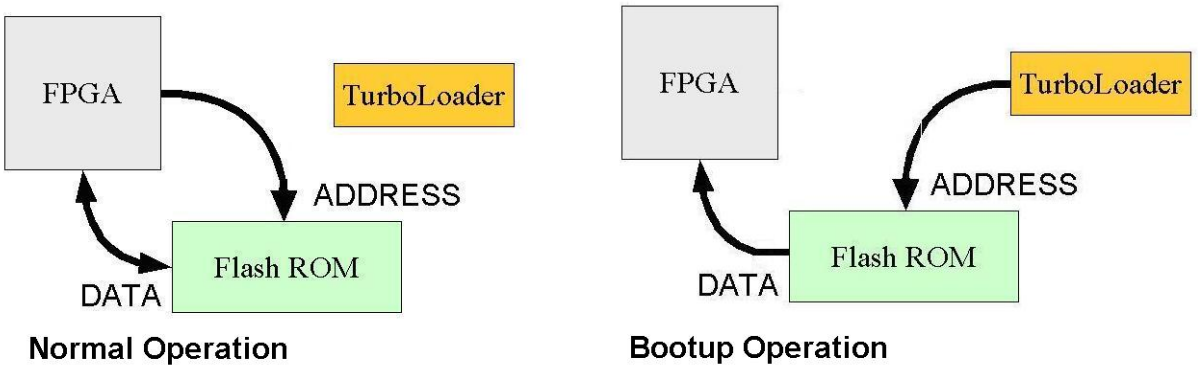


Figure 2

Typical Flash ROM Allocation Table:

Byte addresses	Description	Flash Sectors
0x00000000-0x0000FFFF	Tuple Data and configuration management	0
0x00010000-0x0006FFFF	Primary FPGA Image	1-6
0x000A0000-0x000FFFFF	Backup FPGA Image	7-12
0x000D0000-0x0012FFFF	Secondary Image including boot loader	13-19
0x00140000-0x01FFFFFF	Other FPGA images, executables and data files	20-511

The Flash ROM has a simple, open file system that allows the user to store FPGA images, ELF binary files, or other data. The primary image is used to boot the FPGA initially, and the backup image is only invoked if the primary image fails to load correctly. Executable files are in ELF format and are loaded by a loader within the secondary image. The primary image can either load the secondary image or pause for the PC to access and manage the file system.

DDR2 Memory

The Pico E-14 comes equipped with 256 MB of PC-266 DDR2 memory. There are four 256Mb chips each with 16 bit data paths that are grouped into two 32 bit banks. From 0°C to +95°C, the ram can run at 266 MHz. For operation at temperatures below 0°C, special firmware with reduced ram timings is required. The temperature compensated self-refresh mode must be disabled below -20°C.

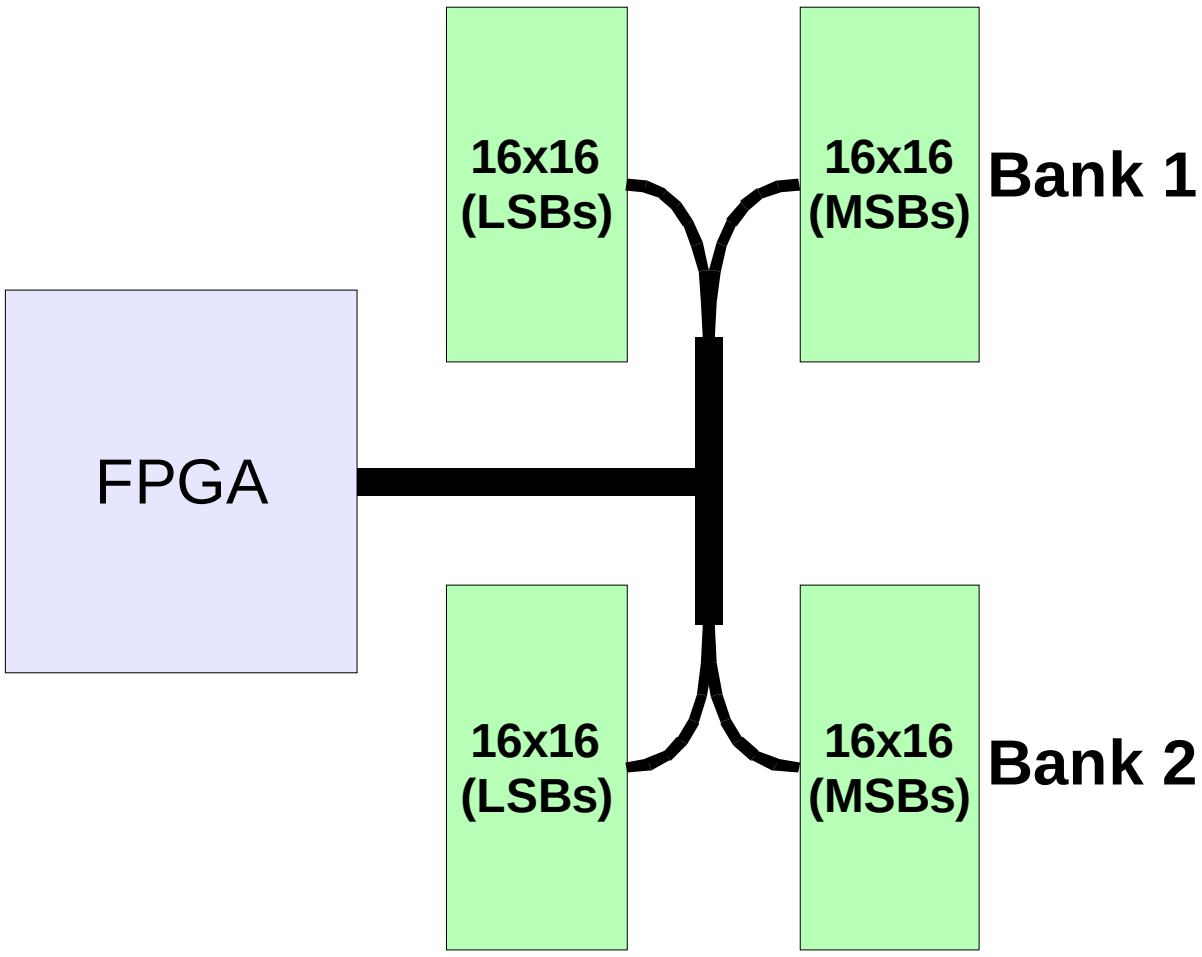


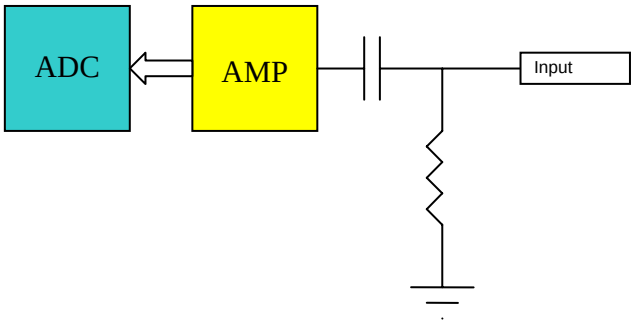
Figure 3

Analog Interface (Optional)

The Pico E-14 also comes equipped with two high-speed analog converters each capable of 14-bit resolution. By default, both analog converters are powered down until the sleep lines are driven low and the amplifier lines are driven high by the FPGA. Both converters are capacitively coupled with pull-down resistors on the output to filter out any DC signal components. Both amplifiers are configured for minimum noise and unity gain.

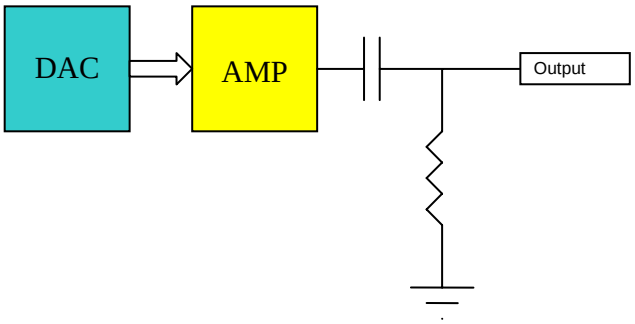
8-Bit, 80 MSPS Analog-to-Digital Converter (ADC)*

The ADC is configured to utilize the internal 1.0V reference voltage and maximum full scale input, giving it a 2V pk-pk input. Currently, the ADC is setup to accept input voltages between 0V and 2V. Clock modes and input data format is set by the system utilizing configuration pins available to the FPGA.



8-Bit, 165 MSPS Digital-to-Analog Converter (DAC)*

The DAC is configured to utilize the internal 1.2V reference voltage and maximum full-scale output, giving it a 2V pk-pk output. Since the DAC actually outputs complementary currents, the amplifier is also utilized as a current to voltage converter and voltage shifter. This allows the voltage to be buffered within the 0V to 3V rail voltages. Currently, the DAC is setup to output between .5V and 2.5V. This gives us a comfortable .5V between our maximum outputs and rail voltages. Clock modes and input data format is set by the system utilizing configuration pins available to the FPGA.



*Please refer to the Analog Interface Selection Guide in Appendix E for compatible 8-12-bit converters

RS-232 Serial Transceiver

The Pico E-14 contains one asynchronous RS-232 serial transceiver that also meets EIA/TIA-232 and V.28/V.24 specifications at a maximum data rate of 250kBps. Because the serial transceiver is directly connected to the FPGA any bit high-level protocol can be implemented in logic. Pico Computing supports various asynchronous, synchronous and military serial protocols.

RS-232 is the most common physical layer protocol for serial data. It is the standard used on serial mice for computers, modems, consumer GPS receivers and even some military radios. Only one wire is needed to send a signal on an RS-232 link. A total of two devices are allowed on a single RS-232 link.

In addition, there are two possible logic states on an RS-232 line (high and low). The high voltage is positive and the low voltage is negative.

Physical Layer Specifications:

Standard	Noise Immunity	Max Distance	Max Speed	Max Connections
RS-232	Satisfactory	50ft	250 kBps*	1 Tx / 1 Rx

*Maximum speed decreases with increased cable length.
*The old RS-232, 422 and 485 standards are now obsolete and have been replaced by EIA/TIA-232, 422 and 485.

Serial Transceiver Specifications:

Maximum Continuous Positive Input Voltage	+25 VDC
Maximum Continuous Negative Input Voltage	-25 VDC
ESD Protection Limit	+/-15,000V
Maximum Short Circuit Duration on Output	Infinite
Typical RS-232 Output Voltage	+/- 5.4 V
RS-232 Maximum Low Input Threshold*	1.2 V
RS-232 Minimum High Input Threshold	1.5 V

*RS-232 Receivers can accept digital inputs

Digital Peripheral Interface

The Pico E-14 features 16 GPIO lines that are used for external peripheral support. Pulling the DIAG_EN pin low replaces 4 GPIO signals with JTAG signals.

All GPIO signals have user selectable pull-up, pull-down, keeper or HI-Z termination. Drive strength is also user selectable between 2 and 24mA. All GPIOs can be configured for input, output and bi-directional mode and are equipped with ESD protection.

DIAG_EN State	JTAG	GPIO
Float / High	Disabled	Enabled
Low	Enabled	Disabled

Electrical Specifications	Minimum	Nominal	Maximum
High Voltage	1.7V	2.5V	2.9V
Low Voltage	-0.2V	0V	0.7V
Input Impedance (Pulldowns Disabled)		HI-Z	
Drive Strength (Selectable)	2 mA		24 mA
ESD Withstand Voltage (Human Body Model)			2 KV

CardBus Interface

The Pico E-14 can run as a standalone product or be connected to a host using the CardBus connector. By default, the Pico E-14 ships with firmware that is ready for use as a CardBus slave device, but it also supports bus mastering. That same firmware also provides the means to switch into standlone mode.[1]

CardBus is a 32-bit interface with a maximum speed of 33 MHz. The Pico E-14 hardware is designed to support standard PCMCIA as well as DMA mode. The CardBus standard specifies that all CardBus hosts be backward compatible with PCMCIA.

Since CardBus systems can only be 3.3V, no digital translating transceivers are required to connect with a host. This allows direct connection to the Virtex-4 FPGA for reduced power consumption. With this design, it is easily possible to reverse the CardBus interface and use the Pico E-14 as a host controller for other CardBus and PCMCIA cards.

Those who are interested in alternate interfaces should contact Pico Computing. The PCMCIA decoder source code and support is available.

PCMCIA Interface Resources:

CompactFlash Association	www.compactflash.org
PCMCIA Website	www.pcmcia.org

[1] For more information on standlone, reference the Standalone documentation located in the doc directory of where Pico Utility is installed.

Digital Bus Interface

When the Pico E-14 is not connected to a CardBus host, the digital bus can be reconfigured to connect with a wide variety of high-speed digital busses and peripherals. All signals have user selectable pull-up, pull-down, keeper or HI-Z termination. Drive strength is also user selectable between 2 and 24mA. All pins can be configured for input, output and bi-directional mode.

With proper termination, speeds of over 200 MHz are possible. The external digital bus is set to transmit and receive at 3.3V only.

Electrical Specifications (DC)	Minimum	Nominal	Maximum
Positive Supply Input Voltage (Vcc)	3.15V	3.3V	5.5V
Low Level Input Voltage	0V	0V	0.7V
High Level Input Voltage	2V	3.0V	3.3V
Drive Strength	2mA		24mA

JTAG Debug Interface

The Pico E-14 is equipped with a JTAG diagnostic port that allows real-time debugging of hardware, firmware and software. Use of the external JTAG port disables four external GPIO pins as well as the internal JTAG loop back.

Some JTAG programs require the length of the instruction register (IR). The IR length is listed below for all devices in the JTAG chain.

Device	Instruction register bit length	
	FX20	FX60
FPGA	10	14
TurboLoader	8	
Ethernet PHY	8	

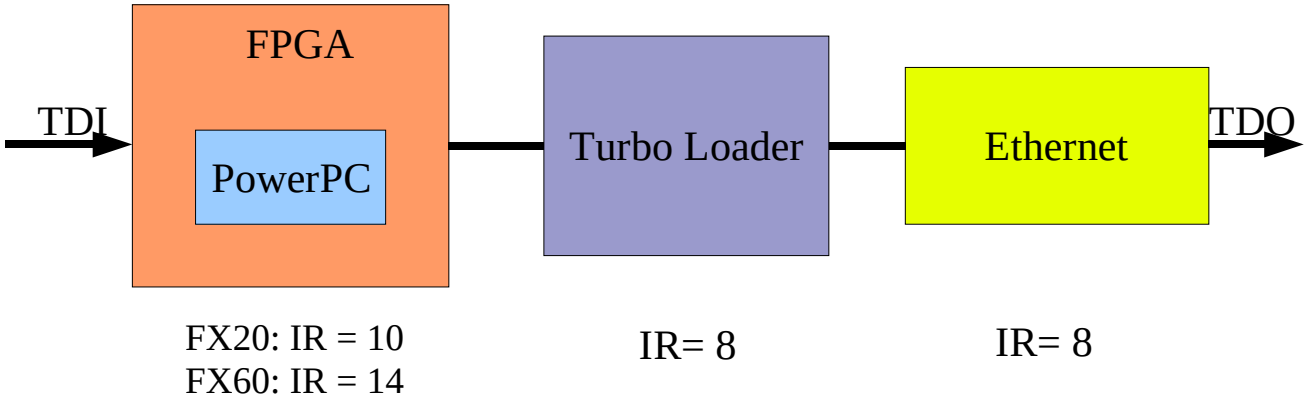


Figure 4

The Primary Image in the Flash ROM contains an embedded JTAG diagnostic port. This allows a user in Windows or Linux to debug software without an external JTAG cable. The internal JTAG diagnostic loop back looks just like a Parallel Port IV diagnostic cable when used with the Pico E-14 driver.

Appendix A – Peripheral I/O Connector Information

Connector Information

Description	Brand	Part Number
Mating Connector	Hirose	NX30TA-32PAA(50)
Mating Connector Backshell	Hirose	NX-32TA-CV1(50)

*Connectors are always in stock at Pico Computing

Peripheral I/O Connector Pinout

1	ETHER_OUT_DD-	Ethernet (Magnetically Isolated)
2	ETHER_OUT_DD+	Ethernet (Magnetically Isolated)
3	GPIO_15_FILTERED	General purpose I/O
4	GPIO_14_FILTERED	General purpose I/O
5	GPIO_13_FILTERED	General purpose I/O
6	GPIO_12_FILTERED	General purpose I/O
7	ETHER_OUT_DC-	Ethernet (Magnetically Isolated)
8	ETHER_OUT_DC+	Ethernet (Magnetically Isolated)
9	GPIO_11_FILTERED	General purpose I/O
10	GPIO_10_FILTERED	General purpose I/O
11	GPIO_9_FILTERED	General purpose I/O
12	GPIO_8_FILTERED	General purpose I/O
13	ETHER_OUT_DB-	Ethernet (Magnetically Isolated)
14	ETHER_OUT_DB+	Ethernet (Magnetically Isolated)
15	GPIO_7_FILTERED	General purpose I/O
16	GPIO_6_FILTERED	General purpose I/O
17	GPIO_5_FILTERED	General purpose I/O
18	GPIO_4_FILTERED	General purpose I/O
19	ETHER_OUT_DA-	Ethernet (Magnetically Isolated)
20	ETHER_OUT_DA+	Ethernet (Magnetically Isolated)
21	DAC_OUTPUT	D/A Converter output
22	SERIAL_RX_FILT	RS-232 Serial receiver input
23	SERIAL_TX_FILT	RS-232 Serial driver output
24	ADC_INPUT	A/D Converter input
25	PIC_TRIGGER_EXT	NOT CONNECTED
26	2.5V_EXT	2.5V 0.45A peripheral power
27	GPIO_3/TDI_FILT	General purpose I/O or JTAG TDI
28	GPIO_2/TDO_FILT	General purpose I/O or JTAG TDO
29	GPIO_1/TMS_FILT	General purpose I/O or JTAG TMS
30	GPIO_0/TCK_FILT	General purpose I/O or JTAG TCK
31	D\I\A\G_\E\N_\	JTAG port enable when shorted to ground
32	GND_EXT	Ground return

NOTE: Pin 1 indicator on the board is actually Pin 32 indicator

Peripheral Connector Pin #1 Location

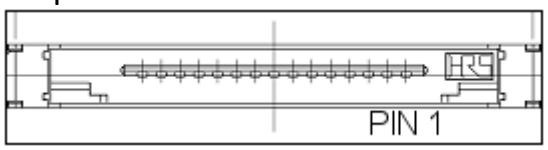


Figure 5

Appendix B – CardBus Connector Information

Connector Information

Description	Brand	Part Number
CardBus Header	Hirose	IC9-68RD-0.635SF-(51)

The Pico E-14 will mate with any Type-II CardBus Header

The function and direction of the pins on the CardBus interface can be easily changed. Please see the "Digital Bus Interface" section for more information.

CardBus Connector Pinout

Name	Pin	Description	Dir
GND	1	Card Ground	PWR
CAD0	2	CardBus Data/Address 0	IO
CAD1	3	CardBus Data/Address 1	IO
CAD3	4	CardBus Data/Address 3	IO
CAD5	5	CardBus Data/Address 5	IO
CAD7	6	CardBus Data/Address 7	IO
C\C\/\B\E\0\	7	Command and Byte Enable	IO
CAD9	8	CardBus Data/Address 9	IO
CAD11	9	CardBus Data/Address 11	IO
CAD12	10	CardBus Data/Address 12	IO
CAD14	11	CardBus Data/Address 14	IO
C\C\/\B\E\1\	12	Command and Byte Enable	IO
CPAR	13	Parity	IO
C\P\E\R\R\	14	Parity Error	IO
C\G\N\T\	15	Grand	I
C\I\N\T\	16	Card Intert Request	O
VCC	17	Card Power (3.3V)	PWR
VPP	18	Card Programming Voltage (Not Used)	PWR
CCLK	19	CardBus Clock	I
C\I\R\D\Y\	20	Initiator Ready	IO
C\C\/\B\E\2\	21	Command and Byte Enable	IO
CAD18	22	CardBus Data/Address 18	IO
CAD20	23	CardBus Data/Address 20	IO
CAD21	24	CardBus Data/Address 21	IO
CAD22	25	CardBus Data/Address 22	IO
CAD23	26	CardBus Data/Address 23	IO
CAD24	27	CardBus Data/Address 24	IO
CAD25	28	CardBus Data/Address 25	IO

CAD26	29	CardBus Data/Address 26	IO
CAD27	30	CardBus Data/Address 27	IO
CAD29	31	CardBus Data/Address 29	IO
RFU	32	Reserved For Future Use	IO
C\C\L\K\R\U\N\	33	Clock Request / Status	O
GND	34	Card Ground	PWR
GND	35	Card Ground	PWR
C\C\D\1\	36	Card Detect	Passive
CAD2	37	CardBus Data/Address 2	IO
CAD4	38	CardBus Data/Address 4	IO
CAD6	39	CardBus Data/Address 6	IO
RFU	40	Reserved For Future Use	IO
CAD8	41	CardBus Data/Address 8	IO
CAD10	42	CardBus Data/Address 10	IO
C\V\S\1\	43	Voltage Select	PWR
CAD13	44	CardBus Data/Address 13	IO
CAD15	45	CardBus Data/Address 15	IO
CAD16	46	CardBus Data/Address 16	IO
RFU	47	Reserved For Future Use	IO
C\B\L\O\C\K\	48	Card Lock	IO
C\S\T\O\P\	49	Stop Transaction	IO
C\D\E\V\S\E\L\	50	Device Select	IO
VCC	51	Card Power (3.3V)	PWR
VPP	52	Card Programming Voltage (Not Used)	PWR
C\T\R\D\Y\	53	Target Ready	IO
C\F\R\A\M\E\	54	Cycle Frame	IO
CAD17	55	CardBus Data/Address 17	IO
CAD19	56	CardBus Data/Address 19	IO
C\V\S\2\	57	Voltage Select	Passive
C\R\S\T\	58	System Reset	I
C\S\E\R\R\	59	System Error	O
C\R\E\Q\	60	Request	O
C\C\/\B\E\3\	61	Command and Byte Enable	IO
CAUDIO	62	Card Audio Signal	O
CSTSCHG	63	Card Status Change	O
CAD28	64	CardBus Data/Address 28	IO
CAD30	65	CardBus Data/Address 30	IO
CAD31	66	CardBus Data/Address 31	IO
C\C\D\2\	67	Card Detect	Passive
GND	68	Card Ground	PWR

CardBus Connector Pull Up and Pull Down Information

Name	Pin	Description	Value
-CGNT	15	Pull Up	15K
-CFRAME	54	Pull Up	15K
-CTRDY	53	Pull Up	15K
-CIRDY	20	Pull Up	15K

For additional information consult the CardBus Standard available from: www.pcmcia.org.

Appendix C – FPGA Pinout

FPGA Pinout

50MHZ_CLOCK	AA14	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
50MHZ_CLOCK	AB12	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
50MHZ_CLOCK	AB14	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
50MHZ_CLOCK	AC13	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
50MHZ_CLOCK	AD15	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
50MHZ_CLOCK	AE13	50 MHz Clock In +/- 50 ppm	I	LV_TTL 3.3V
ADC_AMP_PWUP	AD14	A/D Amplifier Power Up	O	LV_TTL 3.3V
ADC_CLK	V23	Clock	O	LV_CMOS 2.5V
ADC_D0	W23	Data 0 [LSB]	I	LV_CMOS 2.5V
ADC_D1	T24	Data 1	I	LV_CMOS 2.5V
ADC_D2	V21	Data 2	I	LV_CMOS 2.5V
ADC_D3	W18	Data 3	I	LV_CMOS 2.5V
ADC_D4	Y22	Data 4	I	LV_CMOS 2.5V
ADC_D5	W20	Data 5	I	LV_CMOS 2.5V
ADC_D6	AB21	Data 6	I	LV_CMOS 2.5V
ADC_D7	Y18	Data 7	I	LV_CMOS 2.5V
ADC_D8	AB20	Data 8	I	LV_CMOS 2.5V
ADC_D9	AC21	Data 9	I	LV_CMOS 2.5V
ADC_D10	T20	Data 10	I	LV_CMOS 2.5V
ADC_D11	R20	Data 11	I	LV_CMOS 2.5V
ADC_D12	R21	Data 12	I	LV_CMOS 2.5V
ADC_D13	V18	Data 13 [MSB]	I	LV_CMOS 2.5V
ADC_MODE	T17	Data Format Select	O	LV_CMOS 2.5V
ADC_OTR	T18	Out-of-Range Indicator	O	LV_CMOS 2.5V
ADC_PDWN	V22	Power Down A/D Controller	O	LV_CMOS 2.5V
CB_CAD0	K3	CardBus Data/Address 0	I/O	LV_TTL 3.3V
CB_CAD1	F3	CardBus Data/Address 1	I/O	LV_TTL 3.3V
CB_CAD2	D3	CardBus Data/Address 2	I/O	LV_TTL 3.3V
CB_CAD3	C3	CardBus Data/Address 3	I/O	LV_TTL 3.3V
CB_CAD4	M6	CardBus Data/Address 4	I/O	LV_TTL 3.3V
CB_CAD5	L7	CardBus Data/Address 5	I/O	LV_TTL 3.3V
CB_CAD6	K7	CardBus Data/Address 6	I/O	LV_TTL 3.3V
CB_CAD7	J4	CardBus Data/Address 7	I/O	LV_TTL 3.3V
CB_CAD8	G5	CardBus Data/Address 8	I/O	LV_TTL 3.3V
CB_CAD9	G9	CardBus Data/Address 9	I/O	LV_TTL 3.3V
CB_CAD10	F7	CardBus Data/Address 10	I/O	LV_TTL 3.3V
CB_CAD11	F8	CardBus Data/Address 11	I/O	LV_TTL 3.3V
CB_CAD12	D4	CardBus Data/Address 12	I/O	LV_TTL 3.3V
CB_CAD13	C4	CardBus Data/Address 13	I/O	LV_TTL 3.3V
CB_CAD14	D5	CardBus Data/Address 14	I/O	LV_TTL 3.3V

CB_CAD15	D6	CardBus Data/Address 15	I/O	LV_TTL 3.3V
CB_CAD16	C7	CardBus Data/Address 16	I/O	LV_TTL 3.3V
CB_CAD17	J5	CardBus Data/Address 17	I/O	LV_TTL 3.3V
CB_CAD18	K6	CardBus Data/Address 18	I/O	LV_TTL 3.3V
CB_CAD19	E5	CardBus Data/Address 19	I/O	LV_TTL 3.3V
CB_CAD20	E6	CardBus Data/Address 20	I/O	LV_TTL 3.3V
CB_CAD21	E7	CardBus Data/Address 21	I/O	LV_TTL 3.3V
CB_CAD22	D9	CardBus Data/Address 22	I/O	LV_TTL 3.3V
CB_CAD23	C8	CardBus Data/Address 23	I/O	LV_TTL 3.3V
CB_CAD24	F10	CardBus Data/Address 24	I/O	LV_TTL 3.3V
CB_CAD25	G4	CardBus Data/Address 25	I/O	LV_TTL 3.3V
CB_CAD26	J3	CardBus Data/Address 26	I/O	LV_TTL 3.3V
CB_CAD27	L10	CardBus Data/Address 27	I/O	LV_TTL 3.3V
CB_CAD28	K8	CardBus Data/Address 28	I/O	LV_TTL 3.3V
CB_CAD29	F4	CardBus Data/Address 29	I/O	LV_TTL 3.3V
CB_CAD30	K11	CardBus Data/Address 30	I/O	LV_TTL 3.3V
CB_CAD31	H9	CardBus Data/Address 31	I/O	LV_TTL 3.3V
CB_CAUDIO	H3	Card Audio Signal	O	LV_TTL 3.3V
CB_CBLOCK	B9	Card Lock	I/O	LV_TTL 3.3V
CB_CC/BE0	H4	Command and Byte Enables	I/O	LV_TTL 3.3V
CB_CC/BE1	C6	Command and Byte Enables	I/O	LV_TTL 3.3V
CB_CC/BE2	H6	Command and Byte Enables	I/O	LV_TTL 3.3V
CB_CC/BE3	D10	Command and Byte Enables	I/O	LV_TTL 3.3V
CB_CCLK	D11	Clock	I	LV_TTL 3.3V
CB_CCLKRUN	G10	Clock Request / Status	I/O	LV_TTL 3.3V
CB_CDEVSEL	G12	Device Select	I/O	LV_TTL 3.3V
CB_CFRAME	H8	Cycle Frame	I/O	LV_TTL 3.3V
CB_CGNT	A9	Grant	I	LV_TTL 3.3V
CB_CINT	B11	Card Interrupt Request	O	LV_TTL 3.3V
CB_CIRDY	G7	Initiator Ready	I/O	LV_TTL 3.3V
CB_CPAR	A7	Parity	I/O	LV_TTL 3.3V
CB_CPERR	A8	Parity Error	I/O	LV_TTL 3.3V
CB_CREQ	B10	Request	O	LV_TTL 3.3V
CB_CRST	D8	Card Reset	I	LV_TTL 3.3V
CB_CSERR	C9	System Error	O	LV_TTL 3.3V
CB_CSTOP	A10	Stop Transaction	I/O	LV_TTL 3.3V
CB_CSTSCHG	J9	Card Status Change	O	LV_TTL 3.3V
CB_CTRDY	E8	Target Ready	I/O	LV_TTL 3.3V
CB_RFU1	E3	CardBus: Reserved for Future Use	I/O	LV_TTL 3.3V
CB_RFU2	H7	CardBus: Reserved for Future Use	I/O	LV_TTL 3.3V
CB_RFU3	B7	CardBus: Reserved for Future Use	I/O	LV_TTL 3.3V
CPLD_TDI	R13	CPLD JTAG TDI		LV_TTL 3.3V
DAC_AMP_PWUP	K12	D/A Amplifier Power Up	O	LV_TTL 3.3V
DAC_CLK	H11	Clock	O	LV_TTL 3.3V
DAC_CLK-	J11	Complementary Clock	O	LV_TTL 3.3V
DAC_CMODE	B6	Clock Mode Selection	O	LV_TTL 3.3V

DAC_D0	H16	Data 0 [LSB]	O	LV_TTL 3.3V
DAC_D1	K13	Data 1	O	LV_TTL 3.3V
DAC_D2	G11	Data 2	O	LV_TTL 3.3V
DAC_D3	J14	Data 3	O	LV_TTL 3.3V
DAC_D4	E10	Data 4	O	LV_TTL 3.3V
DAC_D5	H12	Data 5	O	LV_TTL 3.3V
DAC_D6	H13	Data 6	O	LV_TTL 3.3V
DAC_D7	C11	Data 7	O	LV_TTL 3.3V
DAC_D8	H14	Data 8	O	LV_TTL 3.3V
DAC_D9	G15	Data 9	O	LV_TTL 3.3V
DAC_D10	G14	Data 10	O	LV_TTL 3.3V
DAC_D11	J15	Data 11	O	LV_TTL 3.3V
DAC_D12	J16	Data 12	O	LV_TTL 3.3V
DAC_D13	G16	Data 13 [MSB]	O	LV_TTL 3.3V
DAC_MODE	K10	Input Data Format	O	LV_TTL 3.3V
DAC_SLEEP	E11	Power Down D/A Controller	O	LV_TTL 3.3V
ETHER_25MHZ	AA15	25 MHz Clock	O	LV_CMOS 2.5V
ETHER_125MHZ	P24	125 MHz Clock	I	LV_CMOS 2.5V
ETHER_COL	AD19	Collision Detect	I	LV_CMOS 2.5V
ETHER_COMA	AC19	Power Save Mode	O	LV_CMOS 2.5V
ETHER_CRS	AA19	Carrier Sense	I	LV_CMOS 2.5V
ETHER_IRQ	AB15	IRQ	I	LV_CMOS 2.5V
ETHER_MDC	AD24	Media Independent Interface Clock	O	LV_CMOS 2.5V
ETHER_MDIO	AC16	Media Independent Interface Data	I/O	LV_CMOS 2.5V
ETHER_RESET	AC24	Reset	O	LV_CMOS 2.5V
ETHER_RX0	U24	MII/GMII Data In 0	I	LV_CMOS 2.5V
ETHER_RX1	AD20	MII/GMII Data In 1	I	LV_CMOS 2.5V
ETHER_RX2	AD21	MII/GMII Data In 2	I	LV_CMOS 2.5V
ETHER_RX3	AD16	MII/GMII Data In 3	I	LV_CMOS 2.5V
ETHER_RX4	U21	MII/GMII Data In 4	I	LV_CMOS 2.5V
ETHER_RX5	T23	MII/GMII Data In 5	I	LV_CMOS 2.5V
ETHER_RX6	AD18	MII/GMII Data In 6	I	LV_CMOS 2.5V
ETHER_RX7	T22	MII/GMII Data In 7	I	LV_CMOS 2.5V
ETHER_RX_CLK	V24	MII/GMII RX Clock	I	LV_CMOS 2.5V
ETHER_RX_CTL	AB16	MII/GMII RX Enable	I	LV_CMOS 2.5V
ETHER_RX_ER	Y23	MII/GMII RX Error	I	LV_CMOS 2.5V
ETHER_TX0	AA22	MII/GMII Data Out 0	O	LV_CMOS 2.5V
ETHER_TX1	AC18	MII/GMII Data Out 1	O	LV_CMOS 2.5V
ETHER_TX2	AB24	MII/GMII Data Out 2	O	LV_CMOS 2.5V
ETHER_TX3	AB19	MII/GMII Data Out 3	O	LV_CMOS 2.5V
ETHER_TX4	AB17	MII/GMII Data Out 4	O	LV_CMOS 2.5V
ETHER_TX5	AA23	MII/GMII Data Out 5	O	LV_CMOS 2.5V
ETHER_TX6	AC17	MII/GMII Data Out 6	O	LV_CMOS 2.5V
ETHER_TX7	AC23	MII/GMII Data Out 7	O	LV_CMOS 2.5V
ETHER_TX_CLK	W24	MII/GMII TX Clock	O	LV_CMOS 2.5V
ETHER_TX_CTL	AA24	MII/GMII TX Enable	O	LV_CMOS 2.5V

ETHER_TX_ER	AA18	MII/GMII TX Error	I	LV_CMOS 2.5V
F\L\A\S\H_\B\Y\T\E\	AD3	Inverted 8/16 Bit Mode Select	O	LV_CMOS 2.5V
F\L\A\S\H_\O\E\	AA3	Inverted Output Enable	O	LV_CMOS 2.5V
F\L\A\S\H_\R\E\S\E\T\	T3	Inverted Reset	O	LV_CMOS 2.5V
F\L\A\S\H_\W\E\	W5	Inverted Write Enable	O	LV_CMOS 2.5V
F\L\A\S\H_\W\P\	Y16	InvertedWrite Protect	O	LV_CMOS 2.5V
F\L\A\S\H_C\E\	V3	Inverted Chip Enable	O	LV_CMOS 2.5V
F\P\G\A_\P\R\O	K17	Inverted FPGA Program	O	LV_CMOS 2.5V
FLASH_A0	AD6	Address 0 [LSB]	I/O	LV_CMOS 2.5V
FLASH_A1	AD8	Address 1	I/O	LV_CMOS 2.5V
FLASH_A2	AD10	Address 2	I/O	LV_CMOS 2.5V
FLASH_A3	AC11	Address 3	I/O	LV_CMOS 2.5V
FLASH_A4	AD9	Address 4	I/O	LV_CMOS 2.5V
FLASH_A5	Y3	Address 5	I/O	LV_CMOS 2.5V
FLASH_A6	AC9	Address 6	I/O	LV_CMOS 2.5V
FLASH_A7	V4	Address 7	I/O	LV_CMOS 2.5V
FLASH_A8	P3	Address 8	I/O	LV_CMOS 2.5V
FLASH_A9	U5	Address 9	I/O	LV_CMOS 2.5V
FLASH_A10	P5	Address 10	I/O	LV_CMOS 2.5V
FLASH_A11	AC4	Address 11	I/O	LV_CMOS 2.5V
FLASH_A12	N4	Address 12	I/O	LV_CMOS 2.5V
FLASH_A13	R5	Address 13	I/O	LV_CMOS 2.5V
FLASH_A14	W3	Address 14	I/O	LV_CMOS 2.5V
FLASH_A15	AA8	Address 15	I/O	LV_CMOS 2.5V
FLASH_A16	AD4	Address 16	I/O	LV_CMOS 2.5V
FLASH_A17	AD11	Address 17	I/O	LV_CMOS 2.5V
FLASH_A18	AB6	Address 18	I/O	LV_CMOS 2.5V
FLASH_A19	AC7	Address 19	I/O	LV_CMOS 2.5V
FLASH_A20	AC6	Address 20	I/O	LV_CMOS 2.5V
FLASH_A21	AB5	Address 21	I/O	LV_CMOS 2.5V
FLASH_A22	AB11	Address 22	I/O	LV_CMOS 2.5V
FLASH_A23	AB9	Address 23	I/O	LV_CMOS 2.5V
FLASH_A24	AB4	Address 24	I/O	LV_CMOS 2.5V
FLASH_A25	AC3	Address 25 [MSB]	I/O	LV_CMOS 2.5V
FLASH_D0	V12	Data 0 [LSB]	I/O	LV_CMOS 2.5V
FLASH_D1	V13	Data 1	I/O	LV_CMOS 2.5V
FLASH_D2	V14	Data 2	I/O	LV_CMOS 2.5V
FLASH_D3	U14	Data 3	I/O	LV_CMOS 2.5V
FLASH_D4	W13	Data 4	I/O	LV_CMOS 2.5V
FLASH_D5	Y13	Data 5	I/O	LV_CMOS 2.5V
FLASH_D6	W14	Data 6	I/O	LV_CMOS 2.5V
FLASH_D7	W15	Data 7	I/O	LV_CMOS 2.5V
FLASH_D8	V11	Data 8	I/O	LV_CMOS 2.5V
FLASH_D9	W11	Data 9	I/O	LV_CMOS 2.5V
FLASH_D10	U15	Data 10	I/O	LV_CMOS 2.5V
FLASH_D11	U16	Data 11	I/O	LV_CMOS 2.5V

FLASH_D12	Y11	Data 12	I/O	LV_CMOS 2.5V
FLASH_D13	Y12	Data 13	I/O	LV_CMOS 2.5V
FLASH_D14	W16	Data 14	I/O	LV_CMOS 2.5V
FLASH_D15	V16	Data 15 [MSB]	I/O	LV_CMOS 2.5V
FLASH_READY	Y15	Flash Status	I	LV_CMOS 2.5V
FPGA_CCLK	M14	FPGA Clock	O	LV_CMOS 2.5V
FPGA_DONE	K15	FPGA Done	O	LV_CMOS 2.5V
FPGA_INIT	L15	FPGA Initialize	O	LV_CMOS 2.5V
GPIO_0	AA4	GPIO 1	I/O	LV_CMOS 2.5V
GPIO_1	AA5	GPIO 2	I/O	LV_CMOS 2.5V
GPIO_2	AC22	GPIO 3	I/O	LV_CMOS 2.5V
GPIO_3	AB22	GPIO 4	I/O	LV_CMOS 2.5V
GPIO_4	Y5	GPIO 1	I/O	LV_CMOS 2.5V
GPIO_5	W4	GPIO 2	I/O	LV_CMOS 2.5V
GPIO_6	Y6	GPIO 3	I/O	LV_CMOS 2.5V
GPIO_7	Y7	GPIO 4	I/O	LV_CMOS 2.5V
GPIO_8	AB10	GPIO 1	I/O	LV_CMOS 2.5V
GPIO_9	Y10	GPIO 2	I/O	LV_CMOS 2.5V
GPIO_10	AA10	GPIO 3	I/O	LV_CMOS 2.5V
GPIO_11	N3	GPIO 4	I/O	LV_CMOS 2.5V
GPIO_12	W19	GPIO 1	I/O	LV_CMOS 2.5V
GPIO_13	AA20	GPIO 2	I/O	LV_CMOS 2.5V
GPIO_14	W21	GPIO 3	I/O	LV_CMOS 2.5V
GPIO_15	AD23	GPIO 4	I/O	LV_CMOS 2.5V
JTAG_LOOP_TCK	V8	JTAG Loop back TCK	O	LV_CMOS 2.5V
JTAG_LOOP_TDI	V6	JTAG Loop back TDI	I	LV_CMOS 2.5V
JTAG_LOOP_TDO	Y8	JTAG Loop back TDO	O	LV_CMOS 2.5V
JTAG_LOOP_TMS	AC8	JTAG Loop back TMS	O	LV_CMOS 2.5V
LOAD	T4	TurboLoader Load Image Request	O	LV_CMOS 2.5V
PEEKABOO	P4	TurboLoader Load Image Request	O	LV_CMOS 2.5V
PIC_CLK	AF14	Power Management Controller Sleep Counter	O	LV_TTL 3.3V
PIC_DATA	AF15	Power Management Controller Sleep Request	O	LV_TTL 3.3V
R\A\M_\C\A\S\	F24	Inverted Column Select	O	SSTL18_II_DCI
R\A\M_\C\L\K\	B14	Inverted Complementary Clock	O	SSTL18_II_DCI
R\A\M_\C\L\K\	E15	Inverted Comp. Clock Feedback	I	SSTL18_II_DCI
R\A\M_\C\S\0\	C23	Inverted Chip Select Bank 0	O	SSTL18_II_DCI
R\A\M_\C\S\1\	C24	Inverted Chip Select Bank 1	O	SSTL18_II_DCI
R\A\M_\R\A\S\	F22	Inverted Row Select	O	SSTL18_II_DCI
R\A\M_\W\E\	B15	Inverted Write Enable	O	SSTL18_II_DCI
RAM_A0	D20	Address 0 [LSB]	O	SSTL18_II_DCI
RAM_A1	F19	Address 1	O	SSTL18_II_DCI
RAM_A2	A12	Address 2	O	SSTL18_II_DCI
RAM_A3	D21	Address 3	O	SSTL18_II_DCI
RAM_A4	E21	Address 4	O	SSTL18_II_DCI
RAM_A5	G21	Address 5	O	SSTL18_II_DCI
RAM_A6	A13	Address 6	O	SSTL18_II_DCI

RAM_A7	E22	Address 7	O	SSTL18_II_DCI
RAM_A8	D24	Address 8	O	SSTL18_II_DCI
RAM_A9	F20	Address 9	O	SSTL18_II_DCI
RAM_A10	F23	Address 10	O	SSTL18_II_DCI
RAM_A11	A14	Address 11	O	SSTL18_II_DCI
RAM_A12	D23	Address 12 [MSB]	O	SSTL18_II_DCI
RAM_BA0	E23	Bank Address 0	O	SSTL18_II_DCI
RAM_BA1	K18	Bank Address 1	O	SSTL18_II_DCI
RAM_CLK	C14	Clock	O	SSTL18_II_DCI
RAM_CLK	F15	Clock Feedback	I	SSTL18_II_DCI
RAM_CLKE0	A15	Clock Enable 0[Power Save Mode]	O	SSTL18_II_DCI
RAM_CLKE1	G22	Clock Enable 1[Power Save Mode]	O	SSTL18_II_DCI
RAM_D0	C19	Data 0 (LSB)	I/O	SSTL18_II_DCI
RAM_D1	F18	Data 1	I/O	SSTL18_II_DCI
RAM_D2	G20	Data 2	I/O	SSTL18_II_DCI
RAM_D3	D19	Data 3	I/O	SSTL18_II_DCI
RAM_D4	C21	Data 4	I/O	SSTL18_II_DCI
RAM_D5	E20	Data 5	I/O	SSTL18_II_DCI
RAM_D6	F17	Data 6	I/O	SSTL18_II_DCI
RAM_D7	B17	Data 7	I/O	SSTL18_II_DCI
RAM_D8	D15	Data 8	I/O	SSTL18_II_DCI
RAM_D9	D14	Data 9	I/O	SSTL18_II_DCI
RAM_D10	C16	Data 10	I/O	SSTL18_II_DCI
RAM_D11	A17	Data 11	I/O	SSTL18_II_DCI
RAM_D12	G17	Data 12	I/O	SSTL18_II_DCI
RAM_D13	B16	Data 13	I/O	SSTL18_II_DCI
RAM_D14	C12	Data 14	I/O	SSTL18_II_DCI
RAM_D15	B12	Data 15	I/O	SSTL18_II_DCI
RAM_D16	H19	Data 16	I/O	SSTL18_II_DCI
RAM_D17	H22	Data 17	I/O	SSTL18_II_DCI
RAM_D18	G24	Data 18	I/O	SSTL18_II_DCI
RAM_D19	H24	Data 19	I/O	SSTL18_II_DCI
RAM_D20	J21	Data 20	I/O	SSTL18_II_DCI
RAM_D21	G19	Data 21	I/O	SSTL18_II_DCI
RAM_D22	K20	Data 22	I/O	SSTL18_II_DCI
RAM_D23	K23	Data 23	I/O	SSTL18_II_DCI
RAM_D24	M22	Data 24	I/O	SSTL18_II_DCI
RAM_D25	M24	Data 25	I/O	SSTL18_II_DCI
RAM_D26	K21	Data 26	I/O	SSTL18_II_DCI
RAM_D27	L24	Data 27	I/O	SSTL18_II_DCI
RAM_D28	N22	Data 28	I/O	SSTL18_II_DCI
RAM_D29	L19	Data 29	I/O	SSTL18_II_DCI
RAM_D30	N24	Data 30	I/O	SSTL18_II_DCI
RAM_D31	J23	Data 31	I/O	SSTL18_II_DCI
RAM_DM0-7	E17	Data Mask [0-7]	O	SSTL18_II_DCI
RAM_DM8-15	C13	Data Mask [8-15]	O	SSTL18_II_DCI

RAM_DM16-23	L18	Data Mask [16-23]	O	SSTL18_II_DCI
RAM_DM24-31	N23	Data Mask [24-31]	O	SSTL18_II_DCI
RAM_LOOPBACK	D13	Loopback Input	I	SSTL18_II_DCI
RAM_LOOPBACK	H17	Loopback Output	O	SSTL18_II_DCI
RAM_ODT0	J19	On-Die Termination Enable 0	O	SSTL18_II_DCI
RAM_ODT1	D18	On-Die Termination Enable 1	O	SSTL18_II_DCI
RAM_STROBE0	C18	Strobe D16-D31 - Bank 0	O	SSTL18_II_DCI
RAM_STROBE1	C17	Strobe D0-D15 - Bank 0	O	SSTL18_II_DCI
RAM_STROBE2	L23	Strobe D16-D31 - Bank 1	O	SSTL18_II_DCI
RAM_STROBE3	K22	Strobe D0-D15 - Bank 1	O	SSTL18_II_DCI
RS232-EN	J13	Serial Transceiver Enable	O	LV_TTL 3.3V
RS232-RX	M5	Serial Receive	O	LV_TTL 3.3V
RS232-TX	L5	Serial Transmit	O	LV_TTL 3.3V
RS232-VALID	L9	Serial Valid	I	LV_TTL 3.3V
SLEEP	U4	TurboLoader Sleep Request	O	LV_CMOS 2.5V
TCK	U10	JTAG TCK	O	LV_CMOS 2.5V
TDI	U11	JTAG TDI	I	LV_CMOS 2.5V
TMS	T10	JTAG TMS	O	LV_CMOS 2.5V
VRN1	F14	NOT CONNECTED	I/O	LV_CMOS 2.5V
VRN2	J24	NOT CONNECTED	I/O	LV_CMOS 2.5V
VRP1	F13	NOT CONNECTED	I/O	LV_CMOS 2.5V
VRP2	H23	NOT CONNECTED	I/O	LV_CMOS 2.5V

Appendix D – CPLD Pinout

CPLD Pinout

Net	Pin	Description	Direction
50MHZ_CLOCK	K2	50 MHz Clock In +/- 50 ppm	I
CPLD_TDI	J10	CPLD JTAG TDI	O
ETHER_TDI	A6	Ethernet JTAG TDI	O
F\L\A\S\H_\B\Y\T\E\	K7	8/16 Bit Mode Select	O
F\L\A\S\H_\O\E\	A8	Output Enable	O
F\L\A\S\H_\R\E\S\E\T\	A2	Flash Reset	O
F\L\A\S\H_\W\E\	A3	Flash Write Enable	O
F\L\A\S\H_\W\P\	A4	Flash Write Protect	O
F\L\A\S\H_C\E\	A9	Flash Chip Enable	O
F\P\G\A_\P\R\O\G\	A5	FPGA Asynchronous Reset	O
FLASH_A0	K8	Address 1 [8 Bit Mode]	O
FLASH_A1	K1	Address 2	I/O
FLASH_A2	H1	Address 3	I/O
FLASH_A3	F1	Address 4	I/O
FLASH_A4	K4	Address 5	I/O
FLASH_A5	C3	Address 6	I/O
FLASH_A6	G3	Address 7	I/O
FLASH_A7	H3	Address 8	I/O
FLASH_A8	A7	Address 9	I/O
FLASH_A9	J1	Address 10	I/O
FLASH_A10	H10	Address 11	I/O
FLASH_A11	G1	Address 12	I/O
FLASH_A12	D1	Address 13	I/O
FLASH_A13	C1	Address 14	I/O
FLASH_A14	K5	Address 15	I/O
FLASH_A15	E1	Address 16	I/O
FLASH_A16	A1	Address 17	I/O
FLASH_A17	B1	Address 18	I/O
FLASH_A18	A10	Address 19	I/O
FLASH_A19	E3	Address 20	I/O
FLASH_A20	F3	Address 21	I/O
FLASH_A21	C5	Address 22	I/O
FLASH_A22	B10	Address 23	I/O
FLASH_A23	C4	Address 24	I/O
FLASH_A24	D8	Address 25	I/O
FLASH_A25	C8	Address 26	I/O
FLASH_D15	G10	Address 0*	I/O
FPGA_CCLK	F10	FPGA Configuration Clock	O
FPGA_DONE	D10	FPGA Done Programming	I
FPGA_INIT	E10	FPGA Ready to Program	I/O
LOAD	K6	Load Image Request	I
PEEKABOO	H5	Output Last Address Before Done Request	I

SLEEP	C10	Sleep Mode Request	I

*Pin D15 turns into Address -1 when the Flash ROM is in 8 bit mode.

Appendix E – Standard Part Number Listing

Standard Part Number Listing

Device	Part Number	Website
Pico E-14 EP		
FPGA	XC4VFX20-10FF672C XC4VFX60-10FF672C	http://www.xilinx.com/virtex4
CPLD	XC2C64A-7CP56I	http://www.xilinx.com/cpld
RAM	HYB18T512160BF-3.7	http://www.infineon.com
ROM	S29GL512N10FAI010	http://www.amd.com/us-en/FlashMemory
Ethernet	88E1111-B2-BAB-I000	http://www.marvell.com
ADC	AD9245ACP	http://www.analog.com
DAC	AD9744ACP	http://www.analog.com
RS-232 Serial	ISL4221EIR	http://www.intersil.com

Appendix F – Errata

The following section lists all known errata:

All versions:
Permanent damage will result if the Pico E-14 is left un-configured and powered on for more than 10 minutes. This should not be a problem since the Pico E-14 automatically loads an FPGA image upon power-on.

Appendix G – FPGA Performance Enhancements

Overview:
Like most silicon devices, the FPGA on the Pico can be overclocked if proper cooling techniques are employed. Care must be taken to avoid thermal runaway.

Thermal Runaway:
As the die temperature of the FPGA increases, it draws more current. This extra current gets turned into heat. If thermal equilibrium is not reached with proper cooling, the FPGA will overheat or overstress the power supplies. In all lab tests, the FPGA core power supply shut down before the FPGA could be damaged by an over temperature condition (although this behavior is not guaranteed). The maximum FPGA core temperature is 150°C. Note that chips surrounding the FPGA will be damaged by temperatures above 85°C.

Heat Sink Placement:
The heat sink of the FPGA is internally connected via thermal grease to the case of the CardBus card on the top side (serial number side). Placing a large heat sink on the outside of the case can allow higher performance.

Power Requirements:
Care must be taken to keep current consumption under the 1A maximum specified by the 3.3V CardBus standard. If an external power supply is available the board can be supplied 5.0V for maximum power, however, the digital interfaces will still communicate at the LVTTL 3.3V standard.

Speed Ratings:
Pico Computing uses all industrial temperature range parts where available. When a -10 industrial temperature speed grade FPGA is created, a -11 commercial speed grade part is tested to -10 performance ratings at the industrial temperature range. Pico computing does not guarantee that -10 industrial parts can be operated at -11 speeds when kept below 85°C.

Appendix E – Analog Interface Selection Guide

Parts in the table below are all pin-compatible with footprints on the Pico E-14 Card. Factors such as cost, power consumption, resolution, and speed should all be considered for the particular application in which the Pico E-14 is utilized.

Part	Resolution (bits)	Speed (MSPS)	Low Power
DAC AD9748ACP	8	165	
DAC AD9740ACP	10	165	
DAC AD9742ACP	12	210	
DAC AD9744ACP	14	165	
DAC AD9704CPZ*	8	175	X
DAC AD9705CPZ*	10	175	X
DAC AD9706CPZ*	12	175	X
DAC AD9707CPZ*	14	175	X
ADC AD9215BCP-65	10	65	
ADC AD9215BCP-80	10	80	
ADC AD9215BCP-105	10	105	
ADC AD9235BCP-20	12	20	
ADC AD9235BCP-40	12	40	
ADC AD9235BCP-65	12	65	
ADC AD9236BCP-80	12	80	
ADC AD9237BCP-20*	12	20	X
ADC AD9237BCP-40*	12	40	X
ADC AD9237BCP-65*	12	65	X
ADC AD9245BCP-80	14	80	

*Part not yet in production from Analog Devices as of 8/11/05

Revision History

14.1.8.11

Initial public release

14.1.8.12

Updated: Electrical Specifications, JTAG Debug interface, updated part numbers

Legal Notices