DATA SHEET

SAA7345
CMOS digital decoding IC with RAM for Compact Disc

Product specification
Supersedes data of 1996 Jan 09
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Philips Semiconductors

CMOS digital decoding IC with RAM for Compact Disc

SAA7345

FEATURES

- Integrated data slicer and clock regenerator
- Digital Phase-Locked Loop (PLL)
- Demodulator and Eight-to-Fourteen Modulation (EFM) decoding
- Subcoding microcontroller serial interface
- Integrated programmable motor speed control
- Error correction and concealment functions
- Embedded Static Random Access Memory (SRAM) for de-interleave and First-In First-Out (FIFO)
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface [European Broadcasting Union (EBU)]
- 2 to 4 times oversampling integrated digital filter
- Audio data peak level detection
- Versatile audio data serial interface
- Digital de-emphasis filter
- Kill interface for Digital-to-Analog Converter (DAC) deactivation during digital silence
- Double speed mode
- Compact Disc Read Only Memory (CD-ROM) modes
- A single speed only version is available (SAA7345GP/SS).

GENERAL DESCRIPTION

The SAA7345 incorporates the CD signal processing functions of decoding and digital filtering. The device is equipped with on-board SRAM and includes additional features to reduce the processing required in the analog domain.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	–	22	50	mA
f_{xtal}	crystal frequency	8	16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	–40	–	+85	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7345GP	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body $14 \times 14 \times 2.2$ mm	SOT205-1

BLOCK DIAGRAM

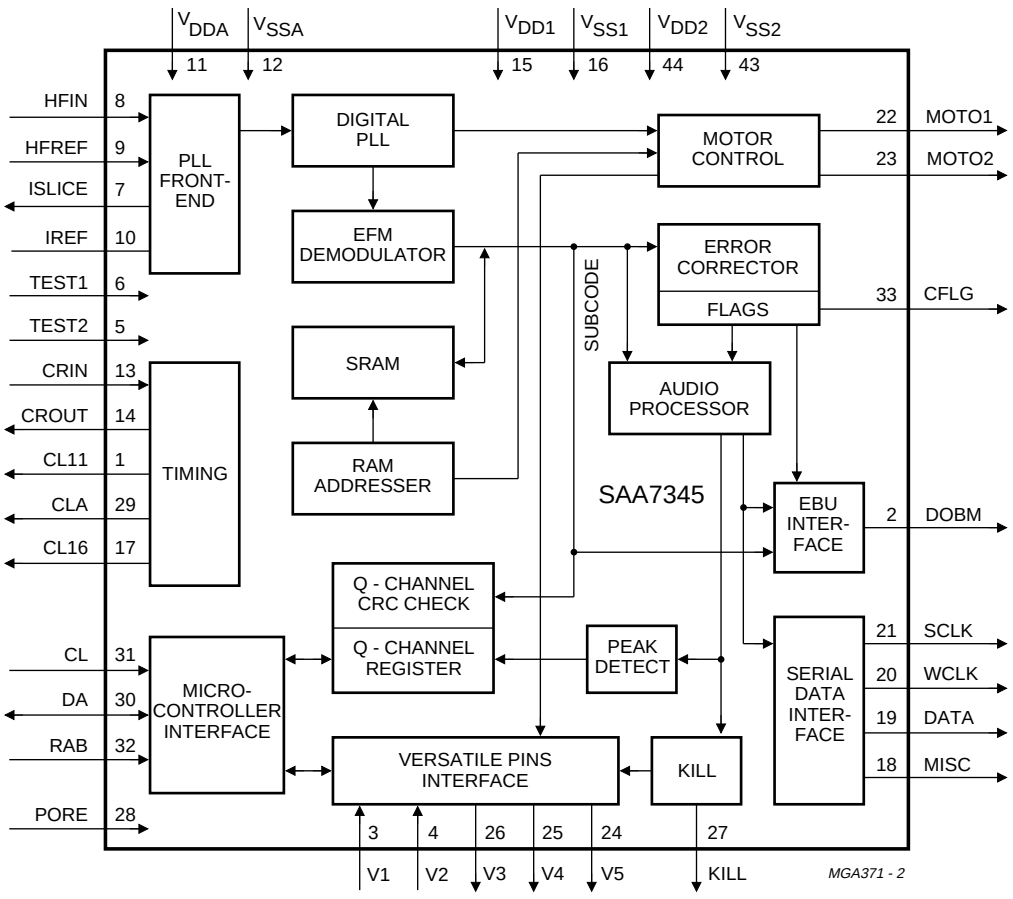


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CL11	1	11.2896 or 5.6448 MHz clock output (3-state); (divide-by-3)
DOBM	2	bi-phase mark output (externally buffered; 3-state)
V1	3	versatile input pin
V2	4	versatile input pin
TEST2	5	test input; this pin should be tied LOW
TEST1	6	test input; this pin should be tied LOW
ISLICE	7	current feedback output from data slicer
HFIN	8	comparator signal input
HFREF	9	comparator common-mode input
IREF	10	reference current pin (nominally $\frac{1}{2}V_{DD}$)
V_{DDA}	11	analog supply voltage; note 1
V_{SSA}	12	analog ground; note 1
CRIN	13	crystal/resonator input
CROUT	14	crystal/resonator output
V_{DD1}	15	digital supply to input and output buffers; note 1
V_{SS1}	16	digital ground to input and output buffers; note 1
CL16	17	16.9344 MHz system clock output
MISC	18	general purpose DAC output (3-state)
DATA	19	serial data output (3-state)
WCLK	20	word clock output (3-state)
SCLK	21	serial bit clock output (3-state)
MOTO1	22	motor output 1; versatile (3-state)
MOTO2	23	motor output 2; versatile (3-state)
V5	24	versatile output pin
V4	25	versatile output pin
V3	26	versatile output pin (open-drain)
KILL	27	kill output; programmable (open-drain)
$\overline{\text{PORE}}$	28	power-on reset enable input (active LOW)
CLA	29	4.2336 MHz microcontroller clock output
DA	30	interface data I/O line
CL	31	interface clock input line
RAB	32	interface R/$\overline{W}$ and acknowledge input
CFLG	33	correction flag output (open-drain)
n.c.	34 to 42	no internal connection
V_{SS2}	43	digital ground to internal logic; note 1
V_{DD2}	44	digital supply voltage to internal logic; note 1

Note

1. All supply pins must be connected to the same external power supply.

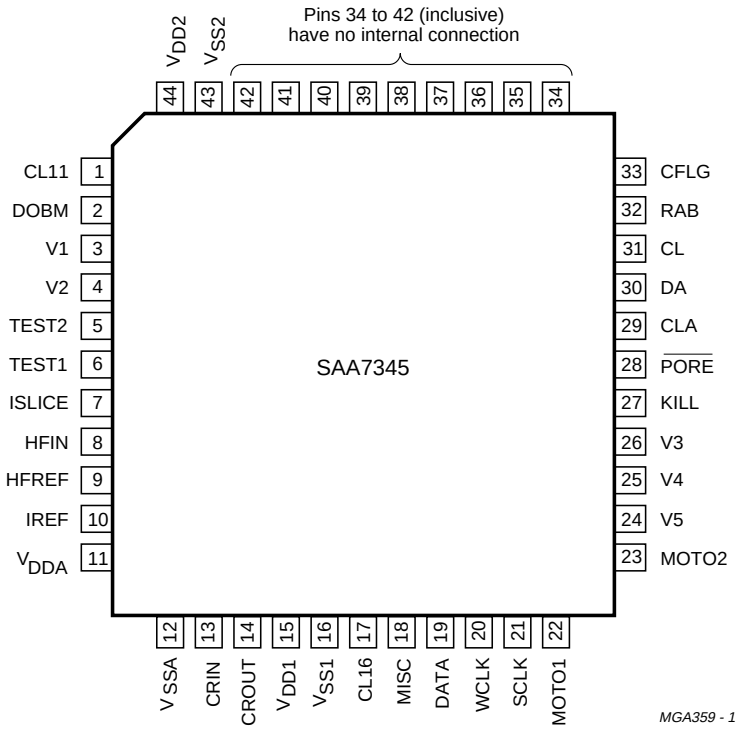


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Demodulator

FRAME SYNC PROTECTION

This circuit will detect the frame synchronization signals. Two synchronization counters are used in the SAA7345:

1. The coincidence counter which is used to detect the coincidence of successive syncs. It generates a Sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.
2. The main counter is used to partition the EFM signal into 17-bit words. This counter is reset when:
   a) A Sync coincidence is generated.
   b) A sync is found within ±6 EFM clocks of its expected position.

The Sync coincidence signal is also used to generate the Lock signal which will go active HIGH when 1 Sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no Sync coincidence is found. This Lock signal is accessed via the status signal when the status control register (address 0010) is set to X100. See section on “Microcontroller interface” .

Data Slicer and Clock Regenerator

The SAA7345 has an integrated slice level comparator which is clocked by the crystal frequency clock. The slice level is controlled by an internal current source applied to an external capacitor under the control of the digital phase-locked loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two microcontroller control registers (addresses 1000 and 1001) for bandwidth and equalization.

For certain applications an off-track input is necessary. If this flag is HIGH, the SAA7345 will assume that the servo is following on the wrong track, and will flag all incoming HF data as incorrect. The off-track is input via the V1 pin when the versatile pins interface register (address 1100) bit 0 is set to logic 1.

EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

Subcode data processing

Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. Sixteen bits are used to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the status signal when the status control register (address 0010) is set to X000 (normal reset condition). Good Q-channel data may be read via the microcontroller interface.

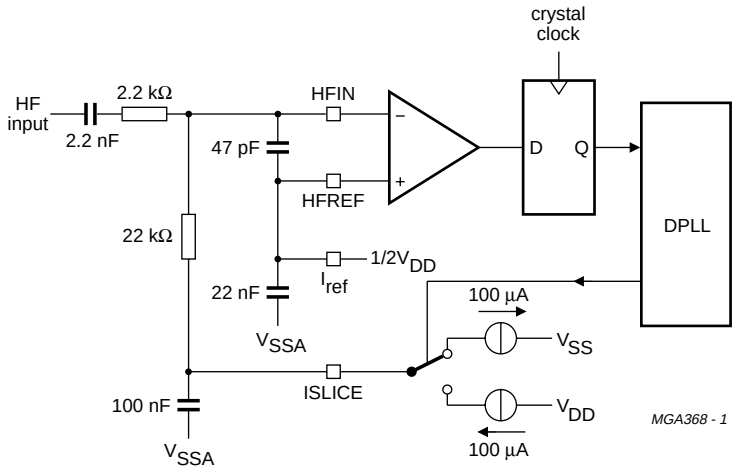


Fig.3 Data slicer showing typical application components.

OTHER SUBCODE CHANNELS

Data of the other subcode channels (Q-to-W) may be read via the V4 pin if the versatile pins interface register (address 1101) is set to XX01.

The format is similar to RS232. The subcode sync word is formed by a pause of 200 µs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between 11.3 µs and 90 µs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

Microcontroller interface

The SAA7345 has a 3-line microcontroller interface which is compatible with the digital servo IC TDA1301.

WRITING DATA TO SAA7345

The SAA7345 has thirteen 4-bit programmable configuration registers as shown in Table 2. These can be written to via the microcontroller interface using the protocol shown in Fig.5.

Write operation sequence

- RAB is held LOW by the microcontroller to hold the SAA7345 DA pin at high-impedance.
- Microcontroller data is clocked into the internal shift register on the LOW-to-HIGH clock transition CL.
- Data D (3 : 0) is latched into the appropriate control register [address bits A (3 : 0)] on the LOW-to-HIGH transition of RAB with CL HIGH.
- If more data is clocked into SAA7345 before the LOW-to-HIGH transition of RAB then only the last 8 bits are used.
- If less data is clocked into SAA7345, unpredictable operation will result.
- If the LOW-to-HIGH transition of RAB occurs with CL LOW, the command will be disregarded.

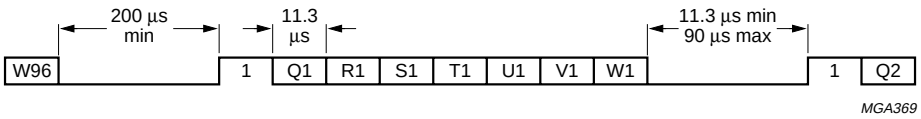


Fig.4 Subcode format and timing at V4 pin.

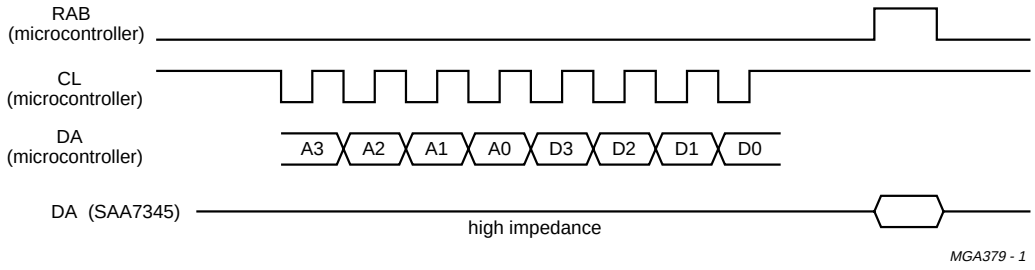
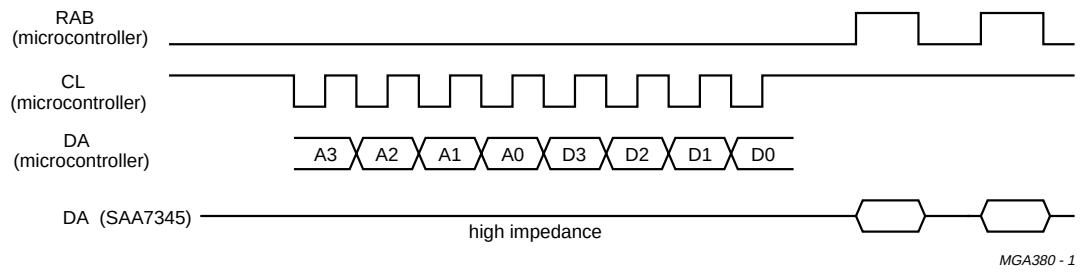


Fig.5 Microcontroller WRITE timing.

WRITING DATA TO SAA7345; REPEAT MODE

The same command can be repeated several times (e.g. for fade function) by applying extra RAB pulses as shown in Fig.6.



Note that CL must stay HIGH between RAB pulses.

Fig.6 Microcontroller WRITE timing; repeat mode.

READING STATUS INFORMATION FROM SAA7345

There are several internal status signals which can be made available on the DA line (Table 1).

Table 1 Internal status signals.

SIGNAL	DESCRIPTION
SUBQREADY-I	LOW if new subcode word is ready in Q-channel register.
MOTSTART1	HIGH if motor is turning at 75% or more of nominal speed.
MOTSTART2	HIGH if motor is turning at 50% or more of nominal speed.
MOTSTOP	HIGH if motor is turning at 12% or less of nominal speed.
PLL Lock	HIGH if Sync coincidence signals are found.
V1	Follows input on V1 pin.
V2	Follows input on V2 pin.
MOTOR-OV	HIGH if the motor servo output stage saturates.

The status signal to be output is selected by status control register (address 0010). The timing for reading the status signal is shown in Fig.7.

Status read operation sequence

- Write appropriate data to register 0010 to select required status signal.
- With RAB LOW; set CL LOW.
- Set RAB HIGH; this will instruct the SAA7345 to output status signal on DA.

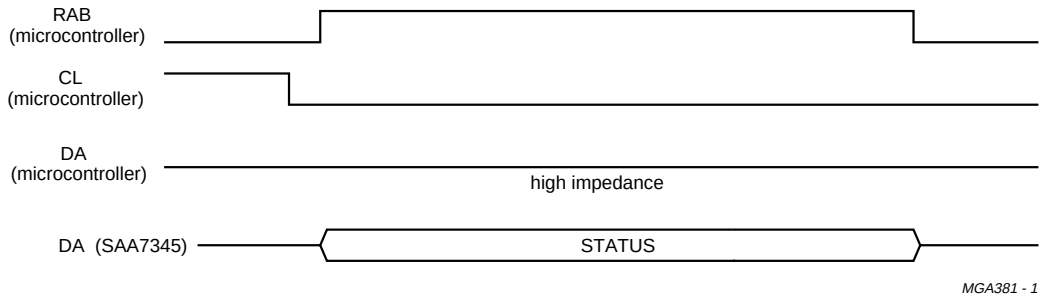


Fig.7 SAA7345 status READ timing.

READING Q-CHANNEL SUBCODE FROM SAA7345

To read Q-channel subcode from SAA7345, the SUBQREADY-I signal should be selected as status signal. The subcode read timing is shown in Fig.8.

Read subcode operation sequence

- Monitor SUBQREADY-I status signal.
- When this signal is LOW, and up to 2.3 ms after its LOW-to-HIGH transition, it is permitted to read subcode.
- Set CL LOW, SAA7345 will output first subcode bit (Q1).
- After subcode read starts, the microcontroller may take as long as it wants to terminate read operation.
- SAA7345 will output consecutive subcode bits after each HIGH-to-LOW transition of CL.
- When enough subcode has been read (1 to 96 bits), stop reading by pulling RAB LOW.

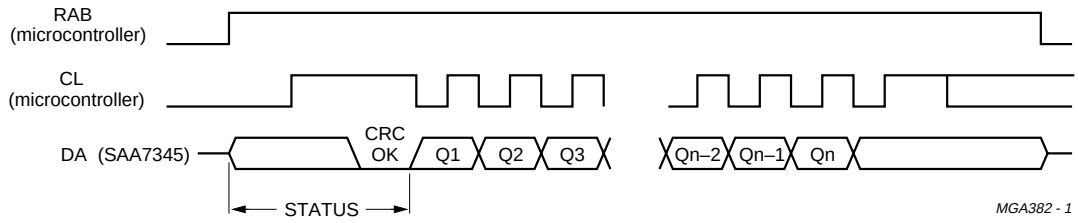


Fig.8 SAA7345 Q-channel subcode READ timing.

PEAK DETECTOR OUTPUT

In place of the CRC-bits (bits 81 to 96), the peak detector information is added to the Q-channel data. The peak information corresponds to the highest audio level (absolute value) and is measured on positive peaks. Only the most significant 8 bits of the peak level are given, in unsigned notation. Bits 81 to 88 contain the LEFT peak value (bit 88 = MSB) and bits 89 to 96 contain the RIGHT channel (bit 96 = MSB). Value is reset after reading Q-channel data.

BEHAVIOUR OF THE SUBQREADY-I SIGNAL

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I signal will react as shown in Fig.9.

When the CRC is good and subcode is being read, the timing in Fig.10 applies.

If t_1 (SUBQREADY-I LOW to end of subcode read) is below 2.6 ms, then t_2 = 13.1 ms (i.e. the microcontroller can read all subcode frames if it completes the read operation within 2.6 ms after subcode ready).

If this criterion is not met, it is only possible to guarantee that t_3 will be below 26.2 ms (approximately).

If subcode frames with failed CRCs are present, the t_2 and t_3 times will be increased by 13.1 ms for each defective subcode frame.

SHARING THE MICROCONTROLLER INTERFACE

When the RAB pin is held LOW by the microcontroller, it is permitted to put any signal on the DA and CL lines (SAA7345 will set output DA to high-impedance). Under this circumstance these lines may be used for another purpose (e.g. TDA1301 microcontroller interface Data and Clock line, see Fig.11).

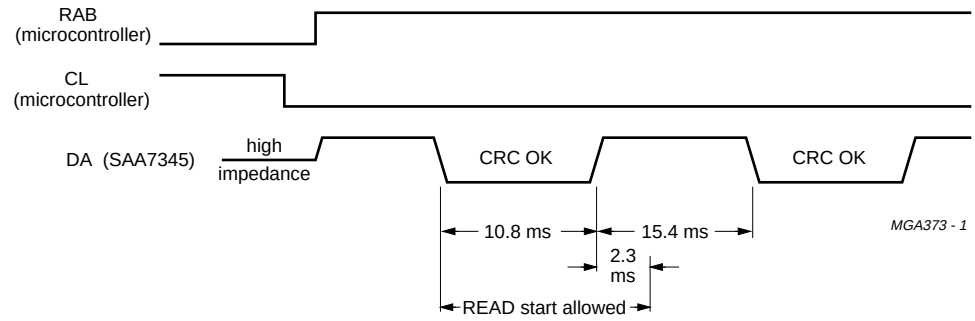


Fig.9 SUBQREADY-I timing when no subcode is read.

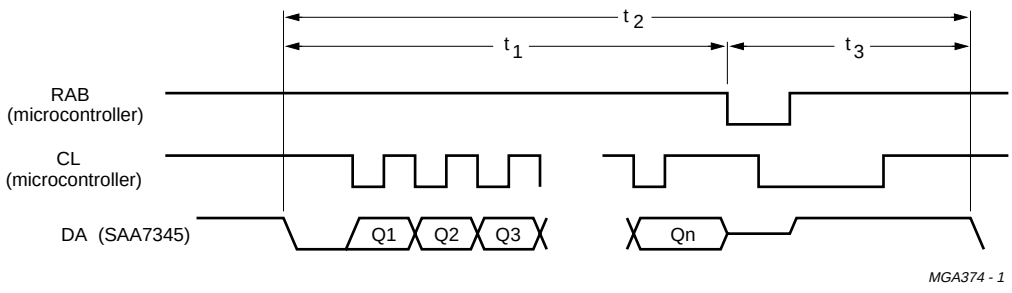


Fig.10 SUBQREADY-I timing when subcode is being read.

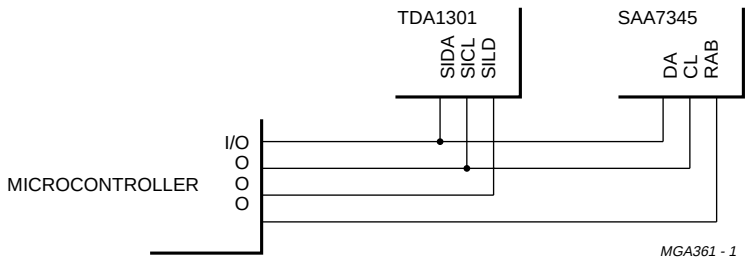


Fig.11 SAA7345 microcontroller interface application diagram.

Table 2 Command registers.

The 'INITIAL' column shows the power-on reset state

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
Fade and Attenuation	0 0 0 0	X 0 0 0	Mute	Reset
		X 0 1 X	Attenuate	
		X 0 0 1	Full Scale	
		X 1 0 0	Step Down	
		X 1 0 1	Step Up	
Motor mode	0 0 0 1	X 0 0 0	Motor off mode	Reset
		X 0 0 1	Motor brake mode 1	
		X 0 1 0	Motor brake mode 2	
		X 0 1 1	Motor start mode 1	
		X 1 0 0	Motor start mode 2	
		X 1 0 1	Motor jump mode	
		X 1 1 1	Motor play mode	
		X 1 1 0	Motor jump mode 1	
		1 X X X	anti-windup active	
		0 X X X	anti-windup off	Reset
Status control	0 0 1 0	X 0 0 0	status = SUBQREADY-I	Reset
		X 0 0 1	status = MOTSTART1	
		X 0 1 0	status = MOTSTART2	
		X 0 1 1	status = MOTSTOP	
		X 1 0 0	status = PLL Lock	
		X 1 0 1	status = V1	
		X 1 1 0	status = V2	
		X 1 1 1	status = MOTOR-OV	
		0 X X X	L channel first at DAC (WCLK normal)	Reset
		1 X X X	R channel first at DAC (WCLK inverted)	

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
DAC output	0 0 1 1	1 0 1 0	I^2S CD-ROM mode	
		1 0 1 1	EIAJ; CD-ROM mode	
		1 1 0 X	I^2S; $4f_s$ mode	Reset
		1 1 1 1	I^2S; $2f_s$ mode	
		1 1 1 0	I^2S; f_s mode	
		0 0 0 X	EIAJ; 16-bit; $4f_s$	
		0 0 1 1	EIAJ; 16-bit; $2f_s$	
		0 0 1 0	EIAJ; 16-bit; f_s	
		0 1 0 X	EIAJ; 18-bit; $4f_s$	
		0 1 1 1	EIAJ; 18-bit; $2f_s$	
		0 1 1 0	EIAJ; 18-bit; f_s	
Motor gain	0 1 0 0	X 0 0 0	Motor gain G = 3.2	Reset
		X 0 0 1	Motor gain G = 4.0	
		X 0 1 0	Motor gain G = 6.4	
		X 0 1 1	Motor gain G = 8.0	
		X 1 0 0	Motor gain G = 12.8	
		X 1 0 1	Motor gain G = 16.0	
		X 1 1 0	Motor gain G = 25.6	
		X 1 1 1	Motor gain G = 32.0	
Motor bandwidth	0 1 0 1	X X 0 0	Motor f_4 = 0.5 Hz	Reset
		X X 0 1	Motor f_4 = 0.7 Hz	
		X X 1 0	Motor f_4 = 1.4 Hz	
		X X 1 1	Motor f_4 = 2.8 Hz	
		0 0 X X	Motor f_3 = 0.85 Hz	Reset
		0 1 X X	Motor f_3 = 1.71 Hz	
		1 0 X X	Motor f_3 = 3.42 Hz	
Motor output configuration	0 1 1 0	X X 0 0	Motor power maximum 37%	Reset
		X X 0 1	Motor power maximum 50%	
		X X 1 0	Motor power maximum 75%	
		X X 1 1	Motor power maximum 100%	
		0 0 X X	MOTO1, MOTO2 pins 3-state	Reset
		0 1 X X	Motor Pulse Width Modulation (PWM) mode	
		1 0 X X	Motor Pulse Density Modulation (PDM) mode	
		1 1 X X	Motor Compact Disc Video (CDV) mode	

REGISTER	ADDRESS	DATA	FUNCTION			INITIAL
			Loop BW (Hz)	Internal BW (Hz)	Low-pass BW (Hz)	
PLL loop filter bandwidth	1 0 0 0	0 0 0 0	1640	525	8400	
		0 0 0 1	3279	263	16800	
		0 0 1 0	6560	131	33600	
		0 1 0 0	1640	1050	8400	
		0 1 0 1	3279	525	16800	
		0 1 1 0	6560	263	33600	
		1 0 0 0	1640	2101	8400	
		1 0 0 1	3279	1050	16800	Reset
		1 0 1 0	6560	525	33600	
		1 1 0 0	1640	4200	8400	
		1 1 0 1	3279	2101	16800	
		1 1 1 0	6560	1050	33600	
PLL loop filter equalization	1 0 0 1	0 0 0 1	PLL 30 ns over-equalization			
		0 0 1 0	PLL 15 ns over-equalization			
		0 0 1 1	PLL nominal equalization			Reset
		0 1 0 0	PLL 15 ns under-equalization			
		0 1 0 1	PLL 30 ns under-equalization			
EBU output	1 0 1 0	X X 0 0	EBU data before concealment			
		X X 1 0	EBU data after concealment and fade			Reset
		X X 1 1	EBU off – output LOW			
		X 0 X X	Level II clock accuracy ($<1000 \times 10^{-6}$)			Reset
		X 1 X X	Level III clock accuracy ($>1000 \times 10^{-6}$)			
		0 X X X	Flags in EBU off			Reset
		1 X X X	Flags in EBU on			
Speed control	1 0 1 1	1 X X X	double-speed mode			
		0 X X X	single-speed mode			Reset
		X 0 X X	33.869 MHz crystal present			Reset
		X 1 X X	16.934 MHz crystal present			
		X X 0 0	standby 1: ‘CD-STOP’ mode (note 1)			Reset
		X X 1 0	standby 2: ‘CD-PAUSE’ mode (note 1)			
		X X 1 1	operating mode			
Versatile pins interface	1 1 0 0	X X X 1	off-track input at V1			
		X X X 0	no off-track input (V1 may be read via status)			Reset
		X X 0 X	Kill-L at KILL output, Kill-R at V3 output			
		X 0 1 X	V3 = 0; single Kill output			Reset
		X 1 1 X	V3 = 1; single Kill output			

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
Versatile pins interface	1 1 0 1	0 0 0 0	4-line motor (using V4, V5)	
		X X 0 1	Q-to-W subcode at V4	
		X X 1 0	V4 = 0	
		X X 1 1	V4 = 1	Reset
		0 1 X X	de-emphasis signal at V5	
		1 0 X X	V5 = 0	
		1 1 X X	V5 = 1	Reset

Note

1. Standby modes = CL, DA and RAB; normal operation.
   a) MISC, SCLK, WCLK, DATA, CL11 and DOBM; 3-state.
   b) CRIN, CROUT, CL16 and CLA; normal operation.
   c) V1, V2, V3, V4 and V5; normal operation.
   d) MOTO1 and MOTO2 - in standby 2 ‘CD-PAUSE’; normal operation.
   e) MOTO1 and MOTO2 - in standby 1 ‘CD-STOP’; held LOW in PWM mode; 3-state in PDM mode.

Error corrector

The error corrector carries out t = 2, e = 0 error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy t = 2, e = 0 means that the error corrector can correct two erroneous symbols per frame and detect all erroneous frames.

The error corrector also contains a flag controller. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of non-correctable errors. They are also output via the EBU signal (DOBM) and the MISC output with I^2S for CD-ROM applications.

The flags output pin CFLG provides information on the state of all error correction and concealment flags.

Audio functions

De-emphasis and phase linearity

When de-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase linearity of the digital oversampling filter to $\leq \pm 1°$ within the band 0 to 16 kHz.

Digital oversampling filter

The SAA7345 contains a 2 to 4 times oversampling filter. The filter specification of the $4 \times$ oversampling filter is given in Table 2 and shown in Fig.12.

These attenuations do not include the sample and hold at the DAC output or the DAC post filter.

When using the oversampling filter, the output level is scaled –0.5 dB down, to avoid overflow on full-scale sinewave inputs (0 to 20 kHz).

Table 3 Digital filter passband characteristics

PASSBAND	ATTENUATION
0 to 19 kHz	≤ 0.001 dB
19 to 20 kHz	≤ 0.03 dB

Table 4 Digital filter stopband characteristics.

STOPBAND	ATTENUATION
24 kHz	≥ 25 dB
24 to 27 kHz	≥ 38 dB
27 to 35 kHz	≥ 40 dB
35 to 64 kHz	≥ 50 dB
64 to 68 kHz	≥ 31 dB
68 kHz	≥ 35 dB
69 to 88 kHz	≥ 40 dB

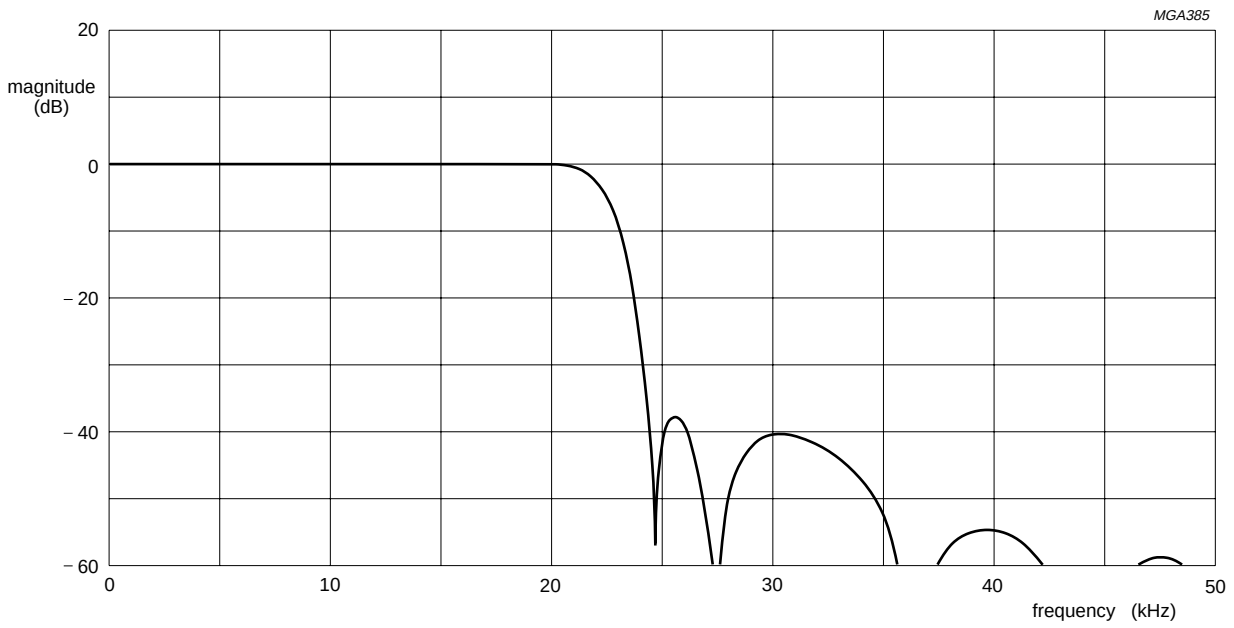


Fig.12 Digital filter characteristics.

CONCEALMENT

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators.

If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.13).

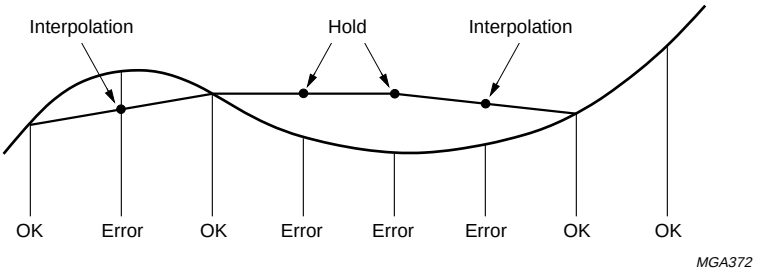


Fig.13 Concealment mechanism.

MUTE, ATTENUATION AND FADE

A digital level controller is present on the SAA7345 which performs the functions of soft mute, attenuation and fade.

Mute and Attenuation

Soft mute is activated by sending the Mute command to the fade control register (address 0000, data X000). The signal will reduced to zero in up to 128 steps (depending on the current position of the fade control), taking a maximum of 3 ms.

Attenuation (–12 dB) is activated by sending the Attenuate command to the fade control register (data X01X).

Attenuation and mute are cancelled by sending the Full Scale command to the fade control register (data X001). It will take 3 ms to ramp the output from mute to the full-scale level.

Fade

The audio output level is determined by the value of the internal fade counter.

$$\text{Level} = \frac{\text{counter}}{128} \times \text{maximum level}$$

- The counter is preset to 128 by the Full Scale command if no oversampling is required.
- The counter is preset to 120 (–0.5 dB scaling) by the Full Scale command if either $2f_s$ or $4f_s$ oversampling is programmed in the DAC output register (address 0011).
- The counter is preset to 32 by the Attenuate command.
- The counter is preset to 0 by the Mute command.

To control the fade counter in a continuous way, the step-up and step-down commands are available (fade control register data X101 and X100). They will increment or decrement the counter by 1 for each register write operation.

- When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see Fig.6).
- A pause of at least 22 μs is necessary between any two step-up or step-down commands.
- When a step-up command is given when the fade counter is already at its full-scale value, the counter will not increment.

DAC Interface

The SAA7345 is compatible with a wide range of Digital-to-Analog Converters. Eleven formats are supported and are shown in Table 5.

All formats are MSB first. f_s is 44.1 kHz in single-speed mode and 88.2 kHz in double-speed mode.

Table 5 DAC interface formats

MODE	DAC CONTROL REGISTER DATA	SAMPLE FREQUENCY	BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1	1 0 1 0	f_s	16	$2.1168 \times n^{(1)}$	CD-ROM (I^2S)	no
2	1 0 1 1	f_s	16	$2.1168 \times n^{(1)}$	CD-ROM (EIAJ)[2]	no
3	1 1 1 0	f_s	16	$2.1168 \times n^{(1)}$	Philips I^2S – 16 bits	yes
4	0 0 1 0	f_s	16	$2.1168 \times n^{(1)}$	EIAJ – 16 bits	yes
5	0 1 1 0	f_s	18	$2.1168 \times n^{(1)}$	EIAJ – 18 bits	yes
6	0 0 0 X	$4f_s$	16	$8.4672 \times n^{(1)}$	EIAJ – 16 bits	yes
7	0 1 0 X	$4f_s$	18	$8.4672 \times n^{(1)}$	EIAJ – 18 bits	yes
8	1 1 0 X	$4f_s$	18	$8.4672 \times n^{(1)}$	Philips I^2S – 18 bits	yes
9	0 0 1 1	$2f_s$	16	$4.2336 \times n^{(1)}$	EIAJ – 16 bits	yes
10	0 1 1 1	$2f_s$	18	$4.2336 \times n^{(1)}$	EIAJ – 18 bits	yes
11	1 1 1 1	$2f_s$	18	$4.2336 \times n^{(1)}$	Philips I^2S – 18 bits	yes

Note

1. n = disc speed.
2. EIAJ is the abbreviation for: Electronic Industries Associated of Japan.

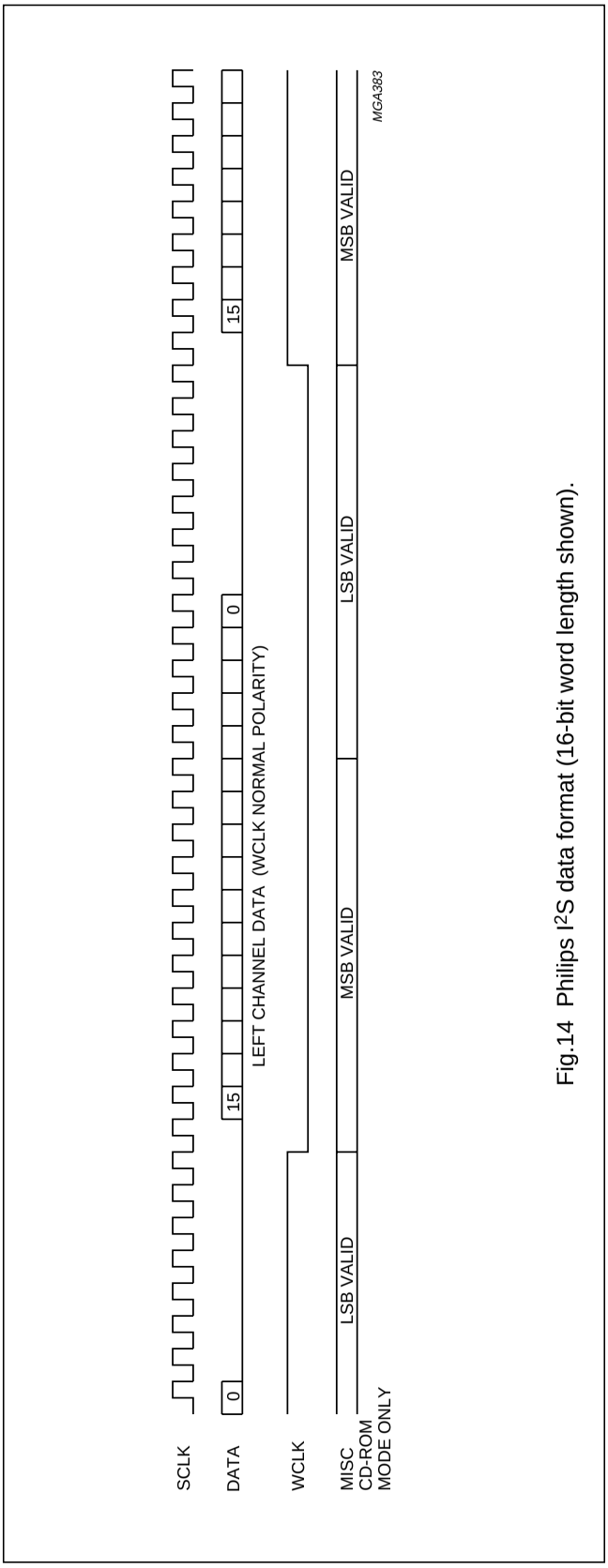


Fig.14 Philips I²S data format (16-bit word length shown).

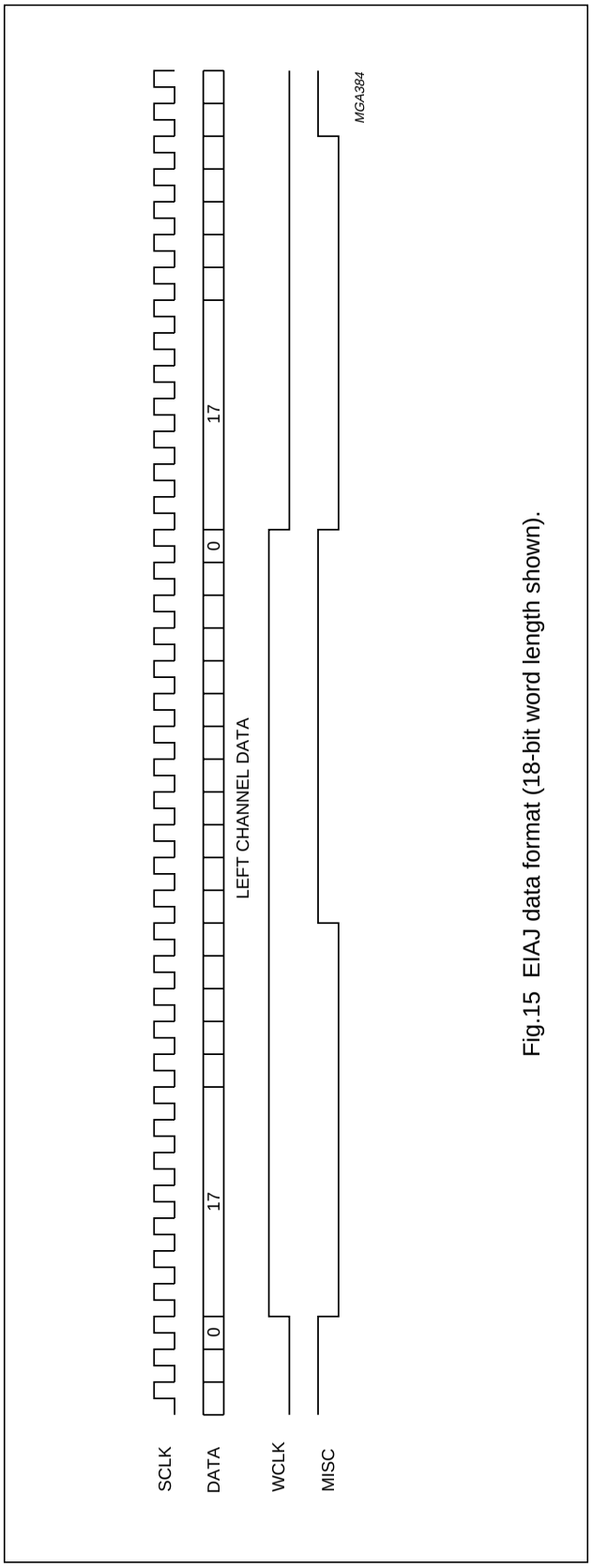


Fig.15 EIAJ data format (18-bit word length shown).

EBU interface

The biphase-mark digital output signal at pin DOBM is in accordance with the format defined by the *"IEC 958"* specification.

Three different modes can be selected via the EBU output control register (address 1010).

Table 6 EBU output modes

EBU CONTROL REGISTER DATA	EBU OUTPUT AT DOBM PIN	EBU VALIDITY FLAG (BIT 28)
X X 1 1	DOBM pin held LOW	–
X X 0 0	data taken before concealment, mute and fade	HIGH if data is non-correctable (concealment flag)
X X 1 0	data taken after concealment, mute and fade	HIGH if data is non-correctable (concealment flag)

FORMAT

The digital audio output consists of 32-bit words (subframes) transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384 (see Table 7).

Table 7 EBU word format

WORD	BITS	FUNCTION
Sync	0 to 3	–
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when bit 3 of EBU control register is set to logic 1
Audio sample	8 to 27	first 4 bits not used (always zero)
Validity flag	28	valid = logic 0
User data	29	used for subcode data (Q-to-W)
Channel status	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

SYNC

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:

- Sync B:
  - Start of a block (384 words), word contains left sample.
- Sync M:
  - Word contains left sample (no block start).
- Sync W:
  - Word contains right sample.

AUDIO SAMPLE

Left and right samples are transmitted alternately.

VALIDITY FLAG

Audio samples are flagged (bit 28 = logic 1) if an error has been detected but was non-correctable. This flag remains the same even if data is taken after concealment.

USER DATA

Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

CHANNEL STATUS

The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is shown in Table 8.

Table 8 EBU channel status

WORD	BITS	FUNCTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic 1; all other bits = logic 0
Clock accuracy	28 to 29	set by EBU control register: 00 = Level II 01 = Level III
Remaining	16 to 27 and 30 to 191	always zero

KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active LOW when silence has been detected for at least 200 ms. Two modes are available, selected by the versatile pins register (address 1100):

1-PIN KILL MODE

Active LOW signal on KILL pin when digital silence has been detected on both LEFT and RIGHT channels for 200 ms.

2-PIN KILL MODE

Independent digital silence detection for left and right channels. The KILL pin is active LOW when digital silence has been detected in the LEFT channel for 200 ms, and V3 is active LOW when digital silence has been detected in the RIGHT channel for 200 ms.

When MUTE is active then the KILL output is forced LOW.

Spindle motor control

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals.

Several output modes are supported:

1. Pulse Density, 2-line (true complement output), 1 MHz sample frequency.
2. PWM output, 2-line, 22.05 kHz modulation frequency.
3. PWM-output, 4-line, 22.05 kHz modulation frequency.
4. CDV motor mode.

The modes are selected via the motor output configuration register (address 0110).

PULSE DENSITY MODE

In the Pulse Density mode the motor output pin MOTO1 is the pulse density modulated motor output signal. A 50% duty cycle corresponds with the motor not actuated, higher duty cycles mean acceleration, lower mean braking.

In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a 1 MHz internal clock signal.

Possible application diagrams are shown in Fig.16.

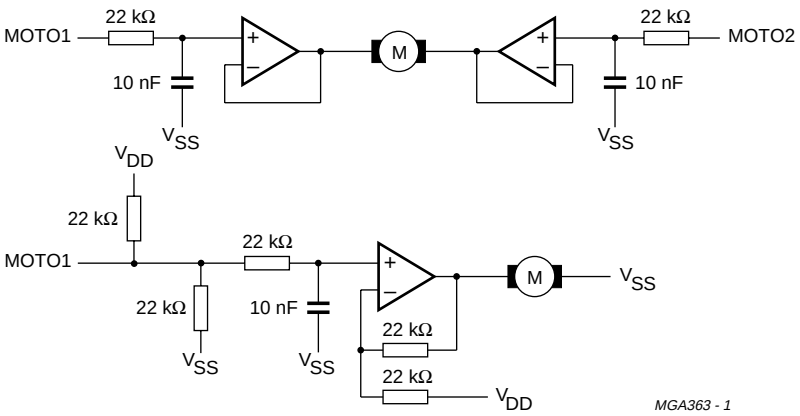


Fig.16 Motor pulse density application diagrams.

PWM MODE, 2-LINE

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output and the motor braking signal is pulse-width modulated on the MOTO2 output.

Figure 17 shows the timing and Fig.18 a typical application diagram.

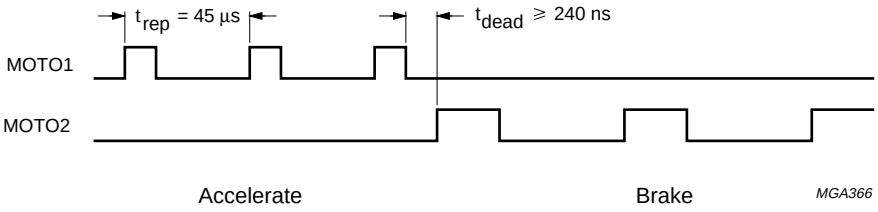


Fig.17 Motor 2-line PWM mode timing.

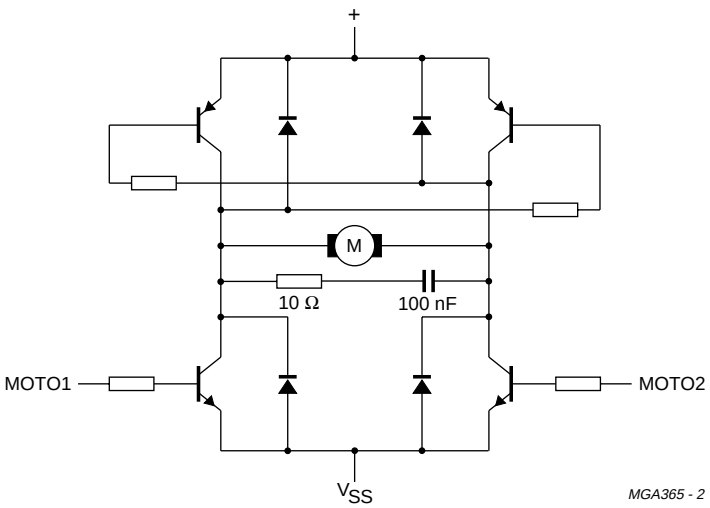


Fig.18 Motor 2-line PWM mode application diagram.

PWM MODE, 4-LINE

Using two extra outputs from the Versatile Pins Interface, it is possible to use the SAA7345 with a 4-input motor bridge.

Figure 19 shows the timing and Fig.20 a typical application diagram.

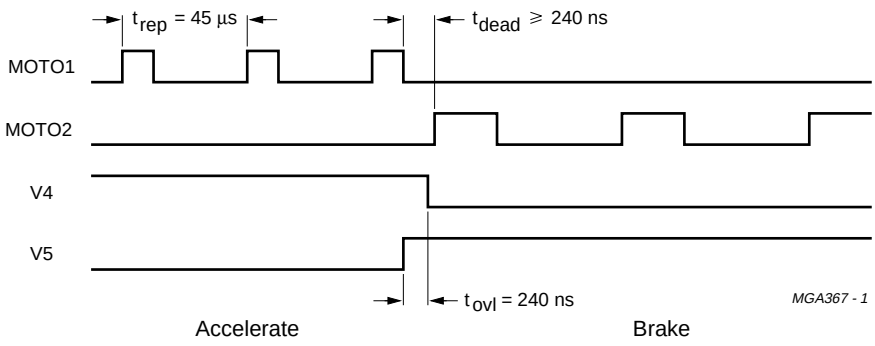


Fig.19 Motor 4-line PWM mode timing.

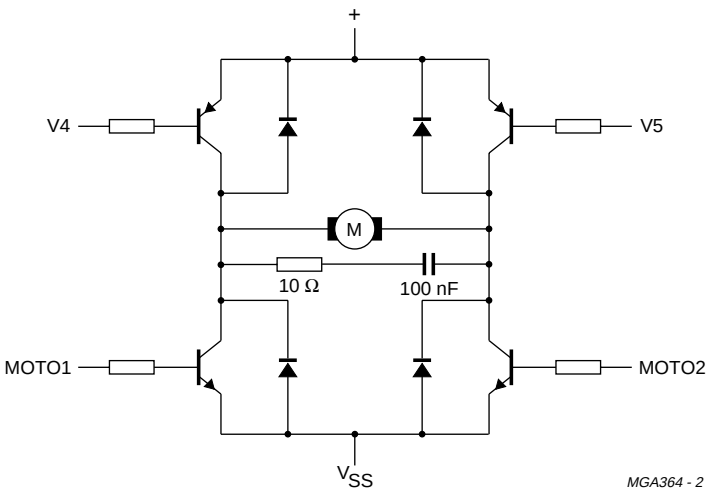


Fig.20 Motor 4-line PWM mode application diagram.

CDV MODE

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin (carrier frequency 300 Hz) and the PLL frequency signal will be put in pulse-density modulated form on the MOTO2 pin (carrier frequency 4.23 MHz). The integrated motor servo is disabled in this mode.

Remark:

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half-full) will result in a PWM output of 60%.

OPERATION MODES

The motor servo has the operation modes as shown in Table 9 and is controlled by the motor mode register (address 0001).

Table 9 Operation modes.

MODE	DESCRIPTION
Start mode 1	Disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller.
Start mode 2	The disc is accelerated as in Start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to Jump mode. The motor status signals are valid (register 0010).
Jump mode	Motor servo enabled but FIFO kept reset at 50%. The audio is muted but it is possible to read the subcode.
Jump mode 1	Similar to Jump mode but motor integrator is kept at zero. Used for long jumps.
Play mode	FIFO released after resetting to 50%. Audio mute released.
Stop mode 1	Disc is braked by applying a negative voltage to the motor. No decisions are involved.
Stop mode 2	The disc is braked as in Stop mode 1, but the PLL will monitor the disc speed. As soon as the disc reaches 12% of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to off mode.
Off mode	Motor not steered.

POWER LIMIT

In Start mode 1, Start mode 2, Stop mode 1 and Stop mode 2, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage via the motor output configuration register (address 0110) to limit current drain during start and stop. The following power limits are possible:

- 100% of maximum (no power limit)
- 75% of maximum
- 50% of maximum
- 37% of maximum.

LOOP CHARACTERISTICS

The gain and cross-over frequencies of the motor control loop can be programmed via the motor gain and bandwidth registers (addresses 0100 and 0101). The possible parameter values are as follows:

Gain: 3.2, 4.0, 6.4, 8.0 12.8, 16, 26.6 or 32.

Cross-over frequency, f_4: –0.5, –0.7, –1.4 or –2.8 Hz.

Cross-over frequency, f_3: –0.85, –1.71 or –3.42 Hz.

FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g. as a result of motor shock), the FIFO will be automatically reset to 50% and the audio interpolator is activated to minimize the effect of data loss.

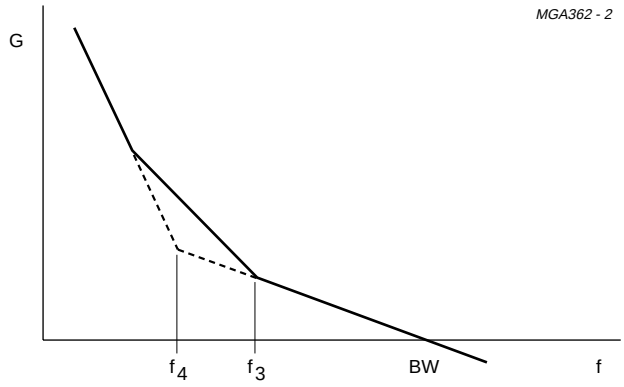


Fig.21 Motor servo mode diagram.

Versatile pins interface

The SAA7345 has five pins that can be reconfigured for different applications as shown in Table 10.

Table 10 Versatile pins

SYMBOL	PIN	TYPE	CONTROL REGISTER ADDRESS	CONTROL REGISTER DATA	FUNCTION
V1	3	input	1 1 0 0	X X X 1	off-track input (from digital servo)
				X X X 0	input may be read via status register (address 0010 data X101)
V2	4	input	–	–	input may be read via status register (address 0010 data X110)
V3	26	output	1 1 0 0	X X 0 X	kill output for right channel
				X 0 1 X	output = logic 0
				X 1 1 X	output = logic 1
V4	25	output	1 1 0 1	0 0 0 0	4-line motor drive (using V4 and V5)
				X X 0 1	Q-to-W subcode output
				X X 1 0	output = logic 0
				X X 1 1	output = logic 1
V5	24	output	1 1 0 1	0 1 X X	de-emphasis output (active HIGH)
				1 0 X X	output = logic 0
				1 1 X X	output = logic 1

Flags Output (CFLG) (open drain output)

A 1-bit flag signal is available at the CFLG pin. This signal shows the status of the error corrector and interpolator and is updated every frame (7.35 kHz).

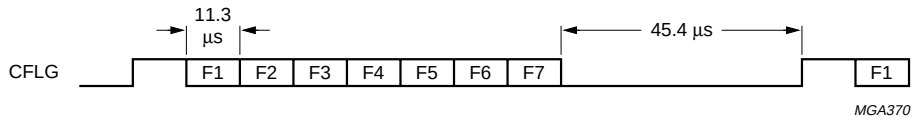


Fig.22 Flags output timing.

Table 11 Meaning of flag bits.

F1	F2	F3	F4	F5	F6	F7	MEANING
0	X	X	X	X	X	X	no absolute time sync
1	X	X	X	X	X	X	absolute time sync
X	0	0	X	X	X	X	C1 frame contained no errors
X	0	1	X	X	X	X	C1 frame contained 1 error
X	1	0	X	X	X	X	C1 frame contained 2 errors
X	1	1	X	X	X	X	C1 frame non-correctable
X	X	X	0	0	X	X	C2 frame contained no errors
X	X	X	0	1	X	X	C2 frame contained 1 error
X	X	X	1	0	X	X	C2 frame contained 2 errors
X	X	X	1	1	X	X	C2 frame non-correctable
X	X	X	X	X	0	0	no interpolations
X	X	X	X	X	0	1	at least one 1-sample interpolation
X	X	X	X	X	1	0	at least one hold and no interpolations
X	X	X	X	X	1	1	at least one hold and one 1-sample interpolation

ABSOLUTE TIME SYNC

The first flag bit (F1) is the absolute time sync signal. It is the FIFO-passed subcode-sync and relates the position of the subcode-sync to the audio data (DAC output).

The flag may be used for special purposes such as synchronization of different players.

FLAGS AT EBU OUTPUT

The CFLG flags are available on bit 4 of the EBU data format when bit 3 of the EBU output control register (address 1010) is set to logic 1.

Double speed mode

Double speed mode is programmed via the Speed control register (address 1011). It is possible to program double speed independent of clock frequency, but optimum performance is achieved with a 33.8688 MHz crystal or a ceramic resonator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–0.5	+6.5	V
$V_{I(max)}$	maximum input voltage		–0.5	V_{DD} + 0.5	V
V_O	output voltage		–0.5	+6.5	V
I_O	output current (continuous)		–	±20	mA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C
V_{es1}	electrostatic handling	note 2	–2000	+2000	V
V_{es2}	electrostatic handling	note 3	–200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	–	22	50	mA
Analog Front End (V_{DD} = 4.5 to 5.5 V); comparator inputs HFIN and HFREF						
f_{clk}	clock frequency		8	–	35	MHz
V_{th}	switching thresholds		1.2	–	V_{DD} – 0.4	V
Analog Front End (V_{DD} = 3.4 to 5.5 V); comparator inputs HFIN and HFREF						
f_{clk}	clock frequency		8	–	20	MHz
V_{tpt}	HFIN input voltage level		–	1.0	–	V
Digital inputs CL and RAB						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	μA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs $\overline{\text{PORE}}$, V1 and V2						
V_{thr}	switching threshold voltage rising		–	–	$0.8V_{DD}$	V
V_{thf}	switching threshold voltage falling		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
R_{PU}	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
t_{rw}	reset pulse width	$\overline{\text{PORE}}$ only	1	–	–	µs
Digital outputs CL16 and CLA						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Digital outputs V4 and V5						
V_{OL}	LOW level output voltage	V_{DD} = 4.5 to 5.5 V; I_{OL} = 10 mA	0	–	1.0	V
		V_{DD} = 3.4 to 5.5 V; I_{OL} = 5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	V_{DD} = 4.5 to 5.5 V; I_{OH} = –10 mA	V_{DD} – 1	–	V_{DD}	V
		V_{DD} = 3.4 V to 5.5 V; I_{OH} = –5 mA	V_{DD} – 1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Open-drain output CFLG						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	C_L = 20 pF; note 1	–	–	30	ns
Open-drain outputs KILL and V3						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-state outputs MISC, SCLK, WCLK, DATA and CL11						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
3-state outputs MOTO1, MOTO2 and DOBM						
V_{OL}	LOW level output voltage	V_{DD} = 4.5 to 5.5 V; I_{OL} = 10 mA	0	–	1.0	V
		V_{DD} = 3.4 to 5.5 V; I_{OL} = 5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	V_{DD} = 4.5 to 5.5 V; I_{OH} = –10 mA	V_{DD} – 1	–	V_{DD}	V
		V_{DD} = 3.4 to 5.5 V; I_{OH} = –5 mA	V_{DD} – 1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	10	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	10	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Digital input/output DA						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; note 1	–	–	15	ns
t_f	output fall time	C_L = 20 pF; note 1	–	–	15	ns
Crystal oscillator input CRIN (external clock)						
g_m	mutual conductance at start-up		–	4	–	mS
R_O	output resistance at start-up		–	11	–	kΩ
C_I	input capacitance		–	–	10	pF
I_{LI}	input leakage current		–10	–	+10	µA
Crystal oscillator output CROUT (see Fig.26)						
f_{xtal}	crystal frequency		8	16.9344	35	MHz
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2S timing						
CLOCK OUTPUT SCLK (see Fig.23)						
t_{cy}	output clock period	sample rate = f_s	–	472.4	–	ns
		sample rate = $2f_s$	–	236.2	–	ns
		sample rate = $4f_s$	–	118.1	–	ns
t_H	clock HIGH time	sample rate = f_s	166	–	–	ns
		sample rate = $2f_s$	83	–	–	ns
		sample rate = $4f_s$	42	–	–	ns
t_L	clock LOW time	sample rate = f_s	166	–	–	ns
		sample rate = $2f_s$	83	–	–	ns
		sample rate = $4f_s$	42	–	–	ns
t_{su}	set-up time	sample rate = f_s	95	–	–	ns
		sample rate = $2f_s$	48	–	–	ns
		sample rate = $4f_s$	24	–	–	ns
t_h	hold time	sample rate = f_s	95	–	–	ns
		sample rate = $2f_s$	48	–	–	ns
		sample rate = $4f_s$	24	–	–	ns
I^2S timing (double speed)						
CLOCK OUTPUT SCLK (see Fig.23)						
t_{cy}	output clock period	sample rate = f_s	–	236.2	–	ns
		sample rate = $2f_s$	–	118.1	–	ns
		sample rate = $4f_s$	–	59.1	–	ns
t_H	clock HIGH time	sample rate = f_s	83	–	–	ns
		sample rate = $2f_s$	42	–	–	ns
		sample rate = $4f_s$	21	–	–	ns
t_L	clock LOW time	sample rate = f_s	83	–	–	ns
		sample rate = $2f_s$	42	–	–	ns
		sample rate = $4f_s$	21	–	–	ns
t_{su}	set-up time	sample rate = f_s	48	–	–	ns
		sample rate = $2f_s$	24	–	–	ns
		sample rate = $4f_s$	12	–	–	ns
t_h	hold time	sample rate = f_s	48	–	–	ns
		sample rate = $2f_s$	24	–	–	ns
		sample rate = $4f_s$	12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microcontroller interface timing (see Figs 24 and 25)						
INPUTS CL AND RAB						
t_L	input LOW time	single speed	500	–	–	ns
		double speed	260	–	–	ns
t_H	input HIGH time	single speed	500	–	–	ns
		double speed	260	–	–	ns
t_r	rise time	single speed	–	–	480	ns
t_f	fall time	double speed	–	–	240	ns
READ MODE						
t_{dRD}	delay time RAB to DA valid		0	–	50	ns
t_{dRZ}	delay time RAB to DA high-impedance		0	–	50	ns
t_{pd}	propagation delay CL to DA	single speed	700	–	980	ns
		double speed	340	–	500	ns
WRITE MODE						
t_{suD}	set-up time DA to CL	single speed; note 2	−700	–	–	ns
		double speed; note 2	−340	–	–	ns
t_{hD}	hold time CL to DA	single speed	–	–	980	ns
		double speed	–	–	500	ns
t_{suCR}	set-up time CL to RAB	single speed	260	–	–	ns
		double speed	140	–	–	ns
t_{dWZ}	delay time DA high-impedance to RAB		50	–	–	ns

Notes

1. Timing reference voltage levels are 0.8 V and V_{DD} − 0.8 V.
2. Negative set-up time means that data may change after clock transition.

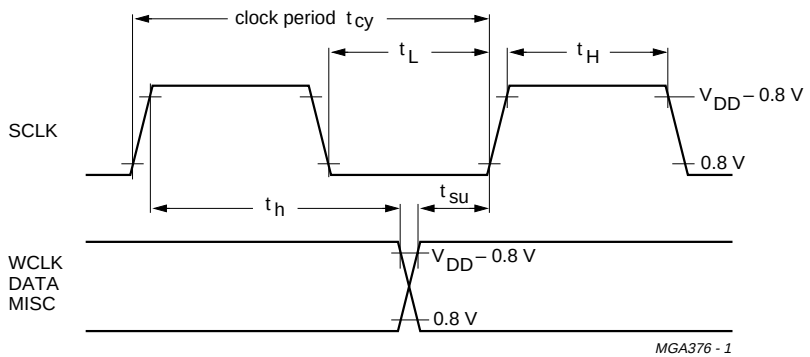


Fig.23 I^2S timing.

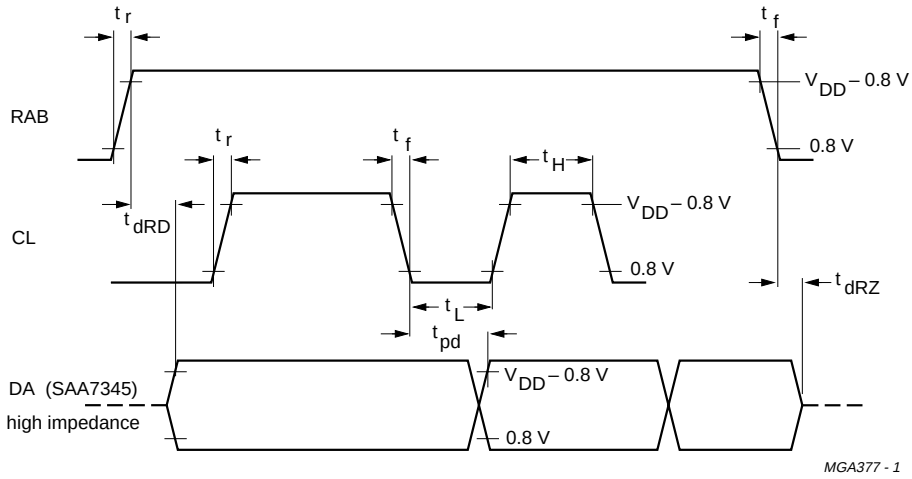


Fig.24 Microcontroller timing; READ mode.

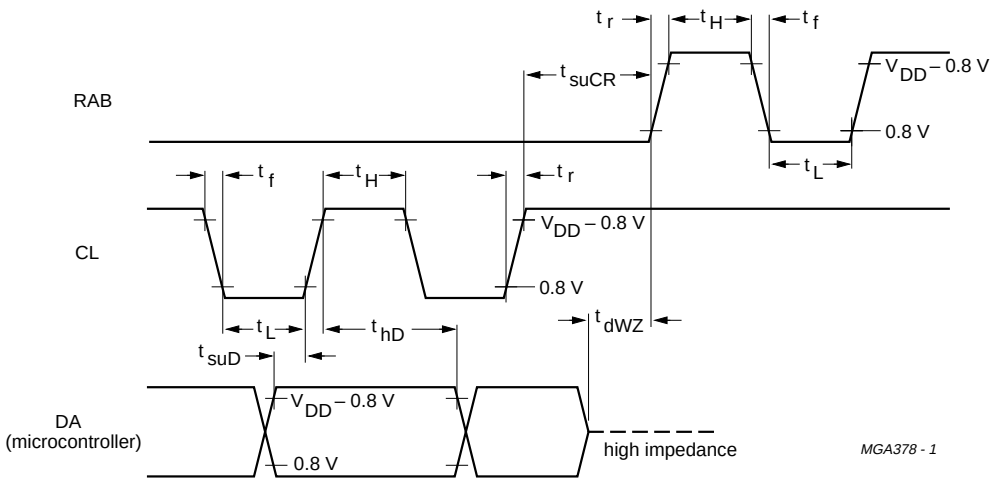


Fig.25 Microcontroller timing; WRITE mode.

APPLICATION INFORMATION

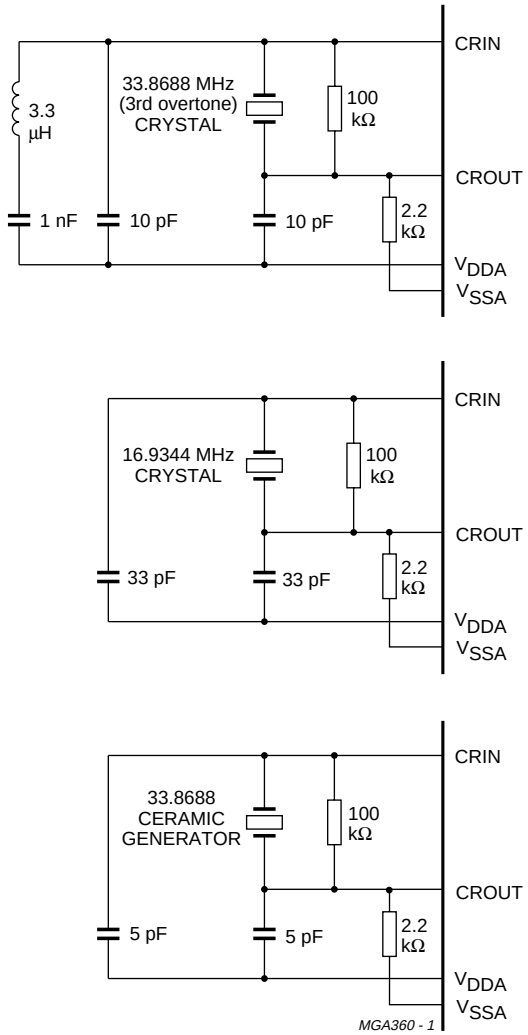
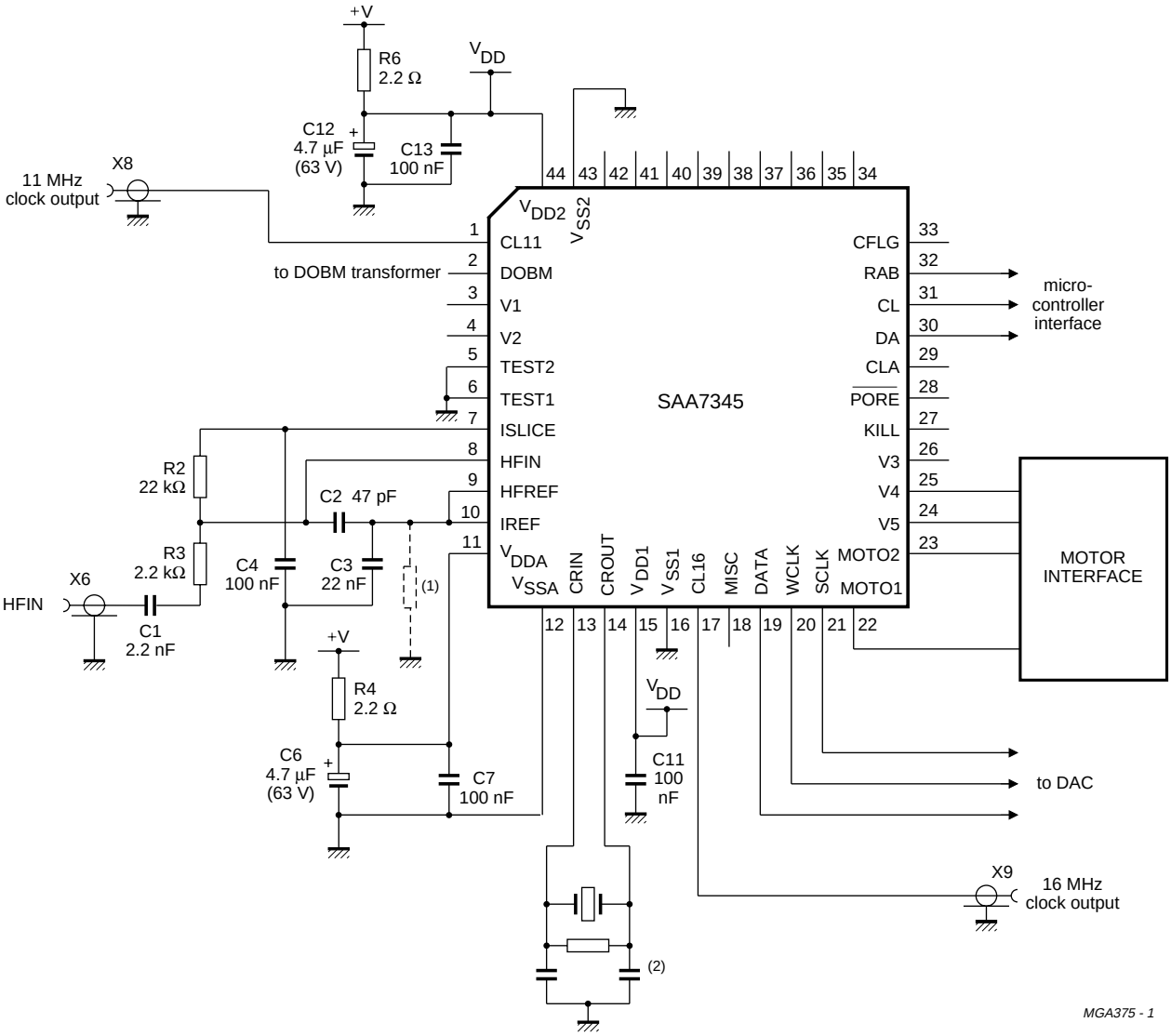


Fig.26 Application circuits for crystal oscillator.



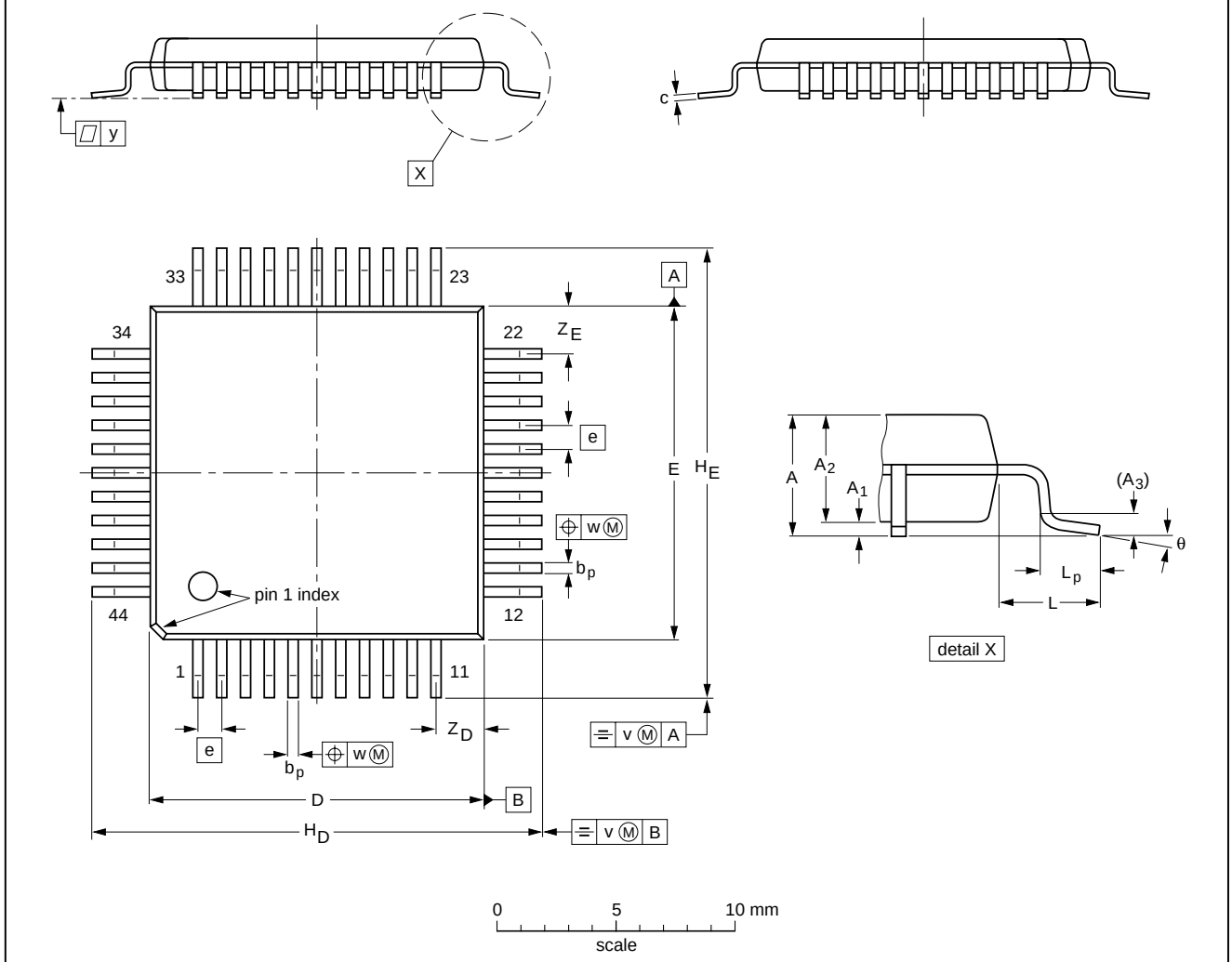
(1) Diagram is for a 5 V application. For 3.4 V applications an additional resistor of 150 kΩ should be added between IREF (pin 10) and ground.

(2) For crystal oscillator circuit see Fig.26.

Fig.27 Typical SAA7345 application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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