PCI-DAS64/M2/16

PCI Bus-Compatible Analog/Digital Data Acquisition & Control Board

User's Guide

MEASUREMENT COMPUTING™

PCI-DAS64/M2/16

Multifunction Analog & Digital I/O

User's Guide

MEASUREMENT COMPUTING™

Document Revision 1, July, 2006

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS64/M2/16 so that you get the most out of its analog, digital, and timing I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *Insta*Cal installation procedure is explained in the *Quick Start Guide*.
Never touch the exposed pins or circuit connections on the board.

Where to find more information

The following electronic documents provide relevant information to the operation of your PCI-DAS64/M2/16.

- MCC's *Specifications: PCI-DAS64/M2/16* (the PDF version of the *Specifications* chapter in this guide) is available on our web site at www.mccdaq.com/pdfs/PCI-DAS64-M2-16.pdf.
- MCC's *Quick Start Guide* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

PCI-DAS64/M2/16 User's Guide (this document) is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-DAS64-M2-16.pdf.

Introducing the PCI-DAS64/M2/16

Overview: PCI-DAS64/M2/16 features

The PCI-DAS64/M2/16 board offers a combination of high speed, channel count and resolution on a single PCI-bus data acquisition board. It offers:

- 64 single-ended or 32 differential 16-bit analog inputs
- 2 MHz sample rate
- Two 16-bit analog outputs
- 100 kHz D/A update rate (16 K FIFO)
- 32 bits of digital I/O
- One 16-bit down-counter
- A variety of analog and digital trigger modes with software-selectable trigger levels and direction

The PCI-DAS64/M2/16 board is designed with Measurement Computing's powerful System Timing Controller (STC) chip. The STC chip controls all A/D sampling and D/A update rates as well as controlling the 8K A/D FIFO, the 8K gain/channel queue and the 16K D/A FIFO buffer. This functionality is based on the STC chip's use of an on-board 32K x 16 SRAM. The STC chip assigns functions to various parts of the SRAM, such as the A/D FIFO buffer, and provides full-speed control and arbitration among the various functions using the various sections of the SRAM buffer.

The STC allows simultaneous full speed A/D sampling, D/A updating and gain/channel queue sequencing, with variable inter-sample timing if desired. The STC chip performs these functions up to 5 MHz, and is available as an OEM component for use in your own designs. The board provides bus-mastering and scatter-gather functionality to assure the desired system timing is maintained.

The PCI-DAS64/M2/16 is completely plug-and-play, with no switches, jumpers or potentiometers on the board. All board addresses, interrupt channels, etc., are set by your computers plug-and-play software. Calibration is performed via software by using on-board trim D/A converters.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS64/M2/16, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

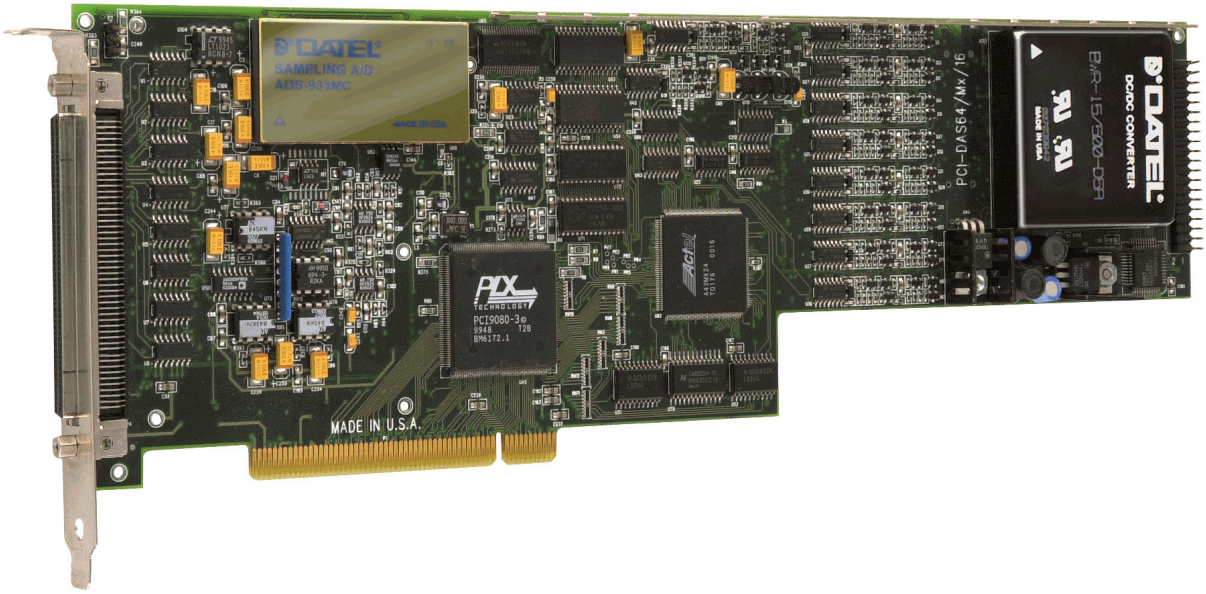
Installing the PCI-DAS64/M2/16

What comes with your PCI-DAS64/M2/16 shipment?

As you unpack your board, make sure each of the items shown below is included.

Hardware

- PCI-DAS64/M2/16



Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-DAS64/M2/16 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables


C100HD50-x


C100MMS-x


C40FF-x


C40-37F-x


BP40-37

- Signal termination and conditioning accessories

  MCC provides signal termination products for use with the PCI-DAS64/M2/16. Refer to the "Field wiring, signal termination and conditioning" section on page 2-7 for a complete list of compatible accessory products.

Unpacking the PCI-DAS64/M2/16

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS64/M2/16 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the PCI-DAS64/M2/16

The PCI-DAS64/M2/16 board is completely plug-and-play, with no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box pops up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the *Measurement Computing Data Acquisition Software* CD and click **OK**.
3. To test your installation and configure your board, run the InstaCal utility you installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 60 minutes before acquiring data. This warm-up period is required for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Calibrate the PCI-DAS64/M2/16 after it has warmed up and immediately before making critical measurements

Use the *Insta*Cal utility to calibrate the PCI-DAS64/M2/16 after it has fully warmed up. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. This pre-measurement calibration insures that your board is operating at the optimum calibration values.

Configuring the PCI-DAS64/M2/16

All hardware configuration options on the PCI-DAS64/M2/16 are software controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (64 single-ended or 32 differential channels), and the edge used for triggering when using an external pacer.

Once configured, any program that uses Measurement Computing's Universal Library will initialize the hardware according to these selections.

Connecting the board for I/O operations

Connectors, cables – main I/O connector

Table 2-1 lists the board connectors, applicable cables and compatible accessory boards.

Table 2-1. Main board connector, cables, accessory equipment

Parameter	Specification
Connector type	Main connector: Shielded SCSI 100-pin D-type
	Auxiliary DIO connector: 40-pin header connector
Compatible cables — main connector	▪ C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet. ▪ C100MMS-x, shielded round cable. x = 1, 2, or 3 meters.
Compatible cables — 40-pin auxiliary connector	▪ C40FF-x ▪ C40-37F-x ▪ BP40-37-x
Compatible accessory products using the C100HD50-x cable	CIO-MINI50 (two required) SCB-50
Compatible accessory products using the C100MMS-x cable	CIO-TERM100 SCB-100
Compatible accessory products using the C40FF-x cable	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37-x and the C37FF-x or C37FFS-x cable	SCB-37 CIO-MINI37 CIO-TERMINAL CIO-ERB24 CIO-ERB08 SSR-RACK24 SSR-RACK08

Pinout – main I/O connector

Table 2-2.
32-channel differential mode

Signal Name	Pin		Pin	Signal Name
LLGND	100	• •	50	GND
CH0 IN HI	99	• •	49	CH0 IN LO
CH1 IN HI	98	• •	48	CH1 IN LO
CH2 IN HI	97	• •	47	CH2 IN LO
CH3 IN HI	96	• •	46	CH3 IN LO
CH4 IN HI	95	• •	45	CH4 IN LO
CH5 IN HI	94	• •	44	CH5 IN LO
CH6 IN HI	93	• •	43	CH6 IN LO
CH7 IN HI	92	• •	42	CH7 IN LO
CH8 IN HI	91	• •	41	CH8 IN LO
CH9 IN HI	90	• •	40	CH9 IN LO
CH10 IN HI	89	• •	39	CH10 IN LO
CH11 IN HI	88	• •	38	CH11 IN LO
CH12 IN HI	87	• •	37	CH12 IN LO
CH13 IN HI	86	• •	36	CH13 IN LO
CH14 IN HI	85	• •	35	CH14 IN LO
CH15 IN HI	84	• •	34	CH15 IN LO
LLGND	83	• •	33	LLGND
CH16 IN HI	82	• •	32	CH16 IN LO
CH17 IN HI	81	• •	31	CH17 IN LO
CH18 IN HI	80	• •	30	CH18 IN LO
CH19 IN HI	79	• •	29	CH19 IN LO
CH20 IN HI	78	• •	28	CH20 IN LO
CH21 IN HI	77	• •	27	CH21 IN LO
CH22 IN HI	76	• •	26	CH22 IN LO
CH23 IN HI	75	• •	25	CH23 IN LO
CH24 IN HI	74	• •	24	CH24 IN LO
CH25 IN HI	73	• •	23	CH25 IN LO
CH26 IN HI	72	• •	22	CH26 IN LO
CH27 IN HI	71	• •	21	CH27 IN LO
CH28 IN HI	70	• •	20	CH28 IN LO
CH29 IN HI	69	• •	19	CH29 IN LO
CH30 IN HI	68	• •	18	CH30 IN LO
CH31 IN HI	67	• •	17	CH31 IN LO
D/A GND 0	66	• •	16	+12V
D/A OUT 0	65	• •	15	GND
D/A GND 1	64	• •	14	-12V
D/A OUT 1	63	• •	13	GND
PC +5V	62	• •	12	DIN0
D/A EXTERNAL PACER	61	• •	11	DIN1
EXT. D/A TRIGGER/PACER GATE	60	• •	10	DIN2
SSH OUT / DAC PACER OUT	59	• •	9	DIN3
A/D PACER OUT	58	• •	8	DOUT0
A/D PACER GATE	57	• •	7	DOUT1
ANALOG TRIGGER IN	56	• •	6	DOUT2
A/D START TRIGGER IN	55	• •	5	DOUT3
A/D STOP TRIGGER IN	54	• •	4	CTR1 GATE
A/D EXTERNAL PACER	53	• •	3	CTR1 CLK
EXTERNAL INTERRUPT	52	• •	2	CTR1 OUT
GND	51	• •	1	GND

PCI slot ↓

Table 2-3. 64-channel single-ended mode

Signal Name	Pin		Pin	Signal Name
LLGND	100	• •	50	GND
CH0 IN	99	• •	49	CH32 IN
CH1 IN	98	• •	48	CH33 IN
CH2 IN	97	• •	47	CH34 IN
CH3 IN	96	• •	46	CH35 IN
CH4 IN	95	• •	45	CH36 IN
CH5 IN	94	• •	44	CH37 IN
CH6 IN	93	• •	43	CH38 IN
CH7 IN	92	• •	42	CH39 IN
CH8 IN	91	• •	41	CH40 IN
CH9 IN	90	• •	40	CH41 IN
CH10 IN	89	• •	39	CH42 IN
CH11 IN	88	• •	38	CH43 IN
CH12 IN	87	• •	37	CH44 IN
CH13 IN	86	• •	36	CH45 IN
CH14 IN	85	• •	35	CH46 IN
CH15 IN	84	• •	34	CH47 IN
LLGND	83	• •	33	LLGND
CH16 IN	82	• •	32	CH48 IN
CH17 IN	81	• •	31	CH49 IN
CH18 IN	80	• •	30	CH50 IN
CH19 IN	79	• •	29	CH51 IN
CH20 IN	78	• •	28	CH52 IN
CH21 IN	77	• •	27	CH53 IN
CH22 IN	76	• •	26	CH54 IN
CH23 IN	75	• •	25	CH55 IN
CH24 IN	74	• •	24	CH56 IN
CH25 IN	73	• •	23	CH57 IN
CH26 IN	72	• •	22	CH58 IN
CH27 IN	71	• •	21	CH59 IN
CH28 IN	70	• •	20	CH60 IN
CH29 IN	69	• •	19	CH61 IN
CH30 IN	68	• •	18	CH62 IN
CH31 IN	67	• •	17	CH63 IN
D/A GND 0	66	• •	16	+12V
D/A OUT 0	65	• •	15	GND
D/A GND 1	64	• •	14	-12V
D/A OUT 1	63	• •	13	GND
PC +5V	62	• •	12	DIN0
D/A EXTERNAL PACER	61	• •	11	DIN1
EXT. D/A TRIGGER/PACER GATE	60	• •	10	DIN2
SSH OUT / DAC PACER OUT	59	• •	9	DIN3
A/D PACER OUT	58	• •	8	DOUT0
A/D PACER GATE	57	• •	7	DOUT1
ANALOG TRIGGER IN	56	• •	6	DOUT2
A/D START TRIGGER IN	55	• •	5	DOUT3
A/D STOP TRIGGER IN	54	• •	4	CTR1 GATE
A/D EXTERNAL PACER	53	• •	3	CTR1 CLK
EXTERNAL INTERRUPT	52	• •	2	CTR1 OUT
GND	51	• •	1	GND

PCI slot ↓

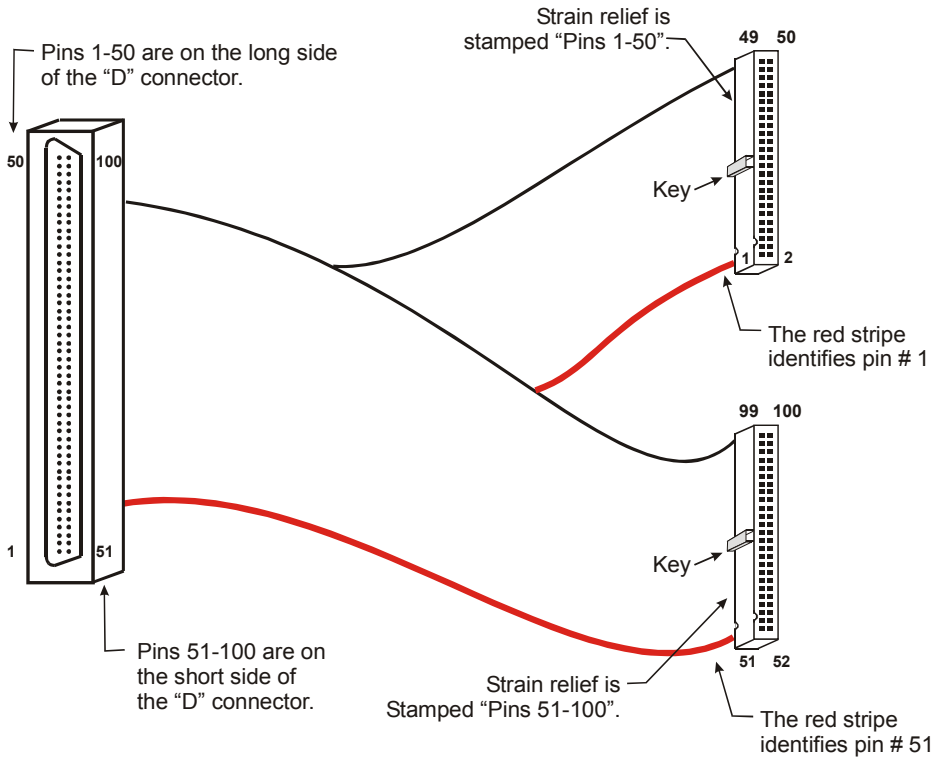


Figure 2-1. C100HD50-x cable connections

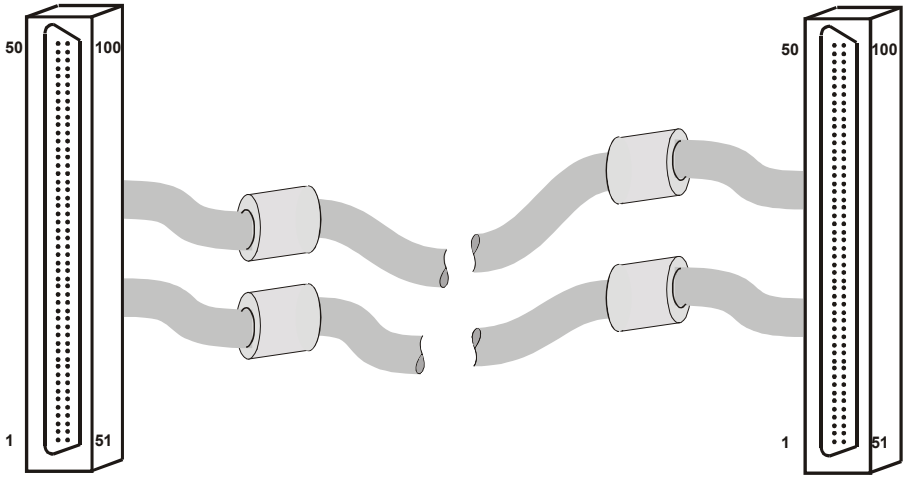


Figure 2-2. C100MMS-x cable

Pin out – auxiliary DIO connector

The auxiliary digital connector can be accessed using a variety of cabling schemes. To bring the 40-pin header out to a bracket at the back of the PC, use a BP40-37 adapter. This terminates in a CIO-DIO series compatible connector to which you can connect a CIO-MINI37 or CIO-TERMINAL screw terminal board using a C37FF-x or C37FFS-x cable. Other options include direct cabling using a C40-37F-x (which maintains CIO-DIO compatibility), or using the C40FF-x cable with the CIO-MINI40 screw terminal board.

Table 2-4. Auxiliary digital connector pin out

NC	1	2	PC +5V
NC	3	4	DIG GND
FIRSTPORTB Bit 7	5	6	FIRSTPORTC Bit 7
FIRSTPORTB Bit 6	7	8	FIRSTPORTC Bit 6
FIRSTPORTB Bit 5	9	10	FIRSTPORTC Bit 5
FIRSTPORTB Bit 4	11	12	FIRSTPORTC Bit 4
FIRSTPORTB Bit 3	13	14	FIRSTPORTC Bit 3
FIRSTPORTB Bit 2	15	16	FIRSTPORTC Bit 2
FIRSTPORTB Bit 1	17	18	FIRSTPORTC Bit 1
FIRSTPORTB Bit 0	19	20	FIRSTPORTC Bit 0
DIG GND	21	22	FIRSTPORTA Bit 7
NC	23	24	FIRSTPORTA Bit 6
DIG GND	25	26	FIRSTPORTA Bit 5
NC	27	28	FIRSTPORTA Bit 4
DIG GND	29	30	FIRSTPORTA Bit 3
NC	31	32	FIRSTPORTA Bit 2
DIG GND	33	34	FIRSTPORTA Bit 1
PC +5V	35	36	FIRSTPORTA Bit 0
DIG GND	37	38	NC
NC	39	40	NC

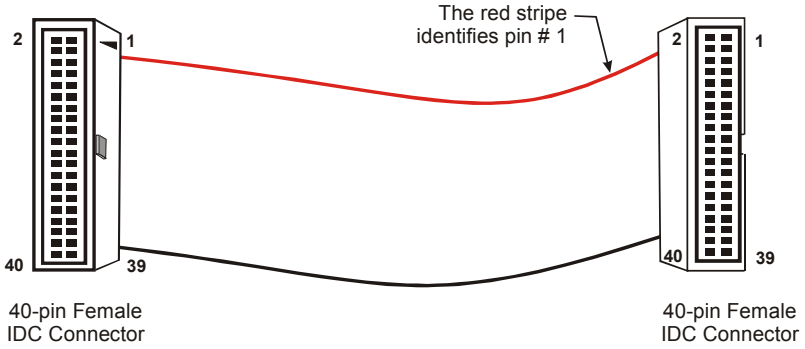


Figure 2-3. C40FF-x cable

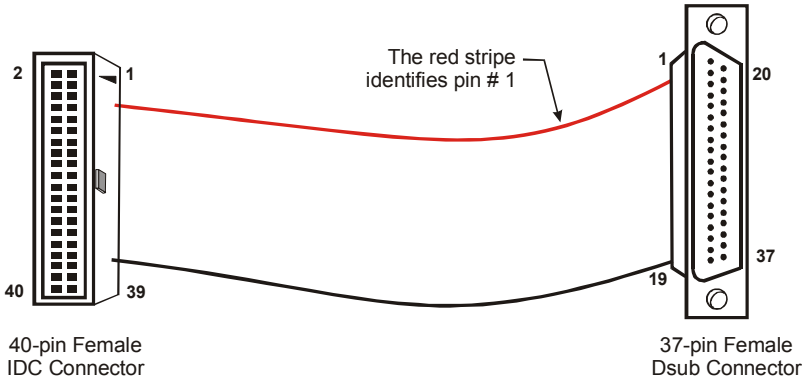


Figure 2-4. C40-37F-x cable

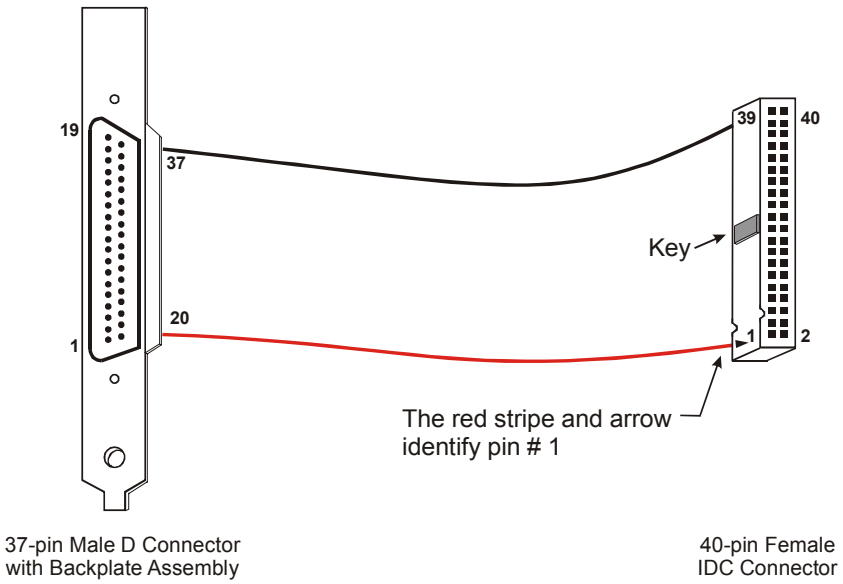


Figure 2-5. BP40-37 cable

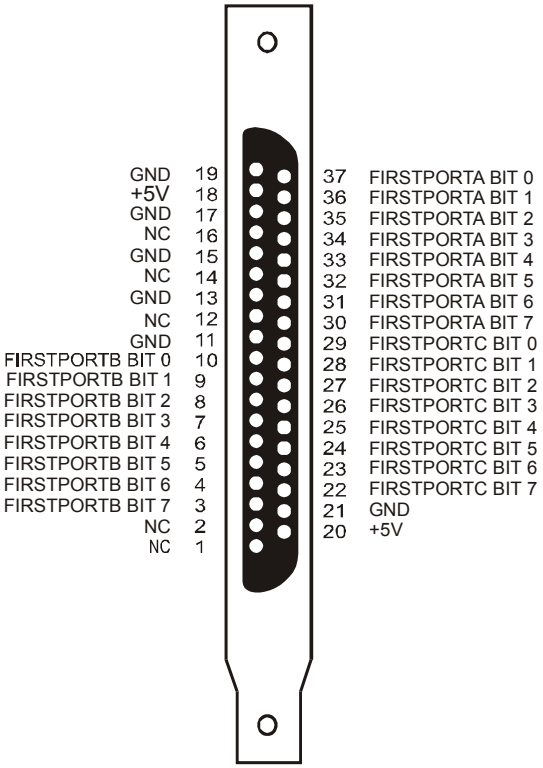


Figure 2-6. BP40-37 cable pin out

40-pin to 37-pin signal mapping

Signal mapping on the C40-37F-x and the BP40-37 cables is not 1:1. Table 2-5 lists the pin numbers of the signals on the 40-pin end and the pin numbers of the associated signals on the 37-pin end.

Table 2-5. Signal mapping on the C40-37F-x and BP40-37F cables

40-pin cable end		37-pin cable end	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	INTERRUPT IN	1	INTERRUPT IN
2	+5V	20	+5V
3	INTERRUPT ENABLE	2	INTERRUPT ENABLE
4	GND	21	GND
5	Port B 7	3	Port B 7
6	Port C 7	22	Port C 7
7	Port B 6	4	Port B 6
8	Port C 6	23	Port C 6
9	Port B 5	5	Port B 5
10	Port C 5	24	Port C 5
11	Port B 4	6	Port B 4
12	Port C 4	25	Port C 4
13	Port B 3	7	Port B 3
14	Port C 3	26	Port C 3
15	Port B 2	8	Port B 2
16	Port C 2	27	Port C 2
17	Port B 1	9	Port B 1
18	Port C 1	28	Port C 1
19	Port B 0	10	Port B 0
20	Port C 0	29	Port C 0
21	GND	11	GND
22	Port A 7	30	Port A 7
23	N/C	12	N/C
24	Port A 6	31	Port A 6
25	GND	13	GND
26	Port A 5	32	Port A 5
27	N/C	14	N/C
28	Port A 4	33	Port A 4
29	GND	15	GND
30	Port A 3	34	Port A 3
31	N/C	16	N/C
32	Port A 2	35	Port A 2
33	GND	17	GND
34	Port A 1	36	Port A 1
35	+5V	18	+5V
36	Port A 0	37	Port A 0
37	GND	19	GND
38	N/C		
39	N/C		
40	N/C		

For digital signal conditioning, you can connect the BP40-37 cable to a C37FF-*x* or C37FFS- *x* cable, and then connect one of these cables to the 37-pin connector on MCC's digital signal conditioning boards. Refer to page 2-10 for a list of compatible boards.

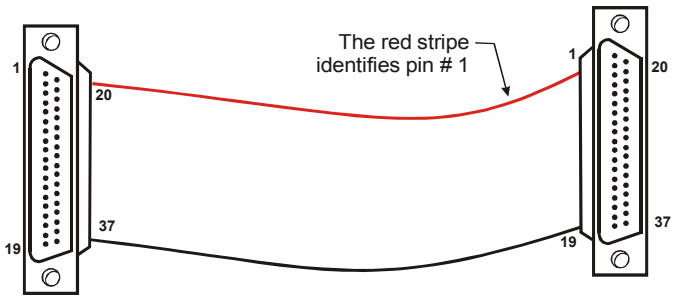


Figure 2-7. C37FF-*x* cable

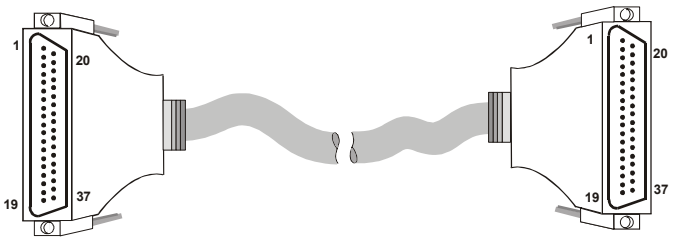


Figure 2-8. C37FFS-*x* cable

Field wiring, signal termination and conditioning

You can use the following accessory boards with the C100HD50-x cable.

- **CIO-MINI50** — 50-pin screw terminal board. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=258.
- **SCB-50 —** 50-conductor, shielded signal connection box. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1168.

You can use the following accessory boards with the C100MMS-x cable.

- **SCB-100 —** 100-conductor, shielded signal connection box. Details are available at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1169.
- **CIO-TERM100** — 100-pin screw terminal board with positions for pull-up resistors. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=281.

You can use the following screw terminal board with the C40FF-x cable.

- **CIO-MINI40** — 40-pin screw terminal board. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=257.

You can use the following screw terminal boards with the C40-37F-x cable directly, or by combining the BP40-37 adapter and C37FF-x or C37FFS-x cable.

- **SCB-37** – 37 conductor, shielded signal connection/screw terminal box. Details on are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1166.
- **CIO-MINI37** – 37-pin universal screw terminal board. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=255.
- **CIO-TERMINAL** — Universal screw terminal with prototype area and circuitry. Includes a 37-pin screw terminal board. Details are available on our web site at http://www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=282.

For digital signal conditioning, you can connect the PCI-DAS64/M2/16 to the following boards using the C40-37F-x cable directly or by combining the BP40-37-x cable with the C37FF-x or C37FFS-x cable.

- **CIO-ERB24** – 24 Form C, 6A relays. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=123&pf_id=241.
- **CIO-ERB08** – Eight Form C, 6A relays. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=123&pf_id=240.
- **SSR-RACK24** – 24-channel solid state module rack. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=122&pf_id=1193.
- **SSR-RACK08** – 24-channel solid state module rack. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=122&pf_id=620.

Programming and Developing Applications

After following the installation instructions in Chapter 2, your board should now be installed and ready for use. Although the board is part of the larger DAS family, in general there may be no correspondence among registers for different boards. Software written at the register level for other DAS models will not function correctly with your board.

Programming Languages

Measurement Computing's Universal Library™ provides access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic® or any other language, please refer to the *Universal Library User's Guide* (available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf)

Packaged Applications Programs

Many packaged application programs, such as SoftWIRE® and HP-VEE™, now have drivers for your board. If the package you own does not have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain drivers.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us by phone, fax or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Register Level Programming

You should use the Universal Library or one of the packaged application programs mentioned above to control your board. Only experienced programmers should try register-level programming. If you need to program at the register level in your application, refer to the *STC Register Map for the PCI-DAS64/Mx/16 Series* (available at www.mccdaq.com/registermaps/RegMapSTC-PCI-DAS64-Mx-16.PDF).

Functional Description

PCI-DAS64/M2/16 block diagram

The PCI-DAS64/M2/16 is a multifunction measurement and control board that provides the following features:

- 32 differential or 64 single-ended 16-bit analog inputs
- Two 16-bit analog outputs
- 32 digital I/O channels
- One 16-bit counter

PCI-DAS64/M2/16 functions are illustrated in the block diagram shown here.

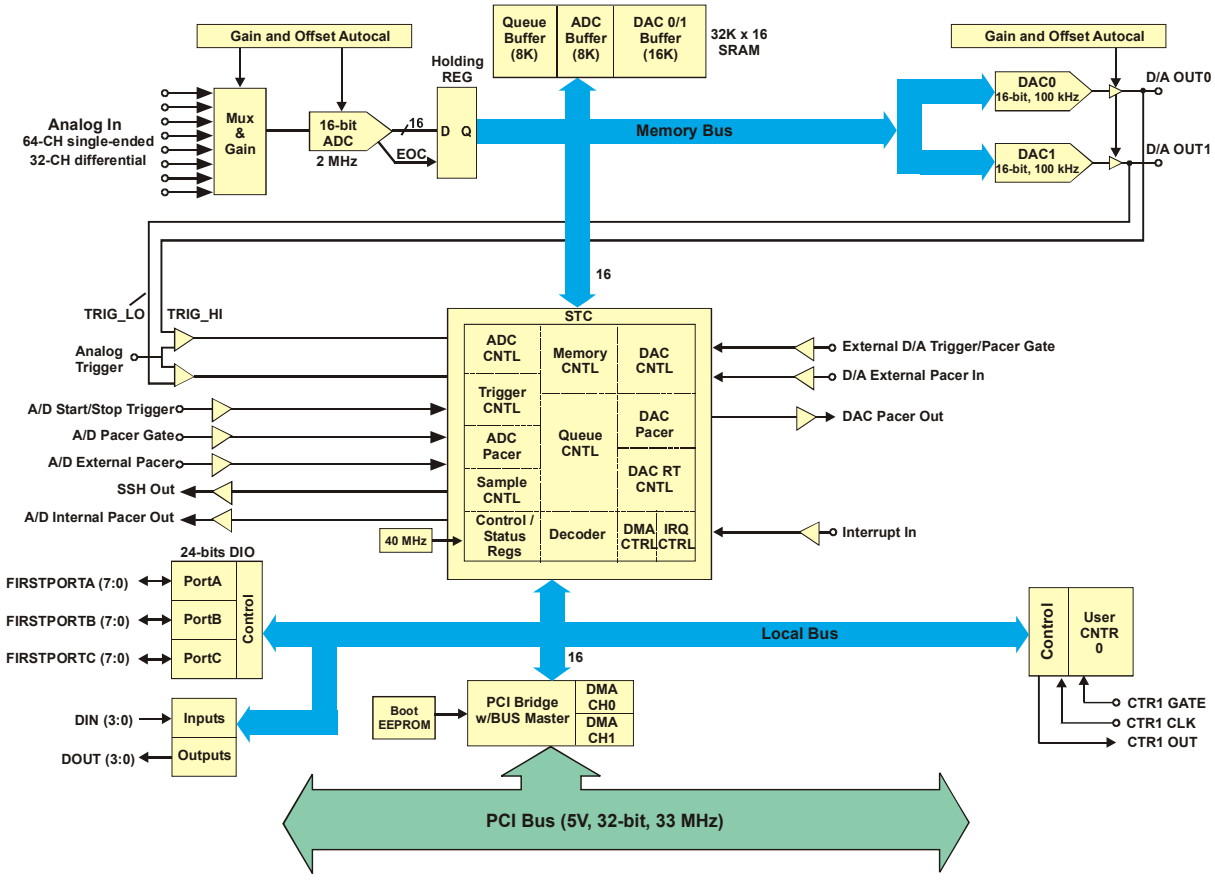


Figure 4-1. PCI-DAS64/M2/16 functional bock diagram

Analog inputs

The PCI-DAS64/M2/16 provides 32 fully differential or 64 single-ended analog inputs. The input mode is software selectable, with no switches or jumpers to set. The PCI-DAS64/M2/16 offers a 2 MHz sample rate. The board offers full speed acquisition in single channel scans, and will perform full accuracy multi-channel scans of up to 1.5 MHz, depending on the operating mode. An 8 K sample gain/channel queue is available making long, complex sample sequencing simple. An 8 K sample FIFO buffer combines with Bus-Master DMA and scatter-gather to assure data taken from the board is transferred into computer memory without missing samples.

Table 4-1 lists the input ranges and resolutions for the available input configurations and gains.

Table 4-1. Analog input range and resolution configurations

Bipolar		Unipolar	
Range	**Resolution**	**Range**	**Resolution**
±5 V	153 μV	0 to 5 V	76.3 μV
±2.5 V	76.3 μV	0 to 2.5 V	38.1 μV
±1.25 V	38.1 μV	0 to 1.25 V	19.1 μV
±0.625 V	19.1 μV		

Burst mode

Channel-to-channel skew is the result of multiplexing the A/D inputs. It is defined as the time between consecutive samples. Burst mode minimizes channel-to-channel skew by clocking the A/D at a high rate between successive samples within a scan, then waiting a specified time before starting a new scan. The PCI-DAS64/M2/16 provides burst mode with a 667 ns minimum sample skew/delay.

Analog output

The PCI-DAS64/M2/16 board provides two high-speed, ±5V 16-bit analog outputs. The outputs are updated via on-board 16 K FIFO buffer and provide a 100 kHz (max) update rate. Repetitive D/A-based waveforms can be stored in on-board memory and generated without requiring ongoing PCI bus transfers. The outputs provide rated accuracy to ±15 mA, are short-circuit-protected (25 mA limit) and are cleared to 0 volts on power-up or reset. The board supports simultaneous full speed operation of both the A/D and D/A.

Digital I/O

The PCI-DAS64/M2/16 provides 32 bits of digital I/O. An 82C55 chip provides 24 bits of CMOS compatible I/O at the board's 40-pin auxiliary digital connector. Four LSTTL-compatible digital inputs and four outputs are provided on the main 100-pin connector. On power up or reset, all I/O ports default to the input state (high impedance).

Counter/timer I/O

The PCI-DAS64/M2/16 provides one 16-bit down counter (1/3 of an 82C54). Clock, gate and output connections are available at the 100-pin user I/O connector.

Calibrating the PCI-DAS64/M2/16

Overview

The PCI-DAS64/M2/16 provides self-calibration of the analog inputs and outputs, eliminating the need for external equipment and user adjustments. All adjustments are made via 8-bit calibration DACs which are referenced to an on-board factory-calibrated standard. The board is fully calibrated at the factory with calibration coefficients stored in nvRAM. At run time, these calibration factors are loaded into system memory and are automatically retrieved each time you specify a different DAC/ADC range.

You can recalibrate any time using factory voltage standards by selecting the **Calibrate** option in *Insta*Cal. A full calibration typically requires less than two minutes. We strongly recommend that you turn your computer on, and allow at least 60 minutes for the internal computer case temperature to stabilize prior to calibrating (or acquiring data with) the board.

A/D calibration is performed at user-selectable conversion frequencies. This is required to reduce any frequency-dependent offset effects across the operating range. When you pull down the **Calibrate** menu option and click on **A/D**, a dialog opens for you to select a calibration frequency (see Figure 5-1). We recommend that you select a frequency as close as possible to the applications' sampling frequency.

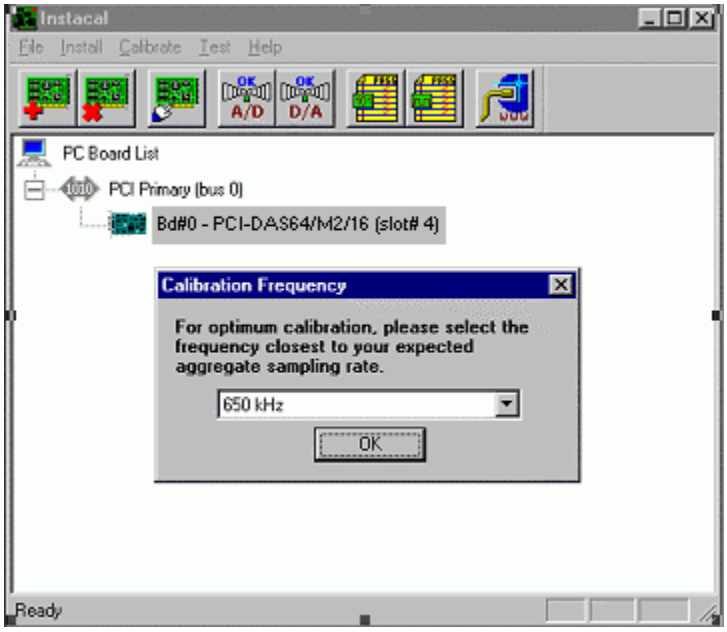


Figure 5-1. *Insta*Cal Calibration Frequency dialog

Table 5-1 lists the available calibration frequencies and recommended sampling frequency ranges. Using this table as a guide, a ±1 LSB offset error relative to the calibrated offset is maintained over a given sampling frequency range. We recommend that you perform A/D calibration at 100 kHz if you intend to use the entire sampling frequency range but do not want to re-calibrate for a given sampling frequency span. In that case, you can expect a ±6 LSB offset drift with respect to the calibrated offset over the full 10 Hz to 2 MHz range.

Table 5-1. Recommended A/D calibration frequencies

Calibration Frequency (kHz)	Min Sampling Frequency (kHz)	Max Sampling Frequency (kHz)
2	0.01	6
15	6	30
50	30	70
100	70	200
300	200	400
650	400	1000
1250	1000	1500
1850	1500	2000

For best results, calibrate the board immediately prior to making your measurements. The high-resolution analog components on the board are somewhat sensitive to temperature and this pre-measurement calibration helps assure your board operates at the same temperature at which it was calibrated.

Calibration theory

Offset calibration for the analog front end is performed via adjustments of the ADC itself. Front-end gain adjustment is performed only via the ADC reference. This strategy was chosen since the gain tolerance of the in-amp circuit is quite good and there is adequate gain tuning range using only the ADC.

A block diagram of the analog front-end calibration system is shown in Figure 5-2.

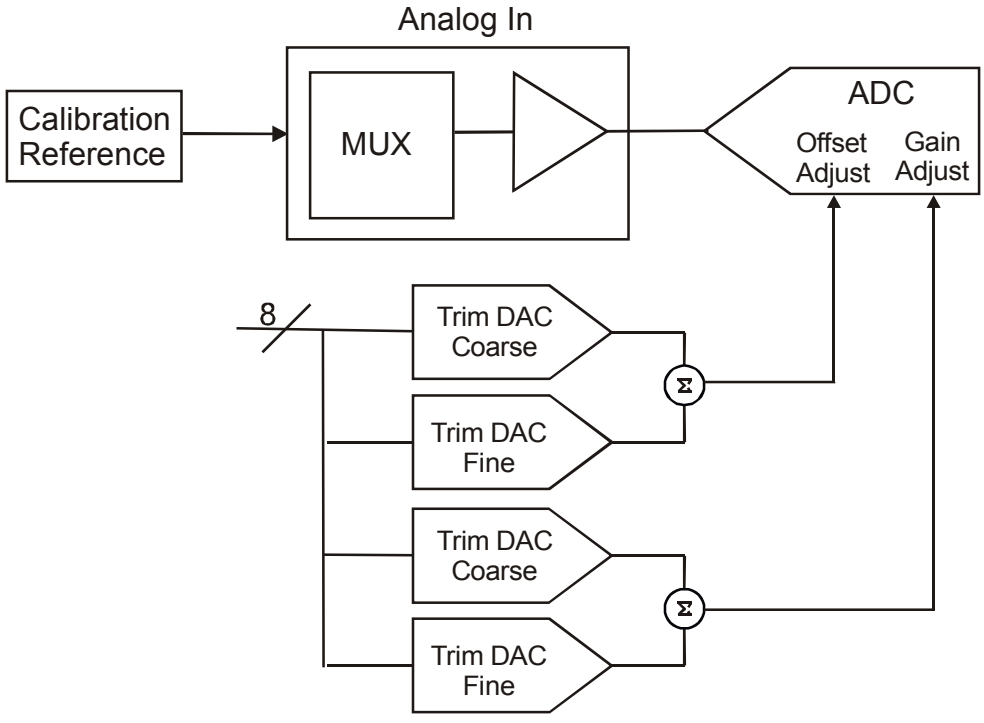


Figure 5-2. Analog front-end calibration system

The analog output circuits are calibrated for gain and offset. Gain calibration of the analog outputs is performed via DAC reference adjustments. Offset adjustments for the analog outputs are made in the output buffer section. The tuning range of this adjustment yields maximum DAC and output buffer offsets.

The calibration scheme for the analog out section is shown in Figure 5-3. This circuit is duplicated for both DAC0 and DAC1

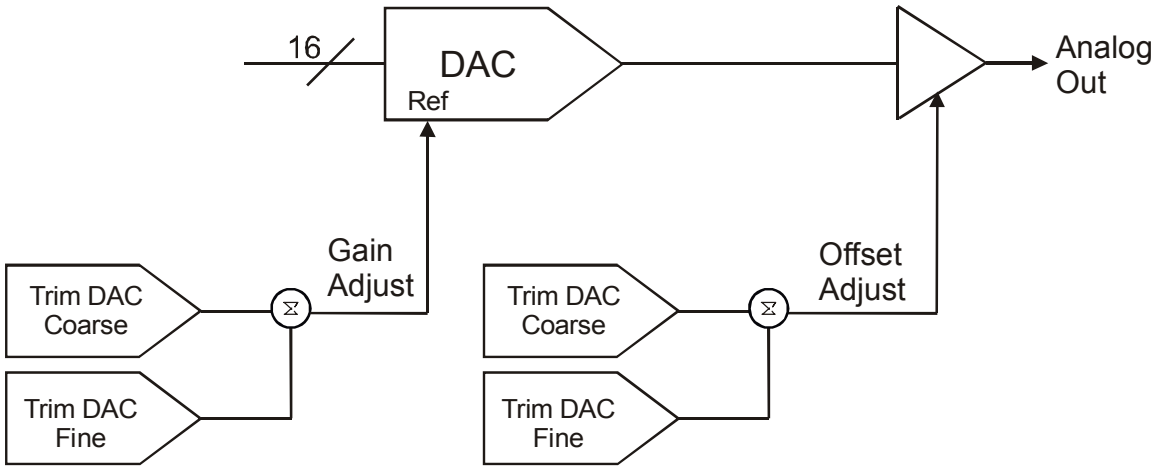


Figure 5-3. Analog out calibration

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Sub-ranging sampling ADC
Resolution	16 bits
Number of channels	32 differential or 64 single-ended, software selectable
Input ranges (software programmable)	±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/bipolar, software selectable
A/D pacing (software programmable)	▪ Internal counter – ASIC ▪ External source (A/D external pacer). The total number of sample clocks must be at least 5 greater than the total number of samples desired. This is required to accommodate the pipelined architecture of the ADC. ▪ Software polled
Burst mode	Software selectable option. Valid for a fixed input range only. Burst rate = 667 nS.
A/D gate sources	▪ External digital (A/D pacer gate) ▪ External analog (analog trigger in)
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window. Trigger levels set by DAC0 and/or DAC1.
A/D trigger sources	▪ External digital (A/D start trigger in and A/D stop trigger in) ▪ External analog (Analog Trigger In)
A/D triggering modes	▪ External digital: Software-configurable for rising or falling edge. ▪ External analog: Software-configurable for positive or negative slope. Trigger levels set by DAC0 and/or DAC1. ▪ Pre-/post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger options.
Data transfer	▪ From 8 k RAM buffer via DMA (demand or non-demand mode) using scatter gather. ▪ Programmed I/O
Configuration memory	*8 K words*
Channel/gain queue	Up to 8 K elements. Programmable channel, gain, and offset.
A/D conversion time	*500 nS*
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.

System throughput

Table 2. System throughput specifications

Condition	Calibration coefficients	Max ADC rate
1. Single channel, single input range.	Per specified range	2.0 MS/s
2. Multiple-channel, single-input range: ±5 V, ±2.5 V, ±1.25 V, 0 to 5 V, 0 to 2.5 V	Per specified range	1.5 MS/s
3. Multiple channel, single input range: ±0.625 V, 0 to 1.25 V	Per specified range	750 kS/s
4. Single channel, multiple input ranges.	Default to value for `cbAInScan()` range	500 kS/s
5. Multiple channels, multiple ranges. All samples in unipolar *or* bipolar bode.	Default to value for `cbAInScan()` range	500 kS/s
6. Multiple channels, multiple ranges. All samples in unipolar *and/or* bipolar bode.	Default to value for `cbAInScan()` range	500 kS/s
7. Multiple-channel, switching unipolar/bipolar mode, single-input range.	Default to value for `cbAInScan()` range	750 kS/s

Note 1: For conditions 1-3, specified accuracy is maintained at rated throughput. Conditions 4-7 apply calibration coefficients which correspond to the range value selected in `cbAInScan()`. These coefficients remain unchanged throughout the scan. Errors of up to 25 counts may be incurred when switching gains while in bipolar or unipolar mode only (conditions 4 and 5). Errors of up to 500 counts may be incurred when mixing unipolar/bipolar modes (conditions 6 and 7).

Accuracy

A 100 kS/s sampling rate, single-channel operation and a 60-minute warm-up. Accuracies are listed for operational temperatures within ±2ºC of internal calibration temperature. Calibrator test source high side tied to channel 0 and low side tied to low-level ground at the user connector

Table 3. Analog input — absolute accuracy specifications

Range	Absolute accuracy
±5.000 V	±6.0 LSB
±2.500 V	±8.0 LSB
±1.250 V	±8.0 LSB
±0.625 V	±10.0 LSB
0 V to +5.000 V	±8.0 LSB
0 V to +2.500 V	±11.0 LSB
0 V to +1.250 V	±13.0 LSB

Table 4. Analog input — typical accuracy specifications

Range	Typical accuracy
±5.000 V	±5.5 LSB
±2.500 V	±7.5 LSB
±1.250 V	±7.5 LSB
±0.625 V	±9.5 LSB
0 V to +5.000 V	±7.5 LSB
0 V to +2.500 V	±10.5 LSB
0 V to +1.250 V	±12.5 LSB

Each PCI-DAS64/M2/16 is tested at the factory to assure the board's overall error does not exceed accuracy limits shown in Table 3.

Typical accuracy is derived directly from the various component typical errors. The information in Table 4 assumes that each of the errors contributes in the same direction.

Table 5. Analog input — accuracy components specifications

Range	Gain error	Offset error	DLE	ILE
±5.000 V	±3.0 max, ±2.0 typ	±3.0 max, ±2.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±2.500 V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±1.250 V	±3.0 max, ±2.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
±0.625 V	±5.0 max, ±4.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 5.000 V	±4.0 max, ±3.0 typ	±4.0 max, ±3.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 2.500 V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ
0 to + 1.250 V	±6.0 max, ±5.0 typ	±5.0 max, ±4.0 typ	±1.0 max, ±0.5 typ	±2 max, ±1.0 typ

As shown in Table 5, total board error is a combination of *gain*, *offset*, *differential linearity error* (DLE), and *integral linearity error* (ILE). The theoretical worst-case error of the board can be calculated by summing these component errors. Worst-case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full-scale 100 Hz triangle wave is input on channel 1, and channel 0 is tied to analog ground at the 100-pin user connector. Table 6 summarizes the influence of channel 1 on channel 0 with the effects of noise removed. The residue on channel 0 is described in LSBs.

Table 6. Crosstalk specifications

Range	Crosstalk (LSB $_{pk-pk}$)	Per channel rate (kS/s)	ADC rate (kS/s)
±5.000 V	15	750	1500
±2.500 V	15	750	1500
±1.250 V	20	750	1500
±0.625 V	8	375	750
0 V to + 5.000 V	15	750	1500
0 V to + 2.500 V	20	750	1500
0 V to + 1.250 V	8	375	750

Table 7. Analog input drift specifications

Analog input full-scale gain drift	+0.3 LSB/°C typical
Analog input zero drift	+2.1 LSB/°C typical
Overall analog input drift	±2.4 LSB/°C typical
Common mode range	±5 V
CMRR @ 60Hz	-90 dB
Input leakage current	*2.3 nA*
Input impedance	*10 x 10*^{11} Ω
Absolute maximum input voltage	*±15 V*
Warm-up time	60 minutes

Noise performance

Table 8 summarizes the worst case noise performance for the PCI-DAS64/M2/16. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single-channel sampling rate. Specification applies to both single-ended and differential modes of operation.

Table 8. Noise performance specifications

Range	±2 counts	±1 count	MaxCounts	LSBrms (Note 2)
± 5.000 V	60%	40%	22	3.3
± 2.500 V	60%	40%	24	3.6
± 1.250 V	60%	40%	26	3.9
± 0.625 V	45%	30%	32	4.8
0 to +5.000 V	60%	40%	24	3.6
0 to +2.500 V	60%	40%	26	3.9
0 to +1.250 V	45%	30%	32	4.8

Note 2: RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

Analog output

Table 9. Analog output specifications

Resolution	*16-bits*
Number of channels	*2*
Voltage range	±5 V
Monotonicity	*Guaranteed monotonic over temperature*
Analog output zero drift	±1.6 LSB/°C
Overall analog output drift	±4.0 LSB/°C
Slew rate	2.5 V/µs
Settling time	FS step to .0008%: 6µs max, all ranges
Current drive	±15 mA
Output short-circuit duration	*Indefinite @25 mA*
Output coupling	*DC*
Output impedance	0.1 Ω
Power up and reset	DACs cleared to 0 V±75 mV max

Accuracy

Table 10. Analog output — absolute accuracy specifications

Range	Absolute accuracy
± 5 V	±16.0 LSB

Table 11 Analog output — accuracy components specifications

Range	Gain error (LSB)	Offset error (LSB)	DLE (LSB)	ILE (LSB)
±5.0 V	±10.0 max	±5.0 max	±1.0 max	±1.0 max

Each PCI-DAS64/M2/16 is tested at the factory to assure the board's overall error does not exceed the absolute accuracy limits listed in Table 10.

Analog output pacing and triggering

Table 12. Analog output pacing and triggering specifications

D/A pacing (software-programmable)	Internal counter – ASIC
	External source (D/A external pacer)
	Software paced
D/A gate sources (software-programmable)	External digital (external D/A trigger/pacer gate)
	External analog (analog trigger in)
D/A gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Software-configurable for above or below reference. Gating levels are set by DAC0 or DAC1.
D/A trigger sources	External digital (external D/A trigger/pacer gate)
	Software triggered
D/A triggering modes	External digital: Software-configurable for rising or falling edge.
Data transfer	From 16 k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
	100 kS/s max per channel

Digital input/output

Table 13. Digital I/O specifications

Digital type (main connector)	Output: 74LS175
	Input: 74LS244
Configuration	Four inputs, four outputs (DIN0 through DIN3; DOUT0 to DOUT3)
Output high voltage (IOH = -0.4 mA)	*2.7 V min*
Output low voltage (IOL = 8 mA)	*0.5 V max*
Input high voltage	*2.0 V min, 7 volts absolute max*
Input low voltage	*0.8 V max, –0.5 volts absolute min*
Digital type (digital I/O connector)	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	2 banks of 8 and 2 banks of 4, or
	3 banks of 8 or
	2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2.5 mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)
SSH output	TTL compatible output, HOLD is asserted from start of the conversion for Channel 0 through conversion of the last channel in the scan. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
SSH polarity	HOLD high (default) or HOLD low, software selectable

Interrupts

Table 14. Interrupt specifications

Interrupts	PCI INTA# - Mapped to IRQ*n* via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC interrupt	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC interrupt sources (software-programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.
	DAC_RETRANSMIT:	Interrupt is generated when the end of a waveform sequence has occurred in retransmit mode.
External interrupt	Interrupt is generated via edge-sensitive transition on the External Interrupt pin. Rising/falling edge polarity software selectable.	

Counters

Table 15. Counter specifications

User counter type	82C54
Configuration	One down counter, 16-bits. Counters 2 and 3 not used.
Counter 1 source	External, from connector (CTR1 CLK)
Counter 1 gate	Available at connector (CTR1 GATE).
Counter 1 output	Available at connector (CTR1 OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 nS min*
Low pulse width (clock input)	*50 nS min*
Gate width high	*50 nS min*
Gate width low	*50 nS min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

Pacer

Table 16. Pacer specifications

ADC pacer type	ASIC
Configuration	One down counter, 24 bits (1 scan interval, 1 sample interval)
ADC pacer source	40 MHz internal source
ADC pacer gate	Internally controlled by software/hardware trigger.
ADC pacer out	ADC pacer clock, available at user connector (A/D PACER OUT)
DAC pacer type	ASIC
Configuration	One down counter, 24 bits (1 scan interval, 1 sample interval)
DAC pacer source	40 MHz or 100 kHz internal source. Software-selectable.
DAC pacer gate	Internally controlled by software/hardware trigger.
DAC pacer out	DAC pacer clock. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT (default) or D/A PACER OUT.
Internal pacer crystal oscillator	40 MHz
Frequency accuracy	50 ppm

Power consumption

Table 17. Power specifications

+5 V	2.9 A typical, 3.3 A max
+12 V	10 mA max.

Environmental

Table 18. Environmental specifications

Operating temperature range	0 to 50 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 19. Mechanical specifications

Card dimensions	315 mm (L) x 100.6 mm (W) x 16 mm (H)

Main connector and pin out

Table 20. Main connector and pinout specifications

Parameter	Specification
Connector type	Shielded SCSI 100-pin D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet.
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters.
Compatible accessory products using the C100HD50-x cable	CIO-MINI50 (two required) SCB-50
Compatible accessory products using the C100MMS-x cable	CIO-TERM100 SCB-100

Differential mode pin out

Table 21. 32-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5 V
13	GND	63	D/A OUT 1
14	-12 V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12 V	66	D/A GND 0
17	CH31 IN LO	67	CH31 IN HI
18	CH30 IN LO	68	CH30 IN HI
19	CH29 IN LO	69	CH29 IN HI
20	CH28 IN LO	70	CH28 IN HI
21	CH27 IN LO	71	CH27 IN HI
22	CH26 IN LO	72	CH26 IN HI
23	CH25 IN LO	73	CH25 IN HI
24	CH24 IN LO	74	CH24 IN HI
25	CH23 IN LO	75	CH23 IN HI
26	CH22 IN LO	76	CH22 IN HI
27	CH21 IN LO	77	CH21 IN HI
28	CH20 IN LO	78	CH20 IN HI
29	CH19 IN LO	79	CH19 IN HI
30	CH18 IN LO	80	CH18 IN HI
31	CH17 IN LO	81	CH17 IN HI
32	CH16 IN LO	82	CH16 IN HI
33	LLGND	83	LLGND
34	CH15 IN LO	84	CH15 IN HI
35	CH14 IN LO	85	CH14 IN HI
36	CH13 IN LO	86	CH13 IN HI
37	CH12 IN LO	87	CH12 IN HI
38	CH11 IN LO	88	CH11 IN HI
39	CH10 IN LO	89	CH10 IN HI
40	CH9 IN LO	90	CH9 IN HI
41	CH8 IN LO	91	CH8 IN HI
42	CH7 IN LO	92	CH7 IN HI
43	CH6 IN LO	93	CH6 IN HI
44	CH5 IN LO	94	CH5 IN HI
45	CH4 IN LO	95	CH4 IN HI
46	CH3 IN LO	96	CH3 IN HI
47	CH2 IN LO	97	CH2 IN HI
48	CH1 IN LO	98	CH1 IN HI
49	CH0 IN LO	99	CH0 IN HI
50	GND	100	LLGND

Single-ended mode pin out

Table 22. 64-channel single-ended mode pin out

Pin	Signal name	Pin	Signal name
1	GND	51	GND
2	CTR1 OUT	52	EXTERNAL INTERRUPT
3	CTR1 CLK	53	A/D EXTERNAL PACER
4	CTR1 GATE	54	A/D STOP TRIGGER IN
5	DOUT3	55	A/D START TRIGGER IN
6	DOUT2	56	ANALOG TRIGGER IN
7	DOUT1	57	A/D PACER GATE
8	DOUT0	58	A/D PACER OUT
9	DIN3	59	SSH OUT / D/A PACER OUT
10	DIN2	60	EXTERNAL D/A TRIGGER/PACER GATE
11	DIN1	61	D/A EXTERNAL PACER
12	DIN0	62	PC +5 V
13	GND	63	D/A OUT 1
14	-12 V	64	D/A GND 1
15	GND	65	D/A OUT 0
16	+12 V	66	D/A GND 0
17	CH63 IN	67	CH31 IN
18	CH62 IN	68	CH30 IN
19	CH61 IN	69	CH29 IN
20	CH60 IN	70	CH28 IN
21	CH59 IN	71	CH27 IN
22	CH58 IN	72	CH26 IN
23	CH57 IN	73	CH25 IN
24	CH56 IN	74	CH24 IN
25	CH55 IN	75	CH23 IN
26	CH54 IN	76	CH22 IN
27	CH53 IN	77	CH21 IN
28	CH52 IN	78	CH20 IN
29	CH51 IN	79	CH19 IN
30	CH50 IN	80	CH18 IN
31	CH49 IN	81	CH17 IN
32	CH48 IN	82	CH16 IN
33	LLGND	83	LLGND
34	CH47 IN	84	CH15 IN
35	CH46 IN	85	CH14 IN
36	CH45 IN	86	CH13 IN
37	CH44 IN	87	CH12 IN
38	CH43 IN	88	CH11 IN
39	CH42 IN	89	CH10 IN
40	CH41 IN	90	CH9 IN
41	CH40 IN	91	CH8 IN
42	CH39 IN	92	CH7 IN
43	CH38 IN	93	CH6 IN
44	CH37 IN	94	CH5 IN
45	CH36 IN	95	CH4 IN
46	CH35 IN	96	CH3 IN
47	CH34 IN	97	CH2 IN
48	CH33 IN	98	CH1 IN
49	CH32 IN	99	CH0 IN
50	GND	100	LLGND

Digital input/output connector and pin out

Table 23. Digital I/O connector specifications

Connector type	40-pin header
Connector compatibility	Translates to standard CIO-DIO24 type using BP40-37
Compatible cable	C40FF-2
Compatible accessory products	CIO-MINI40

Table 24. Digital I/O connector pin out

Pin	Signal name	Pin	Signal name
1	NC	2	PC +5 V
3	NC	4	DIG GND
5	FIRSTPORTB Bit 7	6	FIRSTPORTC Bit 7
7	FIRSTPORTB Bit 6	8	FIRSTPORTC Bit 6
9	FIRSTPORTB Bit 5	10	FIRSTPORTC Bit 5
11	FIRSTPORTB Bit 4	12	FIRSTPORTC Bit 4
13	FIRSTPORTB Bit 3	14	FIRSTPORTC Bit 3
15	FIRSTPORTB Bit 2	16	FIRSTPORTC Bit 2
17	FIRSTPORTB Bit 1	18	FIRSTPORTC Bit 1
19	FIRSTPORTB Bit 0	20	FIRSTPORTC Bit 0
21	DIG GND	22	FIRSTPORTA Bit 7
23	NC	24	FIRSTPORTA Bit 6
25	DIG GND	26	FIRSTPORTA Bit 5
27	NC	28	FIRSTPORTA Bit 4
29	DIG GND	30	FIRSTPORTA Bit 3
31	NC	32	FIRSTPORTA Bit 2
33	DIG GND	34	FIRSTPORTA Bit 1
35	PC +5 V	36	FIRSTPORTA Bit 0
37	DIG GND	38	NC
39	NC	40	NC

CE Declaration of Conformity

Manufacturer:	Measurement Computing Corporation
Address:	10 Commerce Way Suite 1008 Norton, MA 02766 USA
Category:	Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS64/M2/16

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN55022 (1995), EN55024 (1998)

Emissions: Group 1, Class B

- EN55022 (1995): Radiated and Conducted emissions.

Immunity: EN55024

- EN61000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- EN61000-4-3 (1997): Radiated Electromagnetic Field immunity Criteria A.
- EN61000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- EN61000-4-5 (1995): Surge immunity Criteria A.
- EN61000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- EN61000-4-8 (1994): Power Frequency Magnetic Field immunity Criteria A.
- EN61000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in September, 2001. Test records are outlined in Chomerics Test Report #EMI3053.01.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

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