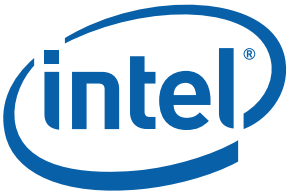
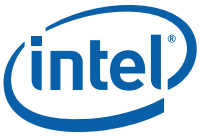


# Intel® Q965 Express Chipset

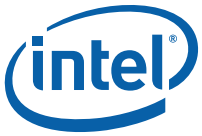
## Development Kit User Manual

*October 2007*

Order Number: 315664-002US



# Contents





## Figures



## Tables

# Revision History

| Date | Revision | Description |
|---|---|---|
| October 2007 | 002 | Change SDVOB to SDVOC in pins 58, 59, 62 and 63 in Table 9, "Intel® SDVO to PCI Express* connector mapping for MEC cards" on page 18. |
| October 2006 | 001 | Initial public release. |

# 1.0 About This Manual

This user's manual describes the use of the Intel® Q965® Express Chipset Development Kit. This manual has been written for OEMs, system evaluators, and embedded system developers. All jumpers, headers, LED functions, and their locations on the board, along with subsystem features and POST codes, are defined in this document.

For the latest information about the Intel® Q965® Express Chipset Development Kit reference platform, visit:

http://developer.intel.com/design/intarch/devkit/index.htm

For design documents related to this platform, such as schematics and layout, please contact your Intel Representative.

## 1.1 Content Overview

Chapter 1: "Development Kit Users Manual Content overview"

This chapter contains a description of conventions used in this manual. The last few sections explain how to obtain literature and contact customer support.

Chapter 2: "Development Kit Hardware Features"

This chapter provides information on the development kit features and the board capability. This includes the information on board component features, jumper settings, pin-out information for connectors and overall development kit board capability.

Chapter 3: "Development Kit Software and BIOS Features"

This chapter provides an overview of development kit software and BIOS features.

Chapter 4: "Development Kit Board Setup"

This chapter provides instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

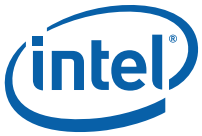
Chapter 5: "Error Messages and Beep Codes"

This chapter describes the various progress codes that are reported by the BIOS and the corresponding LED Codes.

## 1.2 Text Conventions

The following notations may be used throughout this manual.

| | |
|---|---|
| **#** | The pound symbol (#) appended to a signal name indicates that the signal is active low. |



**Variables** Variables are shown in italics. Variables must be replaced with correct values.

**Instructions** Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper-case or lower-case.

**Numbers** Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number.) In some cases, the letter *B* is added for clarity.

**Units of Measure** The following abbreviations are used to represent units of measure:

| | |
|---|---|
| A | amps, amperes |
| Gbyte | gigabytes |
| Kbyte | kilobytes |
| K | kilo-ohms |
| mA | milliamps, milliamperes |
| Mbyte | megabytes |
| MHz | megahertz |
| ms | milliseconds |
| mW | milliwatts |
| ns | nanoseconds |
| pF | picofarads |
| W | watts |
| V | volts |
| µA | microamps, microamperes |
| µF | microfarads |
| µs | microseconds |
| µW | microwatts |

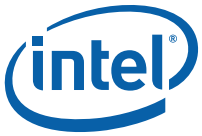
**Signal Names** Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

## 1.3 Glossary of Terms and Acronyms

This section defines conventions and terminology used throughout this document.

## Table 1. Glossary of Terms and Acronyms (Sheet 1 of 3)

| Term | Description |
|---|---|
| ADD2 Card | Advanced Digital Display Card – second Generation. This card provides digital display options for an Intel Graphics Controller. It plugs into an x16 PCI Express* connector but uses the multiplexed SDVO interface. This Advanced Digital Display Card will not work with an Intel Graphics Controller that supports DVO and ADD cards. |
| ACPI | Advanced Configuration and Power Interface |
| ASF | Alert Standard Format |
| BLT | Block Level Transfer |
| Core | The internal base logic in the (G)MCH |
| CRT | Cathode Ray Tube |
| DBI | Dynamic Bus Inversion |
| DDR2 | A second generation Double Data Rate SDRAM memory technology. |
| DMI | Direct Media Interface |
| DVI | Digital Video Interface. Specification that defines the connector and interface for digital displays. |
| FSB | Front Side Bus. FSB is synonymous with Host or processor bus. |
| Full Reset | Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted. |
| GMCH | Graphics Memory Controller Hub component that contains the processor interface, DRAM controller, x16 PCI Express* Graphics port (typically, the external graphics interface), and integrated graphics device (IGD). It communicates with the I/O controller hub (ICH8DO*) and other I/O controller hubs over the DMI interconnect. In this document GMCH refers to the 82Q965 GMCH component. |
| GMA 3000 | Intel® Graphic Media Accelerator 3000 |
| Host | This term is used synonymously with processor. |
| IDER | IDE Redirect |
| INTx | An interrupt request signal where “x” stands for interrupts A, B, C, and D |
| Intel® 64 Architecture | Intel® 64 Architecture[1] (Formerly known as Intel® EM64T) enables the processor to access larger amounts of virtual and physical memory. |
| Intel® Advanced Digital Media Boost | 128-bit SSE instructions are now issued one per clock cycle effectively doubling their speed of execution over previous generation processors. This benefits a broad range of applications including video, audio, encryption, engineering and scientific with improved performance. |
| Intel® AMT | Intel® Active Management Technology |
| Intel® Advanced Smart Cache | The shared L2 cache is allocated to each processor core based on workload up to the full amount of total cache. This is more efficient than today’s dual-core processor. Sharing the cache significantly reduces the time needed to retrieve frequently used data improving performance. |
| Intel® DVO | Digital Video Out port. Term used for the first generation of Intel Graphics Controller’s digital display channels. Digital display data is provided in a parallel format. This interface is not electrically compatible with the 2nd generation digital display channel discussed in this document – SDVO. |
| Intel® ICH8DO | Eighth generation I/O Controller Hub component that contains additional functionality compared to previous ICHs. The I/O Controller Hub component contains the primary PCI interface, LPC interface, USB2, SATA, and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI. |
| Intel® QST | Intel® Quiet System Technology |
| Intel® Smart Memory Access | Optimizes functions for reducing wait time, moving data and accelerating out-of-order execution, keep the pipeline full improving instruction throughput and performance. |



## Table 1. Glossary of Terms and Acronyms (Sheet 2 of 3)

| Term | Description |
|---|---|
| Intel® VT | Intel® Virtualization Technology. Intel® VT allows one hardware platform to function as multiple "virtual" platforms. For businesses, Intel VT Technology[1] (Intel® VT) offers improved manageability, limiting downtime and maintaining worker productivity by isolating computing activities into separate partitions. |
| Intel® Wide Dynamic Execution | Improves execution speed and efficiency, delivering more instructions per clock cycle. Each core can complete up to four full instructions simultaneously. |
| IGD | Internal Graphics Device. |
| LCD | Liquid Crystal Display. |
| LVDS | Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels. |
| MEBx | Management Engine BIOS Extensions |
| MEC | Media Expansion Card – Provides digital display options for an Intel Graphics Controller that supports MEC cards. Plugs into an x16 PCI Express connector but utilizes the multiplexed SDVO interface. Adds Video In capabilities to platform. Will not work with an Intel Graphics Controller that supports DVO and ADD cards. Will function as an ADD2 card in an ADD2 supported system, but Video In capabilities will not work. |
| PCI Express* Graphics | PCI Express* Graphics is a high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express* implementation intended for connecting the (G)MCH to an external Graphics Controller is a x16 link and replaces AGP. |
| PECI | Platform Environmental Control Interface |
| Primary PCI | The Primary PCI is the physical PCI bus that is driven directly by the ICH8DO component. Communication between Primary PCI and the (G)MCH occurs over DMI. Note that the Primary PCI bus is not PCI Bus 0 from a configuration standpoint. |
| Processor | Intel® Core™2 Duo processor E6400 |
| QST | Quiet System Technology |
| SATA | Serial ATA Specification |
| SCI | System Control Interrupt. SCI is used in ACPI protocol. |
| SDVO | Serial Digital Video Out (SDVO). SDVO is a digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS and TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the 82Q965 GMCH, it will be multiplexed on a portion of the x16 graphics PCI Express* interface. |
| SDVO Device | Third party codec that uses SDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-out, etc. |
| SERR | System Error. An indication that an unrecoverable error has occurred on an I/O bus. |
| SMI | System Management Interrupt. SMI is used to indicate any of several system conditions (such as, thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity). |
| SOL | Serial Over LAN |
| SPI | Serial Peripheral Interface |
| SST | Simple Serial Transport |

**Table 1. Glossary of Terms and Acronyms (Sheet 3 of 3)**

| Term | Description |
|---|---|
| Rank | A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM. |
| UMA | Unified Memory Architecture. Describes an IGD using system memory for its frame buffers. |

***Note:***
1. Intel® Virtualization Technology (Intel® VT), and Intel® 64 Architecture require a computer system with a processor, chipset, BIOS, enabling software and/or operating system, device drivers and applications designed for these features. Performance will vary depending on your configuration. Contact your vendor for more information.

## 1.4 Support Options

### 1.4.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

### 1.4.2 Additional Technical Support

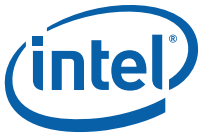
If additional technical support is required, please contact your field sales representative or local distributor.

## 1.5 Product Literature

Product literature can be ordered from the following Intel literature centers:

**Table 2. Intel Literature Centers**

| Location | Telephone Number |
|---|---|
| U.S. and Canada | 1-800-548-4725 |
| U.S. (from overseas) | 708-296-9333 |
| Europe (U.K.) | 44(0)1793-431155 |
| Germany | 44(0)1793-421333 |
| France | 44(0)1793-421777 |
| Japan (fax only) | 81(0)120-47-88-32 |



# 2.0 Development Kit Hardware Features

## 2.1 Overview

This chapter provides information on the development kit features and the board capability. For detailed platform features please refer to the Platform Design Guide for or datasheet for the chipset and the *Intel® Core™2 Duo processor Thermal and Mechanical Design Guidelines*.

## 2.2 Intel® Q965® Express Chipset Development Kit Features Summary

This section summarizes the development kit features.

**Table 3. Development Kit Features Summary (Sheet 1 of 2)**

| | |
|---|---|
| **Form Factor** | 4 Layer µBTX (10.5 inches x 10.4 inches) |
| **Processor** | Intel® Core™ 2 Duo processor E6400<br>Supports 1066 MHz front side bus<br>2M Shared L2 Cache<br>Supports Intel® 64 Architecture<br>Supports Intel® Wide Dynamic Execution, Intel® Smart Memory Access, Intel Advanced Smart Cache, Intel® Advanced Digital Media Boost, Intel® Virtualization Technology |
| **Memory** | DDR2 dual-channel system memory interface<br>Four 240-pin DDR2 SDRAM DIMM sockets (two per channel) supporting dual channel interleaved mode<br>Support for 533MHz, 667MHz, 800MHz unbuffered, non-ECC DDR2 SDRAM modules<br>Supports 128 MB to 8 GB of system memory<br>256 Mbit, 512 Mbit, or 1 Gbit Technology |
| **Chipset** | Intel® Q965 Express Chipset, consisting of:<br>Intel® 82Q965 Graphics Memory Controller Hub ((G)MCH)<br>Intel® 82801GB I/O Controller Hub (ICH8DO) |
| **Video** | Option of either using integrated graphics system or external PCI Express* graphics:<br>Intel® GMA3000 integrated graphics subsystem<br>Supports ADD2 and Intel® Media Expansion Card (MEC, also known as ADD2+) for additional digital display such as DVI, LVDS, etc. depending on the media expansion card features.<br>Supports external PCI Express* (x16) graphics card |
| **Audio** | Intel® High Definition Audio subsystem:<br>8-channel (7.1) audio subsystem and two S/PDIF digital audio outputs using the ADI audio codec. |
| **Legacy I/O Control** | Port Angeles 3.0 Super I/O controller for diskette drive, serial, parallel, and PS/2* ports. |

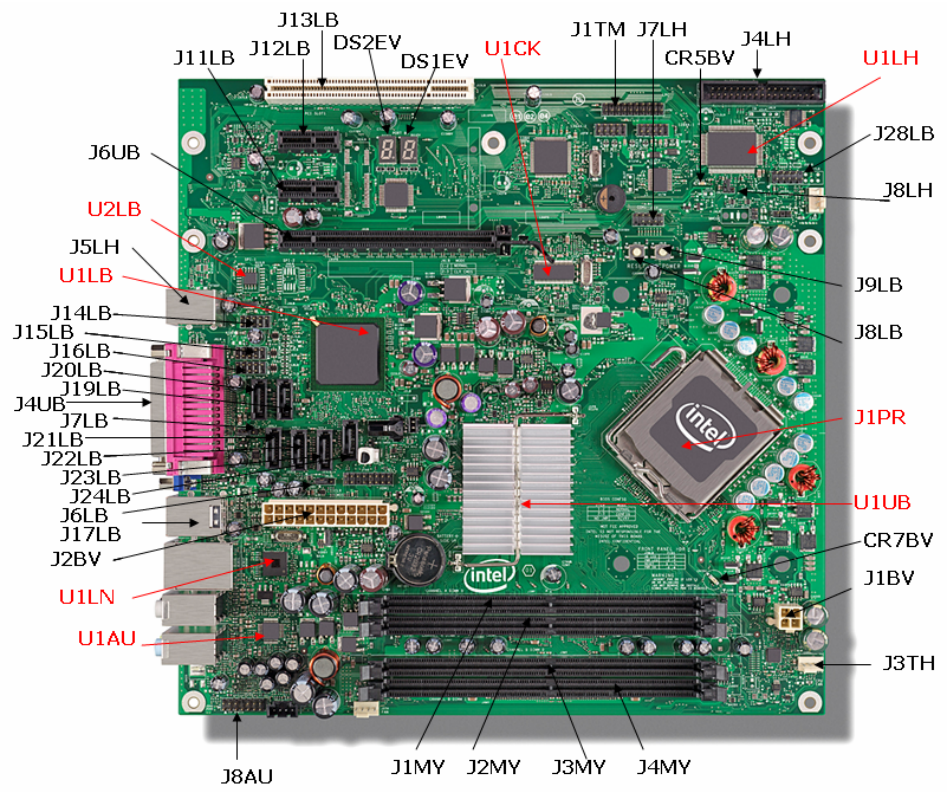
**Table 3. Development Kit Features Summary (Sheet 2 of 2)**

| | |
|---|---|
| **Form Factor** | 4 Layer µBTX (10.5 inches x 10.4 inches) |
| **Peripheral Interfaces** | Six SATA 1.5/3.0 Gb/s ports.<br>Ten Universal Serial Bus (USB) 2.0 ports – Three front panel headers for support of six front panel ports and four back panel ports<br>Three 1394a PCI controller – 2 front headers for support of two ports and one back panel port (Disabled in this Development Kit)<br>PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors<br>One VGA connector provides access to integrated graphics.<br>Six analog audio connectors (Line-in, Line-out, MIC-in, Surround L/R, Surround L/R Rear, Center) and two digital audio connectors driven by Intel High Definition Audio.<br>One parallel port.<br>One diskette drive interface |
| **LAN Support** | Gigabit (10/100/1000 Mbits/s) LAN subsystem using the Intel® 82566DM Gigabit Ethernet Controller |
| **BIOS** | Support for Advanced configuration and power interface (ACPI), plug and play, and SMBIOS.<br>AMI system BIOS. |
| **Expansion Capabilities** | One PCI bus connectors<br>One PCI Express* x16 bus add-in card connector<br>Two PCI Express* x1 bus add-in card connectors |
| **Additional Features** | Trusted Platform Module (TPM) 1.2 support<br>Manageability Engine (ME) support. ME Enabled LED (red-blink)<br>Intel® Active Management Technology (Intel® AMT) with System Defense support<br>Intel® Quiet System Technology (Intel® QST) support<br>Intel® Matrix Storage technology with RAID 0,1,5, 10 support<br>Piezo speaker for BIOS POST codes<br>PORT 80 Display<br>Thermal Diode header<br>BIOS configuration jumper<br>Clear CMOS header<br>Force On header<br>XDP-SSA connector<br>Internal I/O headers<br>• 2x5 Front Panel I/O header<br>• 2x7 Front Panel audio header<br>• 1x2 Chassis intrusion header<br>• 3 four-wire fan headers<br>• 2x5 Serial port header<br>• 2x8 High Definition audio header<br>• 20-pin LPC header |

## 2.3 Board Layout

Figure 1 shows the location of the major components, headers and jumpers.

**Figure 1. Dev Kit Board Main Components, Headers and Jumper Locations**




## 2.3.1 Core Components

**Table 4. Core Components**

| Reference Designator | Component Description |
|---|---|
| J1PR | LGA775 processor socket |
| U1UB | Intel® Q965 (G)MCH |
| U1LB | Intel® ICH8DO |
| U1LN | Intel® 82566DM Gb LAN chip |
| U1CK | Clock Generator CK505 |
| U1LH | Super I/O (Port Angles) |
| U1AU | Audio Codec |
| U2LB | Primary SPI Flash (stuffed with 16 Mb) |

*Note:* There will be 2 SPI footprints on the board. Firmware Hub will not be supported. The primary SPI flash footprint is at XU3LB and stuffed with a 16 Mb (2 MB) SPI flash (U2LB). The secondary SPI flash footprint is at XU5LB and unstuffed.

### 2.3.2 Jumper Settings and Descriptions

**Table 5. Jumper Settings**

| Jumper | Default | Description | Notes |
|---|---|---|---|
| J7LB | 1-2 | BIOS Config/Recovery | 1-2 = Normal<br>2-3 = Config Mode<br>Off = Recovery |
| J6LB | 1-2 | Clear CMOS | 1-2 = Normal<br>2-3 = Clear CMOS |
| J8LH | 1-2 | Power-On Forcing | 1-2 = Normal<br>2-3 = Force On (Sets CPU presence bit; may not always force board power on) |

### 2.3.3 LED Descriptions

Power LEDs are on the board to indicate when standby and core power is being applied to the planes. When on, they indicate that no devices should be inserted or removed. Please refer to Figure 2 for the LED locations.

***Caution:*** Inserting or removing devices when the Standby Power LEDs are on could result in device or board damage.

**Table 6. LED Description**

| LED | Description | Notes |
|---|---|---|
| CR5BV | 5-Volt Standby Power Display LED | Green |
| DS1EV | Port 80 Display – Right | |
| DS2EV | Port 80 Display - Left | |
| CR7BV | ME Enabled LED | Red Blink |

### 2.3.4 Header and Connector Descriptions

**Table 7. Header and Connector Descriptions (Sheet 1 of 2)**

| Header | Description | Notes |
|---|---|---|
| J5LB | Intruder Header | |
| J7LH | Serial Port Header | |
| J3AU | ATAPI CD Header | |
| J7AU | High Definition Media Interface Header | |
| J8AU | Front Panel Audio Header | |
| J28LB | Front Panel Header | |
| J3TH | CPU Fan | |
| J4TH | Chassis Fan | |
| J5TH | Chassis Fan | |
| J2BV | 2x12 Standard Power Connector | |
| J1BV | 2x2 12V Power Connector | |
| J29LB | Power LED header | |
| J24LB | SATA connector | SATA HDD port 0 |

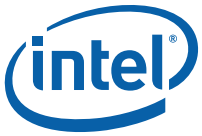


**Table 7. Header and Connector Descriptions (Sheet 2 of 2)**

| Header | Description | Notes |
|---|---|---|
| J22LB | SATA connector | SATA HDD port 1 |
| J23LB | SATA connector | SATA HDD port 2 |
| J21LB | SATA connector | SATA HDD port 3 |
| J19LB | SATA connector | SATA HDD port 4 |
| J20LB | SATA connector | SATA HDD port 5 |
| J1MY | DIMM connector | Channel A DIMM 0 |
| J2MY | DIMM connector | Channel A DIMM 1 |
| J3MY | DIMM connector | Channel B DIMM 0 |
| J4MY | DIMM connector | Channel B DIMM 1 |
| J4LH | Floppy connector | |
| J6UB | X16 PCI Express* Graphics slot | For Graphics cards |
| J11LB | X1 PCI Express slot | PCI Express* port 4 |
| J12LB | X1 PCI Express slot | PCI Express* port 5 |
| J13LB | PCI slot | |
| J14LB | USB Front Panel Header | |
| J15LB | USB Front Panel Header | |
| J16LB | USB Front Panel Header | |
| J1TM | LPC BUS Header (TPM) | In order to Plug a TPM module into this header, you must first disable onboard TPM |
| J1FW | 1394a Front Panel Header | Disabled |
| J2FW | 1394a Front Panel Header | Disabled |
| J9LB | Power Button | |
| J8LB | Reset Button | |
| J2BC | XDP_SSA | This is reserved by Intel for debugging purpose. Located at the back of the board |

### 2.3.5 Back Panel Connectors

Figure 2 shows the location of the back panel connectors for boards equipped with the 8-channel (7.1) audio subsystem. The back panel connectors are color-coded. The figure legend lists the colors used (when applicable).

**Figure 2. Rear Panel I/O Connectors**

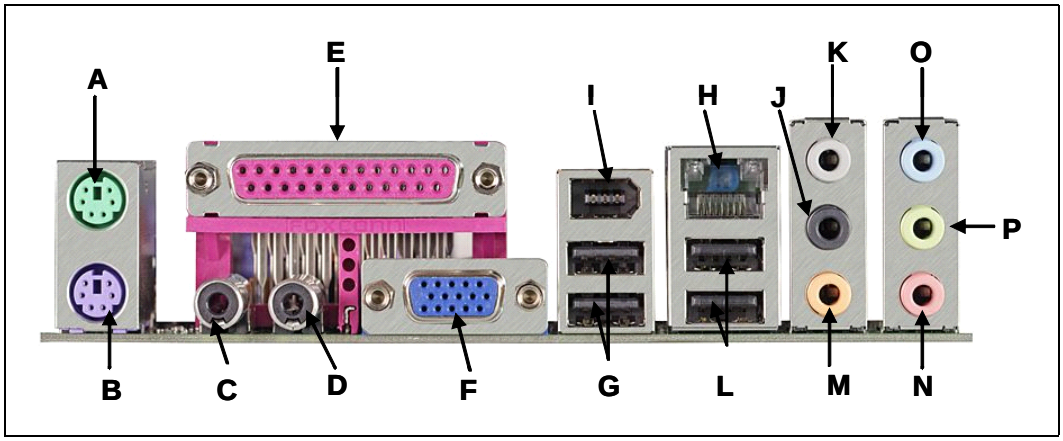



**Table 8. Back panel connectors**

| Callouts from Figure 2.2 | Designator | Description |
|---|---|---|
| A | J5LH | PS/2 mouse port [Green] |
| B | J5LH | PS/2 keyboard port [Purple] |
| C | J1AU | S/PDIF Digital audio output |
| D | J2AU | S/PDIF Digital audio input |
| E | J6LH | Parallel port [Burgundy] |
| F | J4UB | VGA Port |
| G | J17LB | Back Panel USB Ports 1 and 2<br>Overlapping with 1394(J3FW) |
| H | JA1LN | RJ45 LAN connector |
| I | J3FW | 1394 Port present but disabled |
| J | J5AU | Rear Speaker Out |
| K | J5AU | Side Speaker Out |
| L | J18LB | Back Panel USB Ports 3 and 4. Overlapping with LAN MagJack (JA1LN) |
| M | J5AU | Center channel and Subwoofer audio out |
| N | J4AU | MIC In |
| O | J4AU | Audio Line In |
| P | J4AU | Audio Line Out (Front Speaker Out) |

## 2.3.6 PCI Express* x16 / MEC Slot

The PCI Express* x16 slot is following the industry PCI Express* x16 connector standard. Table 2.7 shows the signals for PCI Express* x16 or MEC (SDVO).

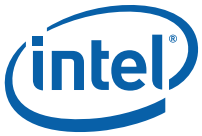


**Table 9. Intel® SDVO to PCI Express* connector mapping for MEC cards (Sheet 1 of 3)**

| Pin Number | Side B | | Side A | |
|---|---|---|---|---|
| | PCI Express* Function | SDVO / MEC Function | PCI Express* Function | SDVO / MEC Function |
| 1 | 12 V | 12 V | PRSNT1# | NC |
| 2 | 12 V | 12 V | 12V | 12V |
| 3 | RSVD | RSVD | 12V | 12V |
| 4 | GND | GND | GND | GND |
| 5 | SMCLK | NC | JTAG2 (TCK) | NC |
| 6 | SMDAT | NC | JTAG3 (TDI) | JTAG3 (TDI) |
| 7 | GND | GND | JTAG4 (TDO) | JTAG4 (TDO) |
| 8 | 3.3 V | 3.3 V | JTAG5 (TMS) | NC |
| 9 | JTAG1 (TRST#) | NC | 3.3 V | 3.3 V |
| 10 | 3.3 Vaux | 3.3 Vaux | 3.3 V | 3.3 V |
| 11 | WAKE# | WAKE# | PERST# | PERST# |
| Key | | | | |
| 12 | RSVD | RSVD | GND | GND |
| 13 | GND | GND | REFCLK+ | REFCLK+ |
| 14 | PET0+(or PETp0) | PET0+(or PETp0) | REFCLK- | REFCLK- |
| 15 | PET0-(or PETn0) | PET0-(or PETn0) | GND | GND |
| 16 | GND | GND | PER0+(or PERp0) | PER0+(or PERp0) |
| 17 | PRSNT2# | SDVO_CtrlClk | PER0-(or PERn0) | PER0-(or PERn0) |
| 18 | GND | GND | GND | GND |
| End of x1 Connector | | | | |
| 19 | PET1+(or PETp1) | NC | RSVD | RSVD |
| 20 | PET1-(or PETn1) | NC | GND | GND |
| 21 | GND | GND | PER1+(or PERp1) | NC |
| 22 | GND | GND | PER1-(or PERn1) | NC |
| 23 | PET2+(or PETp2) | NC | GND | GND |
| 24 | PET2-(or PETn2) | NC | GND | GND |
| 25 | GND | GND | PER2+(or PERp2) | NC |
| 26 | GND | GND | PER2-(or PERn2) | NC |
| 27 | PET3+(or PETp3) | NC | GND | GND |
| 28 | PET3-(or PETn3) | NC | GND | GND |
| 29 | GND | GND | PER3+(or PERp3) | NC |
| 30 | RSVD | RSVD | PER3-(or PERn3) | NC |
| 31 | PRSNT2# | SDVO_CtrlData | GND | GND |
| 32 | GND | GND | RSVD | RSVD |
| End of x4 Connector | | | | |
| 33 | PET4+(or PETp4) | NC | RSVD | RSVD |

**Table 9. Intel® SDVO to PCI Express* connector mapping for MEC cards (Sheet 2 of 3)**

| Pin Number | Side B | | Side A | |
|---|---|---|---|---|
| 34 | PET4-(or PETn4) | NC | GND | GND |
| 35 | GND | GND | PER4+(or PERp4) | NC |
| 36 | GND | GND | PER4-(or PERn4) | NC |
| 37 | PET5+(or PETp5) | NC | GND | GND |
| 38 | PET5-(or PETn5) | NC | GND | GND |
| 39 | GND | GND | PER5+(or PERp5) | NC |
| 40 | GND | GND | PER5-(or PERn5) | NC |
| 41 | PET6+(or PETp6) | NC | GND | GND |
| 42 | PET6-(or PETn6) | NC | GND | GND |
| 43 | GND | GND | PER6+(or PERp6) | NC |
| 44 | GND | GND | PER6-(or PERn6) | NC |
| 45 | PET7+(or PETp7) | NC | GND | GND |
| 46 | PET7-(or PETn7) | NC | GND | GND |
| 47 | GND | GND | PER7+(or PERp7) | NC |
| 48 | PRSNT2# | ADD2+_Enable | PER7-(or PERn7) | NC |
| 49 | GND | GND | GND | GND |
| **End of x8 Connector** | | | | |
| 50 | PET8+(or PETp8) | SDVOC_Clk+ | RSVD | RSVD |
| 51 | PET8-(or PETn8) | SDVOC_Clk- | GND | GND |
| 52 | GND | GND | PER8+(or PERp8) | NC |
| 53 | GND | GND | PER8-(or PERn8) | NC |
| 54 | PET9+(or PETp9) | SDVOC_Blue+ | GND | GND |
| 55 | PET9-(or PETn9) | SDVOC_Blue- | GND | GND |
| 56 | GND | GND | PER9+(or PERp9) | NC |
| 57 | GND | GND | PER9-(or PERn9) | NC |
| 58 | PET10+(or PETp10) | SDVOC_Green+ | GND | GND |
| 59 | PET10-(or PETn10) | SDVOC_Green- | GND | GND |
| 60 | GND | GND | PER10+(or PERp10) | NC |
| 61 | GND | GND | PER10-(or PERn10) | NC |
| 62 | PET11+(or PETp11) | SDVOC_Red+ | GND | GND |
| 63 | PET11-(or PETn11) | SDVOC_Red- | GND | GND |
| 64 | GND | GND | PER11+(or PERp11) | NC |
| 65 | GND | GND | PER11-(or PERn11) | NC |
| 66 | PET12+(or PETp12) | SDVOB_Clk+ | GND | GND |
| 67 | PET12-(or PETn12) | SDVOB_Clk- | GND | GND |
| 68 | GND | GND | PER12+(or PERp12) | NC |

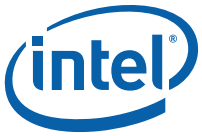


**Table 9. Intel® SDVO to PCI Express* connector mapping for MEC cards (Sheet 3 of 3)**

| Pin Number | Side B | | Side A | |
|---|---|---|---|---|
| 69 | GND | GND | PER12-(or PERn12) | NC |
| 70 | PET13+(or PETp13) | SDVOB_Blue+ | GND | GND |
| 71 | PET13-(or PETn13) | SDVOB_Blue- | GND | GND |
| 72 | GND | GND | PER13+(or PERp13) | NC |
| 73 | GND | GND | PER13-(or PERn13) | NC |
| 74 | PET14+(or PETp14) | SDVOB_Green+ | GND | GND |
| 75 | PET14-(or PETn14) | SDVOB_Green- | GND | GND |
| 76 | GND | GND | PER14+(or PERp14) | NC |
| 77 | GND | GND | PER14-(or PERn14) | NC |
| 78 | PET15+(or PETp15) | SDVOB_Red+ | GND | GND |
| 79 | PET15-(or PETn15) | SDVOB_Red- | GND | GND |
| 80 | GND | GND | PER15+(or PERp15) | NC |
| 81 | PRSNT2# | NC | PER15-(or PERn15) | NC |
| 82 | RSVD | RSVD | GND | GND |
| ***Note:*** End of x16 Connector | | | | |

## 2.3.7 PCI Express* x1

The PCI Express* x1 connectors allow the use of any industry standard PCI Express* device. The pin configuration of the connectors is given below:

**Table 10. PCI Express* (x1) Pinout**

| Pin Number | Side B | Side A |
|---|---|---|
| 1 | 12 V | PRSNT1# |
| 2 | 12 V | 12V |
| 3 | 12 V | 12V |
| 4 | GND | GND |
| 5 | SMCLK | JTAG2 |
| 6 | SMDAT | JTAG3 |
| 7 | GND | JTAG4 |
| 8 | 3.3 V | JTAG5 |
| 9 | JTAG1 | 3.3 V |
| 10 | 3.3 Vaux | 3.3 V |
| 11 | WAKE# | PWRGD |
| Key | | |
| 12 | RSVD | GND |
| 13 | GND | REFCLK+ |

**Table 10. PCI Express* (x1) Pinout**

| Pin Number | Side B | Side A |
|---|---|---|
| 14 | HSOP0 | REFCLK- |
| 15 | HSON0 | GND |
| 16 | GND | HSIP1 |
| 17 | PRSNT2# | HSIN1 |
| 18 | GND | GND |
| ***Note:*** End of x1 Connector | | |

## 2.3.8 Front Panel Header (Power up & Reset)

This development kit board use front panel header (J28LB) for powering-up and board reset. Refer to Table 11 for the front panel header lists.

The front panel header is a 2x5 header, designated as J28LB. The following table outlines the pin out and functionality of this header:

**Table 11. Front Panel Jumper Setting**

| Pin | Signal Name | Description |
|---|---|---|
| 1 | HDD LED Anode | HDD LED Anode |
| 2 | Green Power LED | |
| 3 | HDD LED Cathode | HDD LED Cathode |
| 4 | Yellow Power LED | |
| 5 | Ground | |
| 6 | Switch On | |
| 7 | Reset | |
| 8 | Ground | |
| 9 | Power | VCC |
| 10 | KEY | No pin |

## 2.3.9 Front Panel USB Header

The front panel USB header is a 2x5 header, designated as J14LB, J15LB or J16LB. The following table outlines the pin out and functionality of this header:

**Table 12. Front Panel USB Header (Sheet 1 of 2)**

| Pin | Signal names | Description |
|---|---|---|
| 1 | VREG_FP_USBPWR | Front panel USB power (Ports 0,1) [+5 V or +5 V Dual] Note |
| 2 | VREG_FP_USBPWR | Front panel USB power (Ports 0,1) [+5 V or +5 V Dual] |
| 3 | USB_FP_P0 | Front panel USB Port 0 negative signal |
| 4 | USB_FP_P1 | Front panel USB Port 1 negative signal |
| 5 | USB_FP_P0+ | Front panel USB Port 0 positive signal |
| 6 | USB_FP_P1+ | Front panel USB Port 1 positive signal |
| 7 | Ground | |

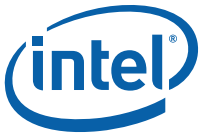


**Table 12. Front Panel USB Header (Sheet 2 of 2)**

| Pin | Signal names | Description |
|---|---|---|
| 8 | Ground | |
| 9 | Key | |
| 10 | USB_FP_OC0 | Front panel USB over current signal (Ports 0,1) |

*Note:* +5 V Dual switches between +5 V and +5 V Standby depending on the current board state.

## 2.3.10 Front Audio Header

The front panel Audio header is a 2x7 header, designated as J8AU. The following table outlines the pin out and functionality of this header:

**Table 13. Front Audio Header**

| Pin | Signal Name | Description |
|---|---|---|
| 1 | AUD_PORT_1_R | Port 1 Audio Right |
| 2 | GND | Ground |
| 3 | AUD_PORT_1_L | Port 1 Audio Left |
| 4 | AUD_FP_PWR | Front Panel Audio Power |
| 5 | AUD_PORT_2_R | Port 2 Audio Right |
| 6 | AUD_FP_RET_R | Front Panel Audio Return Right |
| 7 | AUD_FP_JS | Front Panel Jack Sense |
| 8 | No Connect | Key Pin |
| 9 | AUD_PORT_2_L | Port 2 Audio Left |
| 10 | AUD_FP_RET_L | Front Panel Audio Return Left |
| 11 | AUD_VOL_UP | Audio Volume Up |
| 12 | AUD_VOL_MUTE | Audio Mute |
| 13 | AUD_VOL_DWN | Audio Volume Down |
| 14 | GND | Ground |

## 2.3.11 High Definition Audio Header

The High Definition Audio header is a 2x8 header, designated as J7AU. The following table outlines the pin out and functionality of this header:

**Table 14. High Definition Audio Header (Sheet 1 of 2)**

| Pin | Signal Name | Description |
|---|---|---|
| 1 | AUD_LINK_BCLK_HDR | |
| 2 | GND | Ground |
| 3 | AUD_LINK_RST_HDR | |
| 4 | VCC3 | Power |
| 5 | AUD_LINK_SYNC_HDR | |
| 6 | GND | Ground |
| 7 | AUD_LINK_SDO_HDR | |

**Table 14. High Definition Audio Header (Sheet 2 of 2)**

| Pin | Signal Name | Description |
|---|---|---|
| 8 | VCC3 | Power |
| 9 | AUD_LINK_SDI0 | |
| 10 | +12V | Power |
| 11 | AUD_LINK_SDI1 | |
| 12 | KEY | No Connect |
| 13 | TP_AUD_LINK_SDO_1_HDR | |
| 14 | V_3P3_STBY\G | 3.3V Standby |
| 15 | AUD_LINK_SDI2_R | |
| 16 | GND | Ground |

## 2.3.12 BTX Power Connectors

**Table 15. 2x12 BTX Power Connector**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +3.3V | 13 | GND |
| 2 | +3.3V | 14 | PS_ON# |
| 3 | GND | 15 | GND |
| 4 | +5V | 16 | GND |
| 5 | GND | 17 | GND |
| 6 | +5V | 18 | -5V |
| 7 | GND | 19 | +5V |
| 8 | PWDGD | 20 | +5V |
| 9 | 5 VSB | 21 | -5V |
| 10 | +12V | 22 | +5V |
| 11 | +3.3V | 23 | +5V |
| 12 | -12V | 24 | GND |

**Table 16. 2x2 Auxiliary 12V Power Connector**

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | +12V |
| 4 | +12V |

### 2.3.13 SATA Pinout

**Table 17. SATA Pinout**

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | TXP |
| 3 | TXN |
| 4 | GND |
| 5 | RXN |
| 6 | RXP |
| 7 | GND |

### 2.3.14 Fan Connectors

**Table 18. Fan connectors**

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | RPM |
| 4 | Control |

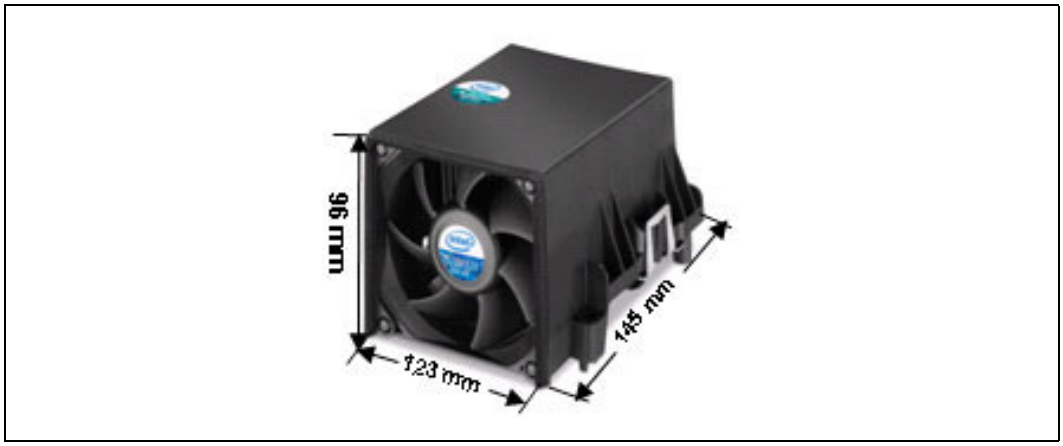
## 2.4 Thermal Considerations

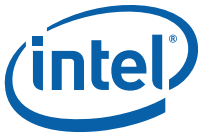
The development kit is shipped with a BTX TYPE I heatsink/fan thermal solution for installation on the processor. BTX systems are designed so that all the high power components are in-line and can be cooled using a single, continuous airflow stream. The BTX Thermal Module Assembly (TMA) provides airflow to the central processing unit (microprocessor) and its voltage regulation (VR), which is located at the front of the system, and then to the memory controller (G)MCH, Input/Output controller (ICH), and the add-in card (AIC) in the first slot position. This same airflow supply pattern is available in all BTX system designs.

The **Thermal Module Assembly (TMA)** consists of 4 main parts:

- The 92mm four-wire fan
- The plastic duct assembly (black)
- The heatsink (copper and aluminum)
- The metal retention clip (for holding the heatsink to the plastic duct assembly)

**Figure 3. BTX Type I Thermal Module Assembly (TMA)**





# 3.0 Development Kit Software and BIOS Features

This chapter provides an overview of development kit software and BIOS features.

## 3.1 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The driver CD included in the kit contains all of the software drivers necessary for basic system functionality under the following operating systems Windows 2000/XP/XP Embedded, and Linux.

*Note:* While every care was taken to ensure the latest version of drivers were provided on the enclosed CD at time of publication, newer versions may be available. Updated drivers for Intel components can be found at: http://developer.intel.com/design/intarch/software/driver/index.htm#q965.

For all third party components, please contact the appropriate vendor for updated drivers.

*Note:* Software in the kit is provided free by the vendor and is only licensed for evaluation purposes.

Refer to the documentation in the evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change. Refer to http://developer.intel.com/design/intarch/devkit for details on additional software from other third-party vendors.

## 3.2 BIOS Features

### 3.2.1 BIOS Overview

This development kit ships pre-installed with Intel BIOS. The BIOS provides an industry-standard BIOS platform to run most standard operating systems, including Windows* 2000/XP/XP Embedded, Linux*, WEPOS and others.

The BIOS is stored in a 16 Mb SPI flash at the primary SPI flash footprint at XU3LB and can be updated using a BIOS flash programming tool. FWH will not be supported

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <DELETE> key after the Power-On Self-Test (POST) memory test begins and before the screen goes black before booting any device. The menu bar is shown below.

**Figure 4. Menu Bar**

| |
|---|
| <MAIN> - <ADVANCED> - <PCIPnP> - <BOOT> - <SECURITY> - <CHIPSET> - <EXIT> |

Table 19 lists the BIOS setup program menu features.

**Table 19. BIOS Setup Program Menu Bar**

| Main | ADVANCED | PCIPnP | BOOT | SECURITY | CHIPSET | EXIT |
|---|---|---|---|---|---|---|
| Displays processor and memory configurations | Configures advanced features and settings | Setup for PCI and PCI Express* | Selects boot options and configurations | Sets passwords and security features | Configures different major components | Saves or discard changes to setup program options |

**Table 20. BIOS Setup Program Function Keys**

| BIOS Setup Program Function Key | Description |
|---|---|
| < or > | Selects a different menu screen (moves the cursor left or right) |
| ^ or | Selects an item (moves the cursor up or down) |
| Tab | Selects a field (not implemented) |
| Enter | Executes command or selects the submenu |
| F9 | Load the optimal default configuration values for the current menu |
| F10 | Save the current values and exits the BIOS setup program |
| ESC | Exits the menu |

## 3.2.2 Resource Configuration

### 3.2.2.1 PCI Auto Configuration

When a PCI card is added and the system is turned on, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to AVAILABLE in Setup are considered to be available for use by add-in card. There is one 32/33 PCI add-in card socket on the board.

### 3.2.2.2 SATA Drive Configuration

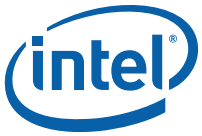
If you select AUTO in the BIOS Setup program, the BIOS automatically sets up the SATA drive configuration with independent I/O channel support. The interface also supports second-generation Serial ATA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.

To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying MANUAL CONFIGURATION in the BIOS setup program.

*Note:* This board only supports Serial ATA drives.

## 3.2.3 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network. The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components.



Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor clock frequency
- Dynamic data, such as event detection and error logging

Non-Plug and play operating systems such as Microsoft Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

### 3.2.4 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system.

After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, follow the operating system's installation instructions.

### 3.2.5 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, or from the network. The default setting is for the Hard Drive to be the first, and the CD-ROM to be the second. There is no third or fourth boot option.

#### 3.2.5.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

#### 3.2.5.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the on-board LAN or a network add-in card with a remote boot ROM installed. In order to boot from the LAN you will have to enter the BIOS and select LAN boot as your first boot device.

#### 3.2.5.3 Booting without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

#### 3.2.5.4 Changing the Boot Device

Pressing the <Delete> key during POST causes the BIOS menu to be displayed. Using your arrow keys move over to <BOOT> and then arrow down to <Boot Device Priority> and then select which device you would like to boot first and second.

*Note:* Please follow the instructions on the right side of the BIOS screen to navigate and change BIOS settings.

### 3.2.6 BIOS Security Features

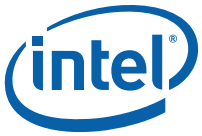
The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered. Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

For enhanced security, use different passwords for the supervisor and user passwords. Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

## 3.3 Graphics Drivers

The Intel® Q965 Express Chipset will work with the Intel® GMA3000 Extreme graphics driver or the Intel® Embedded Graphics Driver (IEGD).



IEGD is created specifically for embedded platforms, offering an adaptable alternative to drivers designed for the desktop market segments. IEGD offers Intel's embedded customers extended life support that correlates with the extended life support of Embedded IA-32 silicon products. IEGD differentiates itself through its configurability and support of unique embedded market segment requirements, including an unprecedented support of advanced display combinations, non-standard display dimensions, and embedded operating systems such as Microsoft* XP Embedded and WePOS.The Intel® Graphics Media Accelerator (GMA) is designed for mainstream desktop usage models focusing on 3D performance and ease of use.

When working with external graphics drivers, the internal graphics will automatically disable. When a discrete graphics card is plugged into to the graphics port (PEG), the integrated graphics will be disabled. Note that this does not apply to an ADD2 card, which is intended to work in conjunction with integrated graphics.

IEGD allows support of external discrete graphics cards in conjunction with integrated graphics when a discrete graphics card is plugged into the PCI Express* x1 or PCI at the ICH. If you have a discrete graphics card plugged into the PCI Express*, it will work in conjunction with the integrated graphics. Note that GMA drivers will not support this, only the IEGD drivers.

## 3.4 Intel® Active Management Technology

Intel® Active Management Technology (AMT) offers tamper-resistant and persistent management capabilities. Specifically, Intel AMT is a hardware-based solution that offers encrypted and persistent asset management and remote diagnostics and/or recovery capabilities for networked platforms. With Intel AMT, IT organizations can easily get accurate platform information, and can perform remote updating, diagnostics, debugging, and repair of a system, regardless of the state of the operating system and the power state of the system. Intel AMT enables IT organizations to discover, heal, and protect all of their computing assets, regardless of system state in the manner described below.

(1) Discovering hardware and software computing assets:

- Intel AMT stores hardware and software asset information in non-volatile memory and allows IT to read the asset information anytime, even if the PC is off.
- Users cannot remove or prevent IT organization access to the information because it does not rely on software agents.

(2) Healing systems remotely, regardless of the operating system or system state:

- Intel AMT provides out-of-band diagnostics and recovery capabilities for IT organizations to remotely diagnose and repair PCs after software, operating system, or hardware failures.
- Alerting and event logging help IT organizations detect and diagnose problems quickly to reduce end-user downtime.

(3) Protecting the enterprise against malicious software attacks:

- Intel AMT helps IT organizations keep software versions and virus protection consistent and up-to-date across the enterprise.
- Version information is stored in non-volatile memory for access anytime by third-party software to check and, if necessary, wake a system to perform off-hours updates.

(4) The key features of Intel AMT include:

- Secure Out of Band (OOB) system management that allows remote management of PCs regardless of system power or operating system state.

  - — SSL3.1/TLS encryption
  - — HTTP authentication
  - — TCP/IP
  - — HTTP web GUI
  - — XML/SOAP API
- Remote troubleshooting and recovery that can significantly reduce desk-side visits and potentially increase efficiency of IT technical staff.
  - — System event log
  - — IDE-Redirection or PXE boot; Network drive or remote CD boot
  - — Serial over LAN
  - — OOB diagnostics
  - — Remote control
  - — Remote BIOS update
- Proactive alerting that decreases downtime and minimizes time to repair.
  - — Programmable policies
  - — Operating system lock-up alert
  - — Boot failure alert
  - — Hardware failure alerts
- Third-party non-volatile storage that prevents users from removing critical inventory, remote control, or virus protection agents.
- Nonvolatile storage for agents
- Tamper-resistant
- Remote hardware and software asset tracking that eliminates time-consuming manual inventory tracking, which also reduces asset accounting costs.
  - — E-Asset Tag
  - — HW/SW inventory

For details of the AMT configurations, please contact your nearest Intel representatives for the Intel® AMT OEM Bring up Guide.

## 3.5 Intel® Quiet System Technology

Intel® ICH8 incorporated a new integrated Intel® Quiet System Technology (Intel QST) interface to provide a low cost solution for a better system thermal/acoustic management solution. Intel QST architecture consists of a Simple Serial Transfer (SST) bus, Platform Environment Control Interface (PECI), four TACH pins and three Pulse Width Modulation (PWM) output pins to monitor, control and manage the system target temperature through a sets of thermal sensors.

QST is run by the manageability engine (ME) residing in MCH and requires SPI flash to host the QST firmware.

Detailed of the QST configurations, please contact your nearest Intel representatives for the QST OEM Bring up Guide.

# 4.0 Setting Up & Configuring the Development Kit

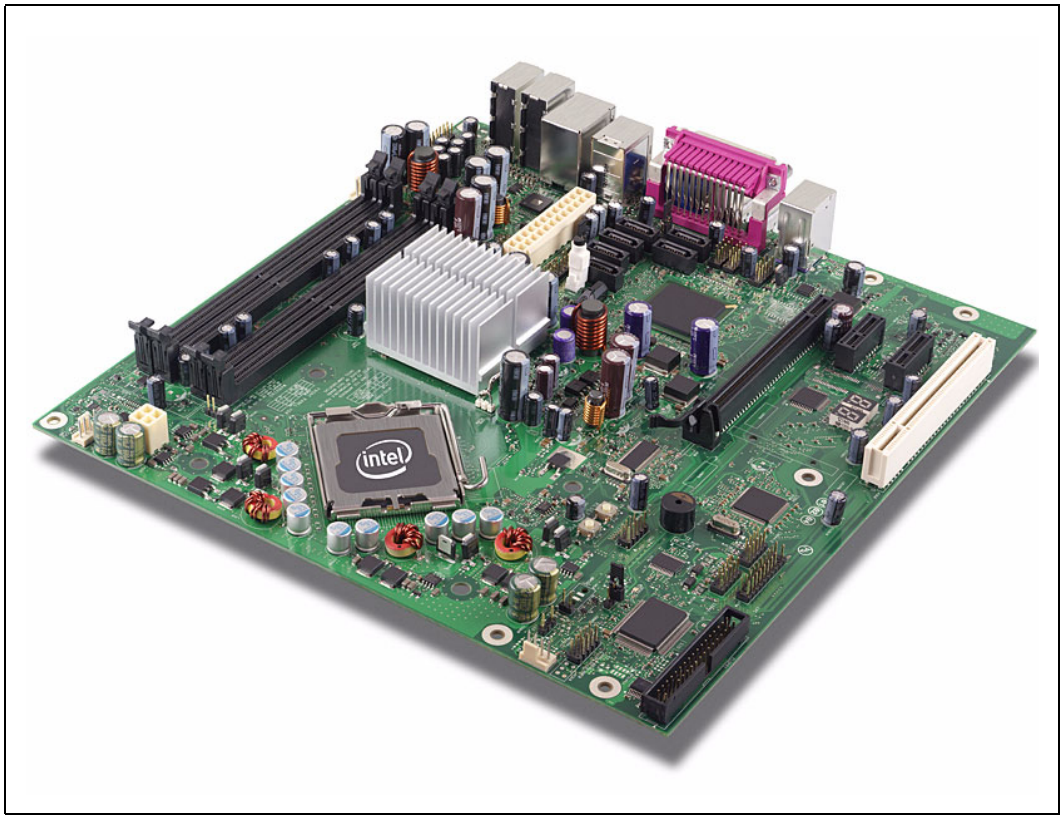
This chapter identifies the evaluation kit basic board's set up and operation. Please refer to Chapter 2.0 for the board layout, jumper setting location and the component reference designator.

## 4.1 Overview

The following hardware is included in the development kit:

- One Intel® Q965 Express Chipset Development Kit reference board.
- One Intel® Core™2 Duo processor E6400 2.13GHz
- One BTX Type I Thermal Module Assembly (TMA) CPU fan heatsink
- One Support and Retention Module (SRM) heatsink mounting plate
- Two 512 Mbyte DDR2 667MHz unbuffered DIMMs
- One Pre-programmed and installed 2 MB SPI Flash

**Figure 5. Development Kit Board**



## 4.2 Additional Hardware & Software Required

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

**VGA or LCD Monitor**

You can use any standard VGA or multi-resolution LCD monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.

**Keyboard**

You will need a PS/2 style or USB keyboard.

**Mouse**

You will need a PS/2 style or USB mouse.

**Hard Drives, Floppy Drives, and SATA or USB Optical Disk Drives**

You can connect up to six SATA drives to the evaluation board. A floppy drive or compact disc drive may be used to load the OS. No drives or cables are included in the kit; the user must provide them as necessary. All the storage devices may be attached to the board simultaneously.

**Video Adapter**

Integrated video is provided via the back panel of the system board. Alternately, users can choose to use any standard external PCI Express* x16 graphics card or MEC. It is user responsibility to install the appropriate drivers and correctly configure any software for video adapters used. Check the BIOS for the proper video settings.

**Power Supply**

The evaluation board is recommended to power up using a standard desktop BTX/ATX 12 V Rev 2.2 power supply that support enhanced BTX system thermal performance. It is recommended the power supply have a minimum of 500 W output and active PFC (power factor correction). The power supply selected must also provide an auxiliary 2x2 12 V connector.

**Other Devices and Adapters**

The evaluation board functions much like a standard desktop computer motherboard. Most PC-compatible peripherals can be attached and configured to work with the evaluation board.

## 4.3 Setting Up the Evaluation Board

Once the hardware described in Section 4.2 is gathered, follow the steps below to set up the evaluation board. This manual assumes you are familiar with the basic concepts involved with installing and configuring hardware for a personal computer system.

*Note:* To locate items discussed in the procedure below, please refer to Chapter 3.0.

1. Create a safe work environment.
2. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge damage, and such damage may cause product failure or unpredictable operation.

Inspect the contents of your kit.

3. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

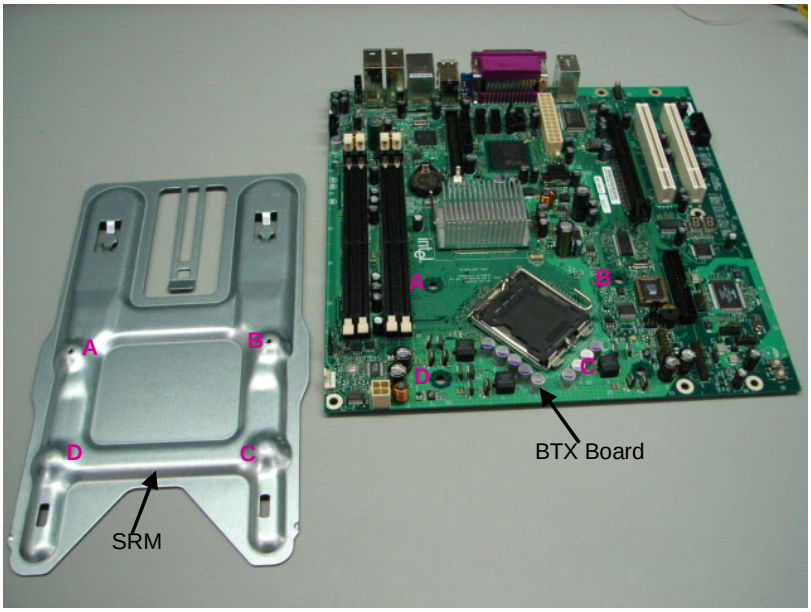
***Caution:*** Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

***Caution:*** Standby voltage is constantly applied to the board. Therefore, do not insert or remove any hardware unless the system is unplugged.

*Note:* The evaluation board is a µBTX form factor. A µBTX chassis may be used if a protected environment is desired.

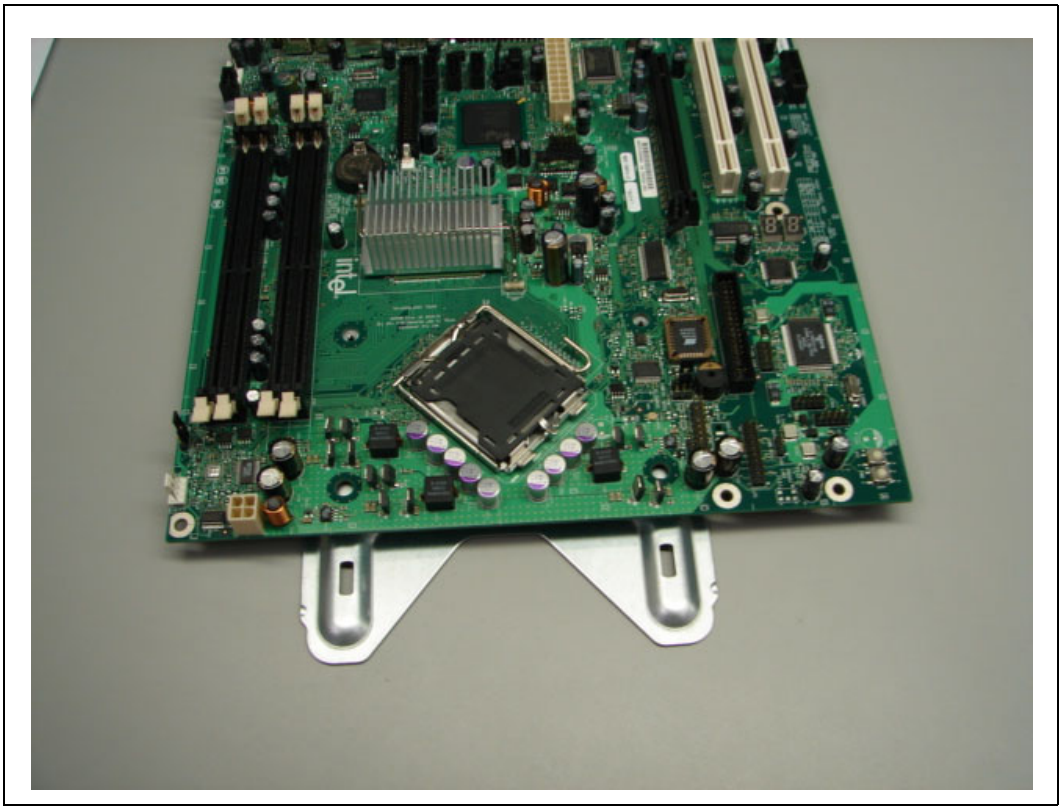
4. Check the jumper settings (refer to Chapter 3.0). Jumper **J6LB** is used to clear the CMOS memory. Make sure this jumper is set for normal operation.
5. Insert the processor (enclosed in the kit is Intel® Core™2 Duo processor E6400) into the LGA775 socket
6. Attach the BTX Thermal Module Assembly (TMA) over the processor to the Support and Retention Module (SRM) by following procedures described below.
7. Place the uBTX board on the Support and Retention Module (SRM) so that the holes A, B, C and D on the PCB line up with the corresponding locations on the SRM (see Figure 6).

**Figure 6. Align the Development Kit Board and SRM**



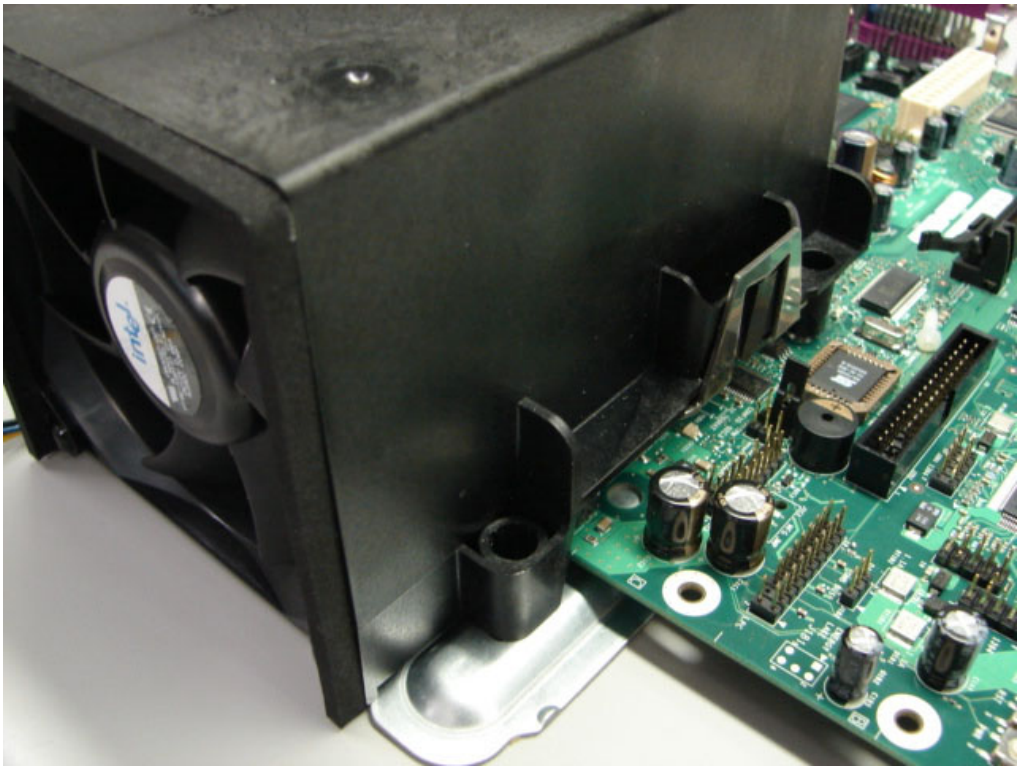
The board and SRM assembly should look like the figure below.

**Figure 7. Assembled SRM and board**



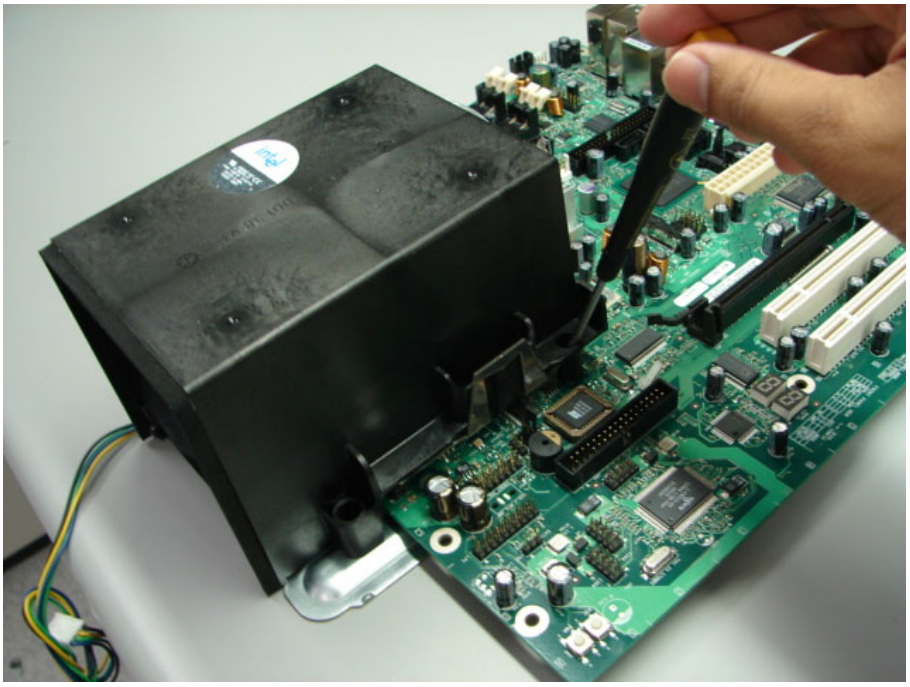
Place the heatsink on top of the processor. The heatsink should align with the holes on the SRM and board as shown below in Figure 7. Please clean the surface of the processor with isopropyl alcohol before attaching the heatsink.

**Figure 8. Align the heatsink with holes on the SRM and board**



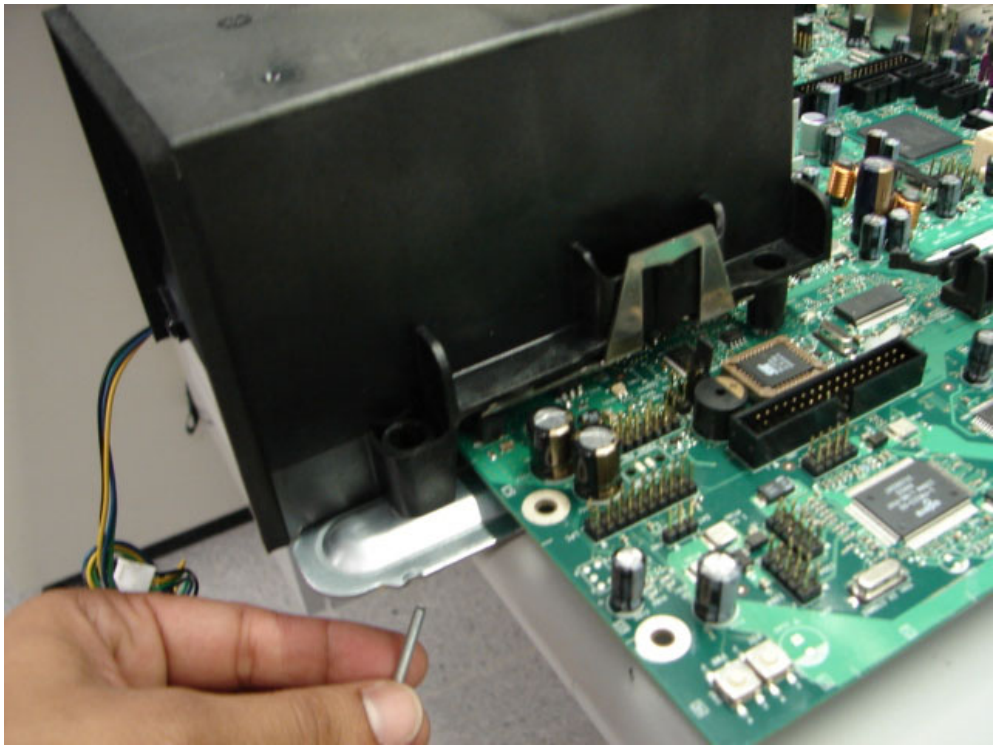
Use two 6-32 screws to partially tighten the rear end of the heatsink to the board and the SRM as shown in Figure 9. The screw uses the threaded holes of the SRM for retention.

**Figure 9. Tighten the heatsink on the SRM and board**



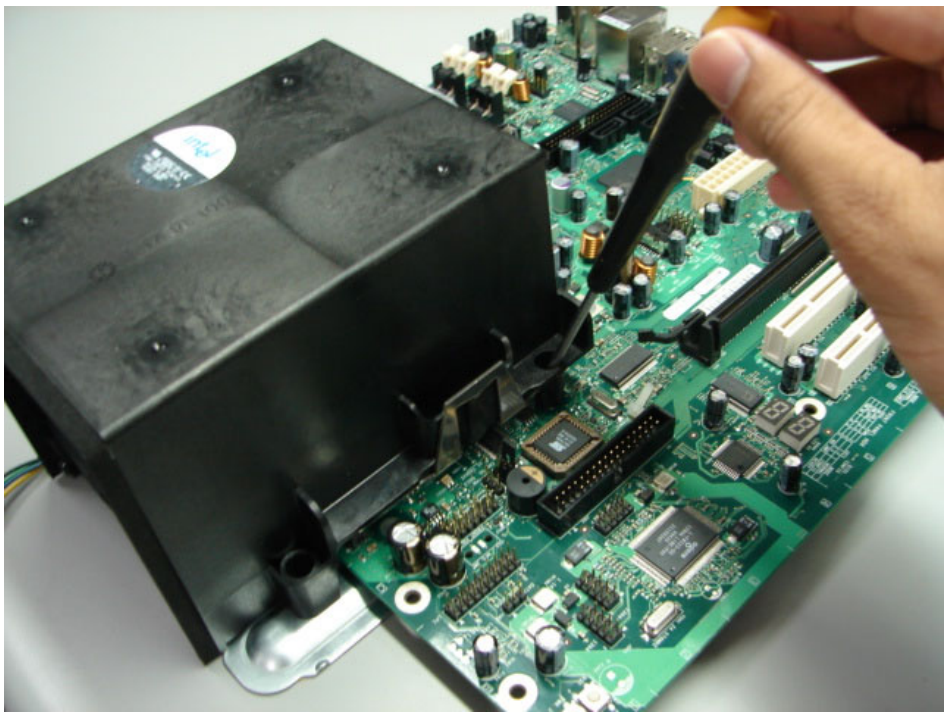
Use two 6-32 nuts and two bolts to secure the front side of the heatsink to the SRM. The screw can be dropped from the top and use a nut at the bottom or the screw can be inserted from the base of the SRM into the heatsink (based on the accessibility of the system).

**Figure 10. Secure the front side of the heatsink to the SRM**



Tighten the screws at the rear end of the heatsink as shown in the figure below.

**Figure 11. Secure the read end of heatsink to the SRM**



*Note:* Please make sure all the screws are tightened before using the system.

8. Plug the processor heat sink fan into J3TH.
9. Connect the SATA drive through SATA cable into J24LB (SATA 0). Connect a power cable to the SATA drive.
10. (Optional) Plug the floppy disk drive through the ribbon cable into J4LH. Connect a power cable to the floppy drive.
11. Insert the two DDR2 memory (enclosed in the kit are two 512 Mbyte DDR2 667MHz unbuffered DIMMs) into slots J1MY and J3MY. Optional to insert DDR2 memory into slots J2MY and J4MY.
12. Insert a USB CD or DVD into one of the USB ports (J17LB) at the back panel. Optional to plug a SATA CD or DVD into J22LB.
13. Connect a PS/2 Keyboard into J5LH (purple connector) at the back panel. Optional to connect a USB keyboard into J17LB.
14. Connect a PS/2 Mouse into J5LH (green connector) or a USB Mouse into one of the USB ports (J17LB) at the back panel.
15. Optional to connect a PCI Express x16 graphics card into J6UB. Optional to install a MEC card into J6UB.
16. Plug the front panel header cable into J28LB.
17. Plug the monitor into the VGA connector J4UB or Plug the monitor into the add in graphics card's video connector.
18. Optional to connect the audio speakers to J4AU and J5AU (Please refer to Chapter 2.0 for details).

19. Optional to connect an Ethernet cable to LAN MagJack connector at J18LB.
20. Connect a standard recommended BTX power supply to the board. Plug the BTX 2x12 connector into J2BV power supply header. Plug the BTX 2x2 12V connector into J1BV.
21. Press the J9LB Power Button to power up the board. Turn on the power to the monitor and evaluation board. Ensure that the fan sink on the processor is operating.

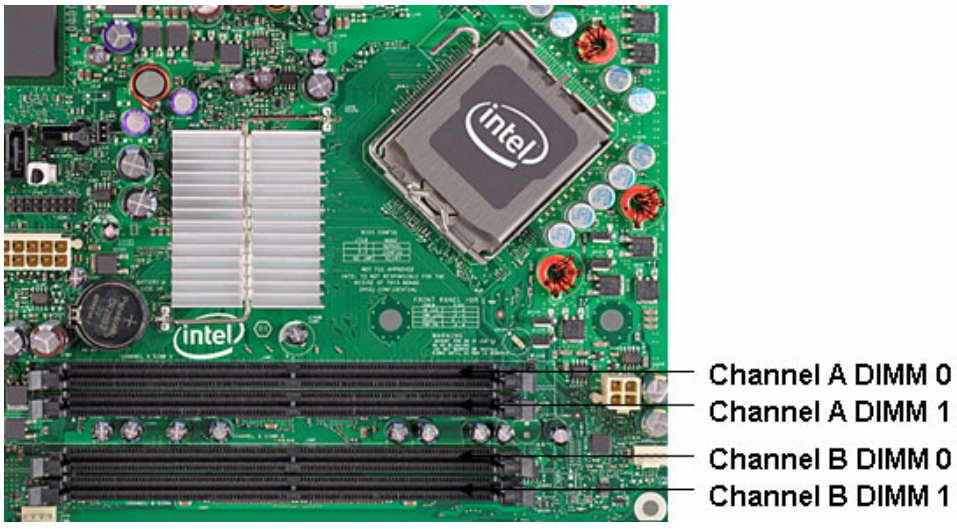
### 4.3.1 Memory Configurations

The Intel Q965 MCH supports two types of memory organization:

**Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speeds DIMMs are used between channels, the slowest memory timing will be used.

**Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speeds DIMMs are used between channels, the slowest memory timing will be used.

**Figure 12. Memory Channel and DIMM Configuration**



#### 4.3.1.1 Dual Channel (Interleaved) Mode Configurations

Figure 13 shows a dual channel configuration using two DIMMs. In this example, the DIMM 0 sockets of both channels are populated with identical DIMMs.

**Figure 13. Dual Channel (Interleaved) Mode Configuration with two DIMMs**

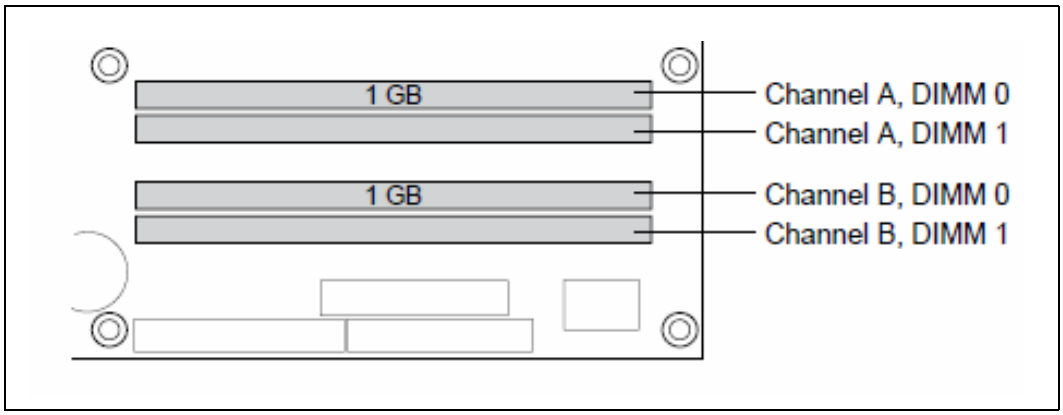



Figure 14 shows a dual channel configuration using three DIMMs. In this example, the combined capacity of the two DIMMs in Channel A equal the capacity of the single DIMM in the DIMM 0 socket of Channel B.

**Figure 14. Dual Channel (Interleaved) Mode Configuration with three DIMMs**

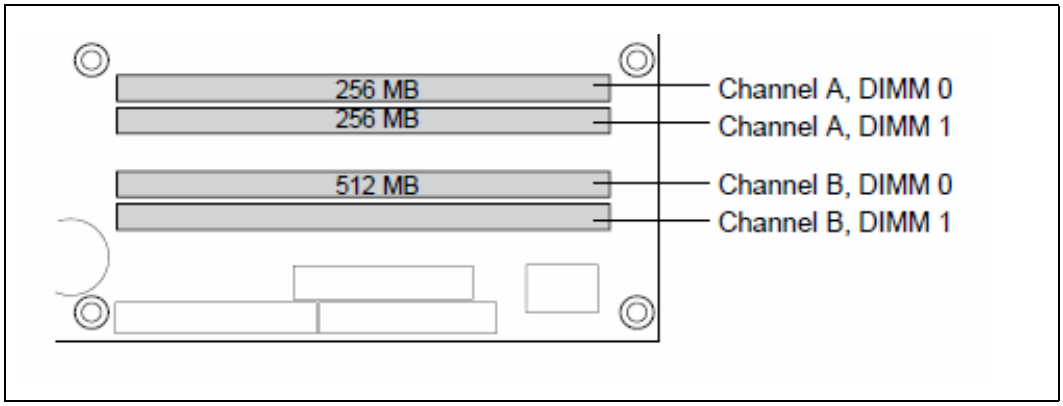
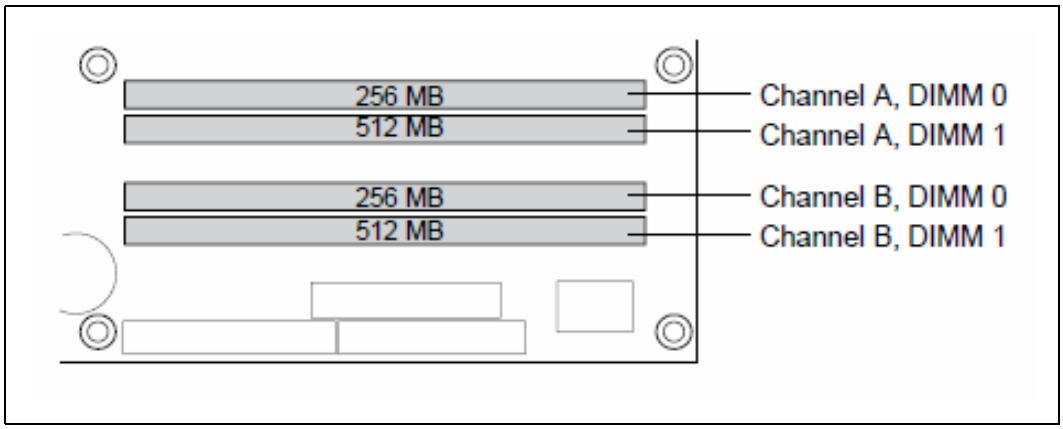


Figure 15 shows a dual channel configuration using four DIMMs. In this example, the combined capacity of the 2x DIMMs in Channel A equals the combined capacity of the 2x DIMMs in Channel B. Also, the DIMMs are matched between DIMM 0 and DIMM 1 of both channels.

**Figure 15. Dual Channel (Interleaved) Mode Configuration with four DIMMs**




### 4.3.1.2 Single Channel (Asymmetric) Mode Configurations

Figure 16 shows a single channel configuration using 1x DIMM. In this example, only the DIMM 0 socket of Channel A is populated. Channel B is not populated.

**Figure 16. Single Channel (Asymmetric) Mode Configuration with one DIMM**

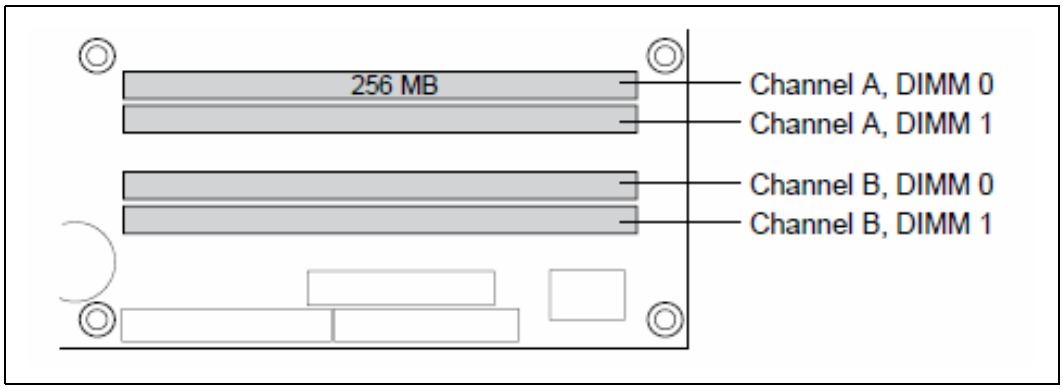
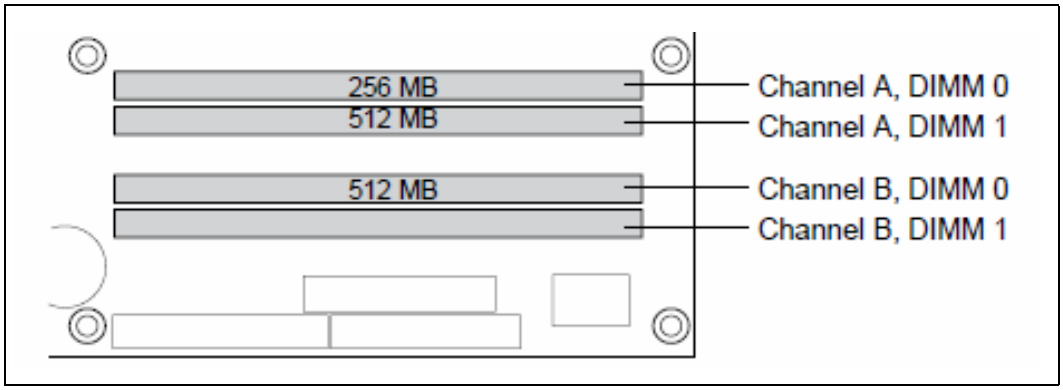


Figure 17 shows a single channel configuration using 3x DIMMs. In this example, the combined capacity of the 2x DIMMs in Channel A does not equal the capacity of the single DIMM in the DIMM 0 socket of Channel B.

**Figure 17. Single Channel (Asymmetric) Mode Configuration with 3x DIMMs**




## 4.4 Audio Subsystem Configurations

The board supports the Intel® High Definition Audio subsystem based on the ADI1988A or 1988B audio codec. The ADI1988 series provides eight channels of DAC (Digital to Analog Converter) that simultaneously support 7.1 sound playback.

The board contains audio connectors on the back panel and two channels of independent stereo sound output at the side of the board. The functions of the back panel audio connectors are dependent on the eight-channel audio subsystem, as described in Chapter 2.0.

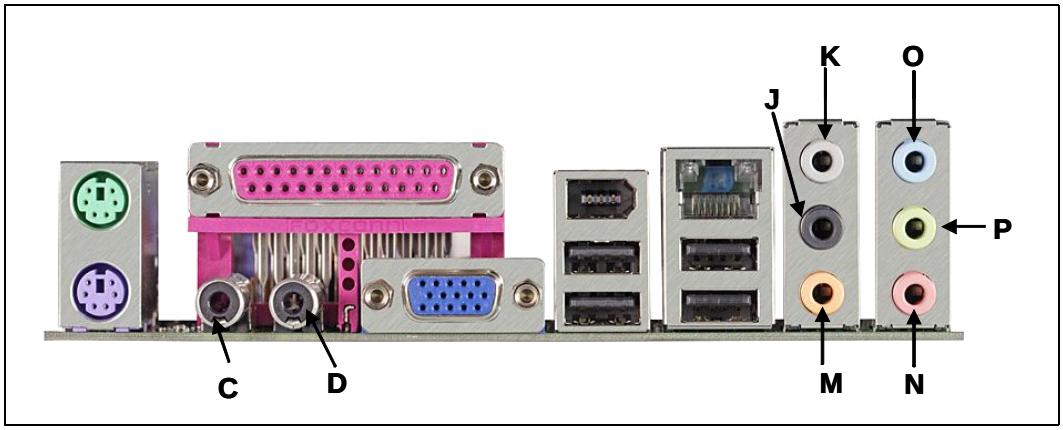
For more information such as specification, schematic, layout and driver on the ADI1988 audio codec, please refer to the ADI website at www.adi.com

### 4.4.1 Eight-Channel (7.1) Audio Subsystem

Figure 18 shows the back panel audio connector for the eight-Channel (7.1) Audio Subsystem. The eight-channel (7.1) audio subsystem includes the following:

- Intel® 82801G I/O Controller Hub (ICH8DO)
- ADI1988 audio codec

**Figure 18. Back Panel Audio Connector Options for Eight-channel Audio Subsystem**



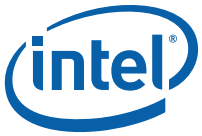


Table 21 describes the lists of back panel task.

**Table 21. Back panel task (Audio)**

| Symbols | Task |
|---|---|
| C | S/PDIF Out |
| D | S/PDIF In |
| K (Gray) | Side Speaker Out |
| J (Black) | Rear Speaker Out |
| M (Orange) | Center channel and Subwoofer audio out |
| O (Light Blue) | Audio Line In |
| P (Green) | Audio Line Out (Front Speaker Out) |
| N (Pink) | Mic In |

## 4.5 LAN Subsystem Configurations

The LAN subsystem consists of the following:

- Physical layer interface device. The development kit include the following LAN devices:
  - — Intel® 82566DM for Gigabit (10/100/1000 Mbits/sec) Ethernet LAN connectivity.
- RJ-45 LAN connector with integrated status LEDs.

### 4.5.1 Gigabit LAN Subsystem

The Gigabit (10/100/1000 Mbits/sec) LAN subsystem includes the Intel® 82566DM controller and a RJ-45 LAN connector with integrated status LEDs.

The Intel® 82566DM Gigabit Ethernet Controller supports the following features:

- PCI Express* link
- 10/100/1000 IEEE 802.3 compliant
- Compliant to IEEE 802.3x flow control support
- TCP, IP, UDP checksum offload
- Transmit TCP segmentation
- Advanced packet filtering
- Full device driver compatibility
- PCI Express* Power Management Support
- Jumbo frame support
- Intel® Active Management Technology
- Alert Standard Format (ASF) 2.0

### 4.5.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector as shown in Figure 19. Table 22 describes the LED states when the board is powered up and the Gigabit LAN subsystem is operating.

**Figure 19. LAN Connector LED locations**

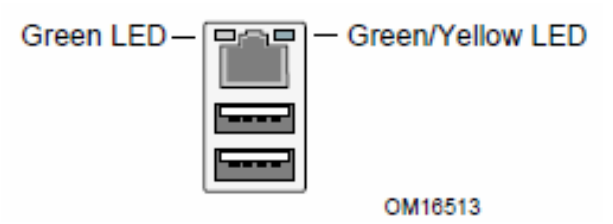



**Table 22. LAN Connector LED status**

| LED | Color | LED State | Condition |
|---|---|---|---|
| Left | Green | Off | LAN link is not established. |
| | | On | LAN link is established. |
| | | Blinking | LAN activity is occurring. |
| Right | N/A | Off | 10 Mbits/sec data rate is selected |
| | Green | On | 100 Mbits/sec data rate is selected |
| | Yellow | On | 1000 Mbits/sec data rate is selected |

## 4.6 Software Kit Installation

### 4.6.1 Installation of a new Operating System

The user will required to install a new operating system on a SATA hard disk using an optical drive or loading an image to the hard disk.

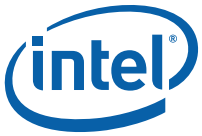
### 4.6.2 Drivers Installation

Once the image is loaded onto the platform and the clean build of OS is done,

Install all the relevant drivers:

- Intel® Chipset Software Installation Utility – Chipset INF files needs to be installed first
- Intel® Embedded Graphics Drivers or Intel® Graphics Media Accelerator Drivers
- Intel® PRO Network Connections LAN Driver
- Others optional – HECI driver, AMT Serial Over LAN, Intel® Management Engine Interface Driver (QST), Intel Matrix Storage Manager

After installation, go to device manager and make sure there are no “!” (Yellow bangs) on the devices.



# 5.0 Error Messages and Beep Codes

This chapter describes the various progress codes that are reported by the BIOS and the corresponding LED Codes.

The LED codes are 8-bit quantities and can be used as Port 80 codes if the platform supports Port 80 capturing device. The higher nibble alone is used for a 4-bit LED.

The Status code driver is responsible for translating the Standard Progress/Error code into a one-byte value. The particular enumeration scheme is set up so that the Port 80 code values will typically increase during the boot process. The early codes are for subsystems closer to the processor and the later codes are for peripherals.

Typically, the order of initialization is Processor -> Memory -> Busses -> Output/Input Devices -> Boot Devices

or

Processor -> Memory -> Recovery -> Busses ->
Output/Input Devices -> Boot Devices

The sequence of POST is platform-specific.

## 5.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST. For information about the location of the onboard speaker refer to Figure 1.

## 5.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS “beep” as described in the following table, Table 23.

**Table 23. Beep codes**

| Type | Pattern | Frequency |
|---|---|---|
| Memory error | Three long beeps | 1280 Hz |
| Thermal warning | Four alternating beeps:<br>High tone, low tone, high tone, low tone | High tone: 2000 Hz<br>Low tone: 1600 Hz |

## 5.3 BIOS Error Messages

Table below show the lists of BIOS error messages and brief description of each.

**Table 24. Lists of error messages and brief description of each**

| Error Message | Explanation |
|---|---|
| CMOS Battery low | The battery may be losing power. Replace the battery soon. |
| CMOS Checksum Bad | The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values. |
| Memory Size Decreased | Memory size has decreased since the last boot. If no memory was removed, then memory may be bad. |
| No Boot device available | System did not find a device to boot. |

## 5.4 Port 80h POST Codes

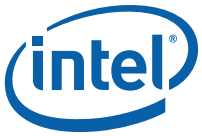
During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

The following tables provide information about the POST codes generated by the BIOS:

- Table 25 lists the Port 80h POST code ranges
- Table 26 lists the Port 80h Progress Code Enumeration
- Table 27 lists the Port 80h POST sequence

**Table 25. Port 80h POST Code Ranges**

| Range | Subsystem |
|---|---|
| 0x00 – 0x0F | Debug codes: Can be used by any PEIM/driver for debug. Blocked on production builds per DFT rule. Not covered in the EPS. |
| 0x10 – 0x1F | Host Processors: 0x1F is unrecoverable CPU error. |
| 0x20 – 0x2F | Memory/Chipset: 0x2F is no memory detected or no useful memory detected. |
| 0x30 – 0x3F | Recovery: 0x3F indicated recovery failure. |
| 0x40 – 0x4F | Reserved for future. |
| 0x50 – 0x5F | IO Busses: PCI, USB, ISA, ATA etc. 0x5F is unrecoverable error. Start with PCI. |
| 0x60 – 0x6F | Reserved for future (for new busses). |
| 0x70 – 0x7F | Output Devices: All output consoles. 0x7F is unrecoverable error. |
| 0x80 – 0x8F | Reserved for future (new output console codes). |
| 0x90 – 0x9F | Input devices: Keyboard/Mouse. 0x9F is unrecoverable error. |
| 0xA0 – 0xAF | Reserved for future (new input console codes). |
| 0xB0 – 0xBF | Boot Devices: Includes Fixed media and removable media. Not that critical since consoles should be up at this point. 0xBF is unrecoverable error. |
| 0xC0-0xCF | Reserved for future. |
| 0xD0-0xDF | Boot Device Selection. |
| 0xE0 – 0xFF | 0xF0 – 0xFF: 0xFF processor exception. 0xE0- 0xEE: Miscellaneous codes. See below. 0xEF boot/S3: resume failure. |

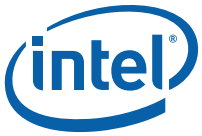


## Table 26. Port 80h Progress Code Enumeration

| Port 80 code | Progress Code Enumeration |
|---|---|
| | **HOST PROCESSOR:** |
| 0x10 | Power-on initialization of the host processor (Boot Strap Processor) |
| 0x11 | Host processor Cache initialization (including APs) |
| 0x12 | Starting Application processor initialization |
| 0x13 | SMM initialization |

| Port 80 code | Progress Code Enumeration |
|---|---|
| **Chipset** | |
| 0x21 | Initializing a chipset component |
| **Memory** | |
| 0x22 | Reading SPD from memory DIMMs |
| 0x23 | Detecting presence of memory DIMMs |
| 0x24 | Programming timing parameters in the memory controller and the DIMMs |
| 0x25 | Configuring memory |
| 0x26 | Optimizing memory settings |
| 0x27 | Initializing memory, such as ECC init |
| 0x28 | Testing memory |
| **PCI Bus** | |
| 0x50 | Enumerating PCI busses |
| 0x51 | Allocating resources to PCI bus |
| 0x52 | Hot Plug PCI controller initialization |
| 0x53-0x57 | Reserved for PCI Bus |
| **USB** | |
| 0x58 | Resetting USB bus |
| 0x59 | Reserved for USB |
| **ATA/ATAPI/SATA:** | |
| 0x5A | Resetting PATA/SATA bus and all devices |
| 0x5B | Reserved for ATA |
| **SMBUS** | |
| 0x5C | Resetting SMBUS |
| 0x5D | Reserved for SMBUS |
| **LOCAL CONSOLE:** | |

| Port 80 code | Progress Code Enumeration |
|---|---|
| 0x70 | Resetting the VGA controller |
| 0x71 | Disabling the VGA controller |
| 0x72 | Enabling the VGA controller |
| **Remote Console** | |
| 0x78 | Resetting the console controller |
| 0x79 | Disabling the console controller |
| 0x7A | Enabling the console controller |
| **Keyboard (PS2 or USB)** | |
| 0x90 | Resetting keyboard |
| 0x9 | Disabling the keyboard |
| 0x9 | Detecting the presence of the keyboard |
| 0x9 | Enabling the keyboard |
| 0x9 | Clearing keyboard input buffer |
| 0x9 | Instructing keyboard controller to run Self Test (PS2 only) |
| **Mouse (PS2 OR USB)** | |
| 0x98 | Resetting mouse |
| 0x99 | Detecting mouse |
| 0x9A | Detecting presence of mouse |
| 0x9B | Enabling mouse |
| **Fixed Media** | |
| 0xB0 | Resetting fixed media |
| 0xB1 | Disabling fixed media |
| 0xB2 | Detecting presence of a fixed media (IDE hard drive detection etc.) |
| 0xB3 | Enabling/configuring a fixed media |
| **Removable Media** | |
| 0xB8 | Resetting removable media |
| 0xB9 | Disabling removable media |
| 0xBA | Detecting presence of a removable media (IDE, CDROM detection etc.) |
| 0xBC | Enabling/configuring a removable media |
| **BDS** | |
| 0xDy | Trying boot selection y (y=0 to 15) |
| **PEI Core** | |
| 0xE0 | Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT |
| 0xE2 | Permanent memory found. |
| 0xE1,0xE3 | Reserved for PEI/PEIMs |



| Port 80 code | Progress Code Enumeration |
|---|---|
| **DXE Core** | |
| 0xE4 | Entered DXE phase |
| 0xE5 | Started dispatching drivers |
| 0xE5 | Started connecting drivers |
| **DXE Drivers** | |
| 0xE7 | Waiting for user input |
| 0xE8 | Checking password |
| 0xE9 | Entering BIOS setup |
| 0xEA | TBD – Flash Update |
| 0xEB | Calling Legacy Option ROMs |
| 0xEE | TBD – Calling Int 19. One beep unless silent boot is enabled. |
| 0xEF | TBD – Unrecoverable Boot failure/S3 resume failure |
| **RUNTIME PHASE/EFI OS BOOT** | |
| 0xF4 | Entering Sleep state |
| 0xF5 | Exiting Sleep state |
| 0xF8 | EFI boot service ExitBootServices ( ) has been called |
| 0xF9 | EFI runtime service SetVirtualAddressMap ( ) has been called |
| 0xFA | EFI runtime service ResetSystem ( ) has been called |
| **PEIMS/RECOVERY** | |
| 0x30 | Crisis Recovery has initiated per User request |

| Port 80 code | Progress Code Enumeration |
|---|---|
| 0x31 | Crisis Recovery has initiated by software (corrupt flash) |
| 0x34 | Loading recovery capsule |
| 0x35 | Handing off control to the recovery capsule |
| 0x3F | Unable to recover |

## Table 27. Typical Port 80h POST Sequence (Sheet 1 of 2)

| Port 80 code | Progress Code Enumeration |
|---|---|
| 0x21 | Initializing a chipset component |
| 0x22 | Reading SPD from memory DIMMs |
| 0x23 | Detecting presence of memory DIMMs |
| 0x25 | Configuring memory |
| 0x28 | Testing memory |
| 0x34 | Loading recovery capsule |

## Table 27. Typical Port 80h POST Sequence (Sheet 2 of 2)

| Port 80 code | Progress Code Enumeration |
|---|---|
| 0xE4 | Entered DXE phase |
| 0x12 | Starting Application processor initialization |
| 0x13 | SMM initialization |
| 0x50 | Enumerating PCI busses |
| 0x51 | Allocating resources to PCI bus |
| 0x92 | Detecting the presence of the keyboard |
| 0x90 | Resetting keyboard |
| 0x94 | Clearing keyboard input buffer |
| 0x95 | Keyboard Self Test |
| 0xEB | Calling Video BIOS |
| 0x58 | Resetting USB bus |
| 0x5A | Resetting PATA/SATA bus and all devices |
| 0x92 | Detecting the presence of the keyboard |
| 0x90 | Resetting keyboard |
| 0x94 | Clearing keyboard input buffer |
| 0x5A | Resetting PATA/SATA bus and all devices |
| 0x28 | Testing memory |
| 0x90 | Resetting keyboard |
| 0x94 | Clearing keyboard input buffer |
| 0xE7 | Waiting for user input |
| 0x01 | Int 0x19 |
| 0x00 | Ready to boot. |