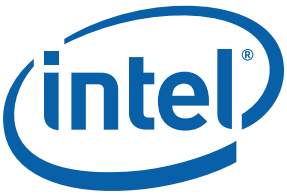

Intel® IXP45X and Intel® IXP46X Product Line of Network Processors

Hardware Design Guidelines

February 2007

Document No:305261; Revision:004

Contents

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Revision History

Date	Revision	Description
February 2007	004	• Section 1.4, Figure 1, Figure 2, Section 3.5: Updated the number of supported SMII ports from six to three. • Table 11, Table 12, Table 16: Updated pin type for UTP_OP_ADDR[4:0], UTP_IP_ADDR[4:0], and ETH_MDC. • Section 7.0, "DDR-SDRAM" : Updated design information. • Removed SS-SMII references since this feature is not supported. • Incorporated specification changes, specification clarifications and document changes from the *Intel® IXP4XX Product Line of Network Processors Specification Update* (306428-006) • Updated Intel® product branding.
August 2005	003	The following changes were made in this release: • Table 4: added ECC signal interface recommendation. • Table 5: corrected EX_IOWAIT_N and EX_WAIT_N pull-up recommendations. • Section 3.3.2, Table 5, Section 3.3.3, Section 3.3.4, and Section 3.3.6: changed pull-down resistor value from 10K to 4.7K. • Table 16: corrected UTP_OP_SOC pull-down recommendation. • Section 3.12.2: clarified description. • Added new information: Section 3.12.3, "Supporting 5 V PCI Interface" and Section 3.12.4, "PCI Option Interface" . • Section 3.12.5: clarified 5V support. • Table 24: updated power supply requirements for 667 MHz core speed processor. • Section 6.2 and Section 6.3: enhanced description, figure, and tables. • Section 7.1.7.1: enhanced clock group routing guidelines.
May 2005	002	Updated to add support for Intel® IXP455 Network Processor. Section 3.2.1: enhanced signal descriptions for DDRI_CK[2:0] and DDRI_CB[7:0].
March 2005	001	Initial release of document.

1.0 Introduction

This design guide provides recommendations for hardware and system designers who are developing with the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. This document should be used in conjunction with the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet* and sample schematics provided for the Intel® IXDP465 Development Platform in that platform's documentation kit.

Design Recommendations are necessary to meet the timing and signal quality specifications.

The guidelines recommended in this document are based on experience and simulation work done at Intel while developing the Intel® IXDP465 Development Platform. These recommendations are subject to change.

Note: This document discusses all features supported on the Intel® IXP465 Network Processor. A subset of these features is supported by certain processors in the IXP45X/ IXP46X product line, such as the Intel® IXP460 or Intel® IXP455 network processors. For details on feature support listed by processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

1.1 Content Overview

Chapter Name	Description
Chapter 1.0, "Introduction"	Conventions used in this manual and related documentation
Chapter 2.0, "System Architecture"	System architectural block diagram and system memory map
Chapter 3.0, "General Hardware Design Considerations"	Graphical representation of most common peripheral interfaces.
Chapter 4.0, "General PCB Guide"	General PCB design practice and layer stack-up description
Chapter 5.0, "General Layout and Routing Guide"	More specific layout and routing recommendations for board designers
Chapter 6.0, "PCI Interface Design Considerations"	Board-design recommendations when implementing PCI interface
Chapter 7.0, "DDR-SDRAM"	Board-design recommendations when implementing DDRI memory interface

1.2 Related Documentation

The reader of this design guide should also be familiar with the material and concepts presented in the following documents:

Title	Document #
Hardware-Assisted IEEE 1588* Implementation in the Intel® IXP46X Product Line White Paper	305068
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual	306262
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet	306261
Intel® IXP4XX Product Line of Network Processors Specification Update	306428
Intel® IXP400 Software Programmer's Guide	252539
Intel® IXP400 Software Specification Update	273795
Intel® XScale™ Core Developer's Manual	273473
Intel® IXDP465 Development Platform Documentation Kit	N/A
Intel XScale® Microarchitecture *Technical Summary*	—
Intel StrataFlash® Memory (J3) to Intel® Embedded Memory (J3 v.D) Conversion Guide - Application Note 835	308555
Migration Guide for Intel StrataFlash® Synchronous Memory (J3) to Intel StrataFlash® Embedded Memory (P30 and P33) - Application Note 812	306667
Migration Guide for Intel StrataFlash® Synchronous Memory (K3/ K18) to Intel StrataFlash® Embedded Memory (P30) - Application Note 825	306669
Double Data Rate (DDR) SDRAM Specification, 2004; JEDEC Solid State Technology Association	JESD79D
I^2C-Bus Specification from Philips Semiconductors*	Available at http://www.nxp.com
IEEE 802.3 Specification	N/A
IEEE 1149.1 Specification	N/A
PCI Local Bus Specification, Rev. 2.2	N/A
Universal Serial Bus Specification, Revision 1.1	N/A
UTOPIA Level 2 Specification, Revision 1.0	N/A
Note: For Intel documentation, see the Intel Technical Documentation Center, available through the following link: http://www.intel.com/products/index.htm	

1.3 Acronyms and Abbreviations

Table 1 lists the acronyms and abbreviations used in this guide.

Table 1. List of Acronyms and Abbreviations

Term	Explanation
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
ATM	Asynchronous Transfer Mode
DDR	Double Data Rate
EMI	Electro-Magnetic Interference
GPIO	General Purpose Input/Output
HSS	High Speed Serial
I2C	Inter-Integrated Circuit
IP	Internet Protocol
ISA	Instruction Set Architecture
LAN	Local Area Network
MII	Media-Independent Interface
NPE	Network Processor Engine
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PHY	Physical Layer Interface
PLL	Phase-Locked Loop
PMU	Performance Monitoring Unit
SDRAM	Synchronous Dynamic Random Access Memory
SME	Small-to-Medium Enterprise
SMII	Serial Media-Independent Interface
SSP	Synchronous Serial Protocol
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VTT	Termination Voltage Supply

1.4 Overview

The IXP45X/IXP46X network processors are highly integrated devices, capable of interfacing with most common industry standard peripherals, required for high-performance control applications.

Note: This document discusses all features supported on the Intel® IXP465 Network Processor. A subset of these features is supported by certain processors in the IXP45X/IXP46X product line, such as the Intel® IXP460 or Intel® IXP455 network processors. For details on feature support listed by processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

Some of the key features of the IXP45X/IXP46X network processors, when used as a single-chip solution for embedded applications, are as follows:

- Intel XScale® Processor (compliant with Intel® StrongARM* architecture) — Up to 667 MHz

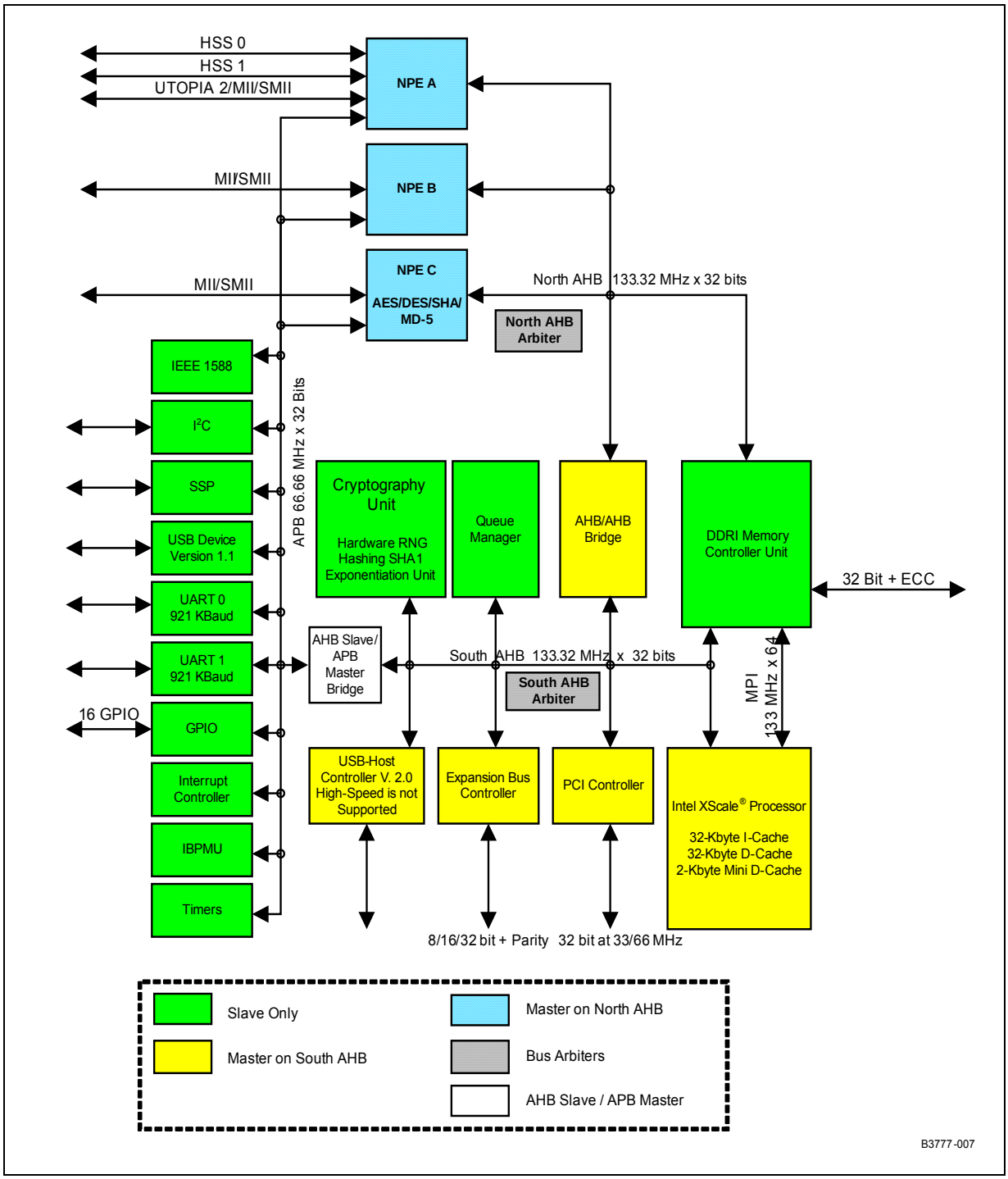
- 32-bit PCI interface Master/Target 33/66 MHz
- Device Universal Serial Bus (USB) Controller
- Host Universal Serial Bus (USB) Controller
- DDRI-266 SDRAM (133-MHz Clock, 266-Mbps per data line) — User-enabled ECC, supports up to 1 Gbyte of external memory
- 32-bit Expansion Bus Interface — Master/Target interface
- Two UART ports
- Up to three Ethernet ports (consult device part number for enabled features) MII/ SMII
- Up to three NPEs
- UTOPIA Level 2 Interface
- Synchronous Serial Port Interface (SSP)
- Two High-Speed Serial Port Interfaces (HSS)
- Inter-Integrated Circuit (IIC or I2C) Interface
- 16 GPIO (General Purpose Input Output)
- Packaging
  - — 544-pin PBGA package
  - — Commercial temperature (0° to +70° C)
  - — Extended temperature (-40° to +85° C)

For a complete features list and block diagram description, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

Note: Some features require Intel-supplied software. To determine if a feature is enabled in a particular software release, refer to the *Intel® IXP400 Software Specification Update*.

A block diagram of all major internal hardware components of the IXP465 network processor is given in Figure 1. The illustration also shows how the components interface with each other through the various bus interfaces such as the North AHB, South AHB, and APB.

Figure 1. Intel® IXP465 Component Block Diagram



Note: Figure 1 shows the Intel® IXP465 Network Processor. For details on feature support listed by processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

1.5 Typical Applications

- High-performance DSL modem
- High-performance cable modem
- Residential gateway
- SME router
- Integrated access device (IAD)
- Set-top box
- DSLAM
- Access points — 802.11a/b/g
- Industrial controllers
- Network printers
- VoIP Gateways

2.0 System Architecture

2.1 System Architecture Description

The Intel® IXP45X and Intel® IXP46X Product Line of Network Processors are multi-function processors that integrate the Intel XScale® Processor (ARM* architecture compliant) with highly integrated peripheral controllers and intelligent network processor engines.

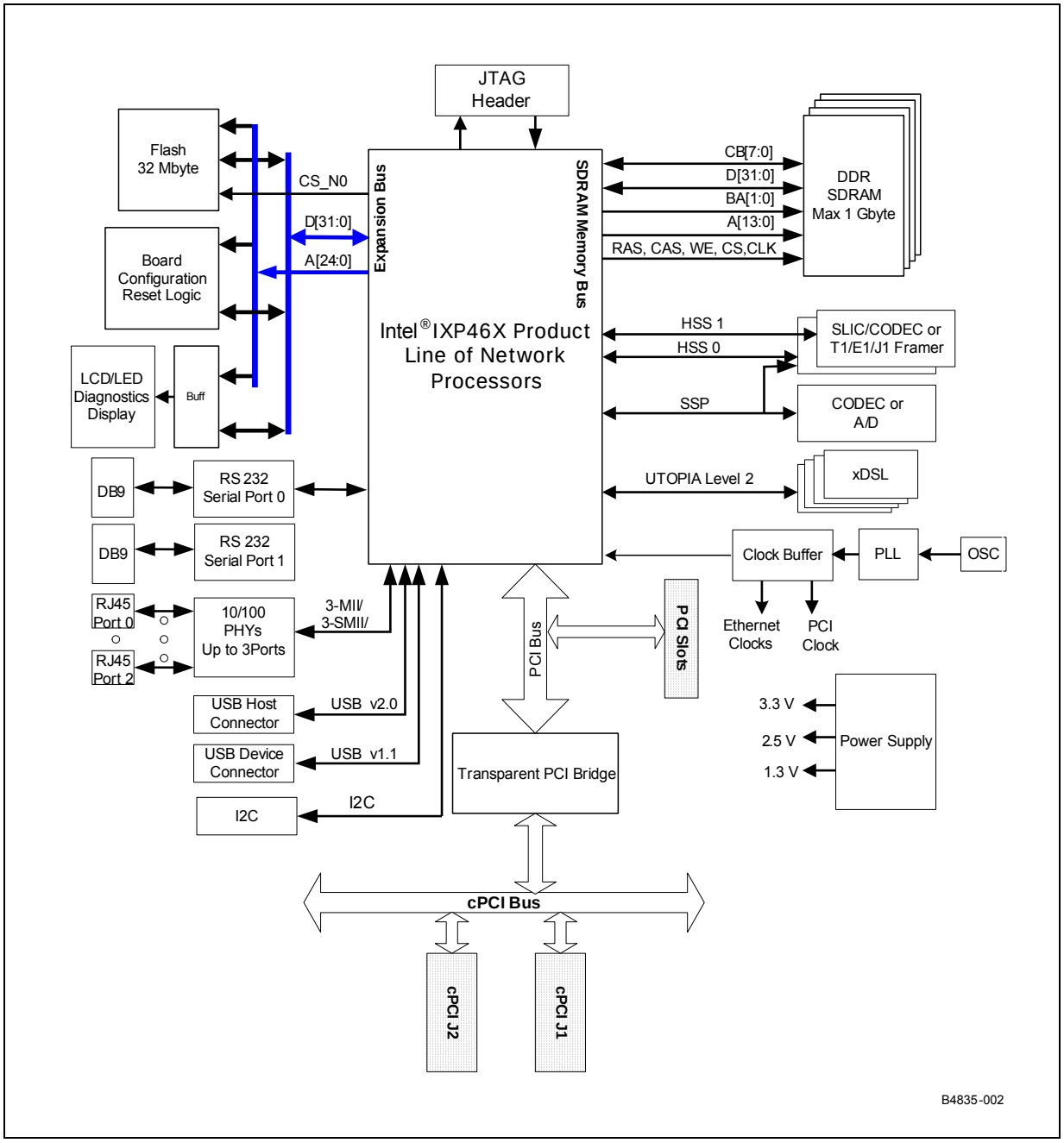
The processor is a highly integrated design, manufactured with Intel's 0.18-micron production semiconductor process technology. This process technology — along with numerous, dedicated-function peripheral interfaces and many features with the Intel XScale processor — addresses the needs of many system applications and helps reduce system costs. The processors can be configured to meet many system application and implementation needs.

Figure 2 illustrates one of many applications for which the IXP45X/IXP46X network processors can be implemented. For detailed functional descriptions, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

2.2 System Memory Map

For a complete memory map and register description of each individual module, refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Figure 2. Intel® IXP465 Example System Block Diagram



3.0 General Hardware Design Considerations

This chapter contains information for implementing and interfacing to major hardware blocks of the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. Such blocks include DDR SDRAM, Flash, SRAM, Ethernet PHYs, UART and most other peripherals interfaces. Signal definition tables list resistor recommendations for pull-ups and pull-downs.

Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected. Features enabled by a specific part number and required to be Soft Fuse-disabled, only require pull-ups or pull-downs in the ***clock-input signals.*** Other conditions may require pull-up or pull-down resistors for configuration purposes at power on or reset. Likewise, open-collector outputs must be pulled-high.

Warning: The IXP45X/IXP46X network processors' I/O pins are 3.3 V only, except for DDR SDRAM which is 2.5 V. *None of the I/Os are 5-V tolerant.*

Table 2 gives the legend for interpreting the **Type** field used in this chapter's signal-definition tables.

Table 2. Signal Type Definitions

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open-drain pin
TRI	Tri-State pin
PWR	Power pin
GND	Ground pin

3.1 Soft Fusible Features

Soft Fuse Enable/Disable is a method to enable or disable features in hardware, virtually disconnecting the hardware modules from the processor.

Some of the features offered in the IXP45X/IXP46X product line can be Soft Fuse Enabled/Disabled during boot. It is recommended that if a feature is not used in the design, the feature be Soft disabled. This helps reduce power and maintain the part running at a cooler temperature. When Soft Fuse Disabled, a pull-up resistor must be connected to each clock input pins of the disabled feature interface. All other signals can be left unconnected.

Soft Fuse Enable/Disable can be done by writing to EXP_UNIT_FUSE_RESET register, for more information refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual* and review the register description.

Table 3. Soft Fusible Features

Name	Description
PCI	The complete bus must be enabled or disable.
HSS0/1	Can only be disable as a pair.
UTOPIA	If enabling UTOPIA, MACs on NPE A are disabled. If enabling MACs on NPE A, UTOPIA are disabled.
ETHERNET	Can Enable either MII MACs or SMII MACs, but not both at the same time. Enable of MACs can be separately done per each NPE.
USB Host	Each USB can be Enable separately.
USB Device	Each USB can be Enable separately.
DDR ECC	DDR can be disabled separately form the rest of the DDR interface.

3.2 DDR-266 SDRAM Interface

The IXP45X/IXP46X network processors support unbuffered, DDR-266 SDRAM technology, capable of addressing two memory banks (one bank per CS). Each bank can be configured to support 32/64/128/256/512-Mbyte for a total combined memory support of 1 Gbyte.

The device supports non-ECC and ECC for error correction, which can be enable or disable by software as required. Banks have a bus width of 32 bits for non ECC or 40 bits for ECC enable (32-bit data + 8-bit ECC).

For a complete feature list, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

General DDR SDRAM routing guidelines can be found in Section 7.1.7, “Routing Guidelines” on page 88. For more detailed information, see the PC266 DDR SDRAM specification.

3.2.1 Signal Interface

Table 4. DDR SDRAM Interface Pin Description (Sheet 1 of 2)

Name	Input Output	Device-Pin Connection	VTT Termination	Description
DDRI_CK[2:0]	O	Connect a pair of differential clock signals to every device; When using both banks, daisy chain devices with same data bit sequence.	No	DDR SDRAM Clock Out — Provides the positive differential clocks to the external SDRAM memory subsystem.
DDRI_CK_N[2:0]	O	Same as above	No	DDR SDRAM Clock Out — Provides the negative differential clocks to the external SDRAM memory subsystem.
DDRI_CS_N[1:0]	O	Use the same CS to control 32-bit data + 8-bit ECC, per bank	Yes	Chip Select — Must be asserted for all transactions to the DDR SDRAM device. One per bank.
DDRI_RAS_N	O	The RAS signal must be connected to each device in a daisy chain manner	Yes	Row Address Strobe — Indicates that the current address on DDRI_MA[13:0] is the row.
DDRI_CAS_N	O	The CAS signal must be connected to each device in a daisy chain manner	Yes	Column Address Strobe — Indicates that the current address on DDRI_MA[13:0] is the column.

Table 4. DDR SDRAM Interface Pin Description (Sheet 2 of 2)

Name	Input Output	Device-Pin Connection	VTT Termination	Description
DDRI_WE_N	O	The WE signal must be connected to each device in a daisy chain manner	Yes	Write Strobe — Defines whether or not the current operation by the DDR SDRAM is to be a read or a write.
DDRI_DM[4:0]	O	Connect to each DM device pin. For the 8-bit devices connect one DM signal per device. For the 16-bit devices connect two DM signal per device (depending on how many data bits are being used).	Yes	Data Bus Mask — Controls the DDR SDRAM data input buffers. Asserting DDRI_WE_N causes the data on DDRI_DQ[31:0] and DDRI_CB[7:0] to be written into the DDR SDRAM devices. DDRI_DM[4:0] controls this operation on a per-byte basis. DDRI_DM[3:0] are intended to correspond to each byte of a word of data. DDRI_DM[4] is intended to be utilized for the ECC byte of data.
DDRI_BA[1:0]	O	The BA signals must be connected to each device in a daisy chain manner.	Yes	DDR SDRAM Bank Selects — Controls which of the internal DDR SDRAM banks to read or write. DDRI_BA[1:0] are used for all technology types supported.
DDRI_MA[13:0]	O	All address signals need to be connected to each device in a daisy chain manner.	Yes	Address bits 13 through 0 — Indicates the row or column to access depending on the state of DDRI_RAS_N and DDRI_CAS_N.
DDRI_DQ[31:0]	I/O	Need to be connected in parallel to achieve a 32-bit bus width.	Yes	Data Bus — 32-bit wide data bus.
DDRI_CB[7:0]	I/O	Connect to ECC memory devices.	Yes	ECC Bus — Eight-bit error correction code which accompanies the data on DDRI_DQ[31:0]. When ECC is disabled and not being used in a system design, these signals can be left un-connected.
DDRI_DQS[4:0]	I/O	Connect DQS[3:0] to devices with data signals and DQS[4] to devices with ECC signals.	Yes	Data Strobes Differential — Strobes that accompany the data to be read or written from the DDR SDRAM devices. Data is sampled on the negative and positive edges of these strobes. DDRI_DQS[3:0] are intended to correspond to each byte of a word of data. DDRI_DQS4] is intended to be utilized for the ECC byte of data.
DDRI_CKE[1:0]	O	Use one CKE per bank, never mix the CKE on the same bank. Use CKE[0] for bank0 and CKE[1] for bank1	Yes	Clock enables — One clock after DDRI_CKE[1:0] is de-asserted, data is latched on DQ[31:0] and DDRI_CB[7:0]. Burst counters within DDR SDRAM device are not incremented. De-asserting this signal places the DDR SDRAM in self-refresh mode. For normal operation, DDRI_CKE[1:0] must be asserted.
DDRI_RCVENOUT_N	O	Connect RCVEOUT to RCVENIN and follow note on pin description in this table.	No	RECEIVE ENABLE OUT must be connected to DDRI_RCVENIN_N signal of the IXP45X/ IXP46X product line and the propagation delay of the trace length must be matched to the clock trace plus the average DQ Traces.
DDRI_RCVENIN_N	I	Same as above	No	RECEIVE ENABLE IN provides delay information for enabling the input receivers and must be connected to the DDRI_RCVENOUT_N signal of the IXP45X/ IXP46X network processors.
DDRI_RCOMP	O	Tied off to a resistor	Tied off to a resistor	20 Ohm Resistor connected to ground used for process/temperature adjustments.
DDRI_VREF	I	VCCM/2	VCCM/2	DDR SDRAM Voltage Reference — is used to supply the reference voltage to the differential inputs of the memory controller pins.

3.2.2 DDR SDRAM Memory Interface

The IXP45X/IXP46X network processors support compatible DDR-266 SDRAM, 8- and 16-bit wide devices, with a total bus width of 32 bits. Only 32-bit-wide accesses are supported.

The maximum supported memory is 1 Gbyte, configured by enabling both physical banks of DDR-266 SDRAM devices. Each bank can be composed of four 1-Gbit (32 Mbit X 8 X 4) devices and use one chip-selects per bank. The minimum supported memory is 32 Mbyte, configured by enabling a single physical bank of DDR-266 SDRAM devices. The bank would consist of two 128-Mbit (2 Mbit X 16 X 4) devices and using a single chip-select.

All supported memory configurations are listed in Table 28 on page 78. Remember that these are all non-buffer devices, as the IXP45X/IXP46X network processors only support non-buffer memory devices.

For a complete description on how the IXP45X/IXP46X network processors interface to DDR SDRAM, see Chapter 7.0, “DDR-SDRAM”.

3.2.3 DDR SDRAM Initialization

For instructions on DDR SDRAM initialization, refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual* and its section titled “DDR SDRAM Initialization.”

3.3 Expansion Bus

The Expansion Bus of the IXP45X/IXP46X network processors is specifically designed for compatibility with Intel- and Motorola*-style microprocessor interfaces and Texas Instruments* DSP standard Host-Port Interfaces* (HPI).

The expansion bus controller includes a 25-bit address bus and a 32-bit wide data path, running at a maximum speed of 80 MHz from an external clock oscillator. The bus can be configure to support the following target devices:

- Intel multiplexed
- Intel StrataFlash®
- Micron* Flow-Through ZBT
- Motorola non multiplexed
- Intel non-multiplexed
- Synchronous Intel StrataFlash® Memory
- Motorola multiplexed
- Texas Instruments* Host Port Interface (HPI)

The expansion bus controller also has an arbiter that supports up to four external devices that can master the expansion bus. External masters can be used to access external slave devices that reside on the expansion bus, including access to internal memory mapped regions within the IXP45X/IXP46X network processors.

All supported modes are seamless and no additional glue logic is required. Other cycle types may be supported by configuring the Timing and Control Register for Chip Select.

Applications having less than 32 data bits may connect to less than the full 32 bits. Devices with wider than 32-bit data bus are not supported. A total of eight chip selects are supported with an address space of up to 32 Mbytes per chip select.

3.3.1 Signal Interface

Table 5. Expansion Bus Signal Recommendations

Name	Input Output	Pull Up Down	Recommendations
EX_CLK	I	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_ALE	TRI O	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_ADDR[24:0]	I/O	Yes	Use 4.7-KΩ resistors for pull-downs; required for boot strapping for initial configuration of Configuration Register 0. Pull-ups are not required as for when the system comes out of reset, all bits are initially set HIGH. For more details, see Table 6. For additional details on address strapping, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.
EX_WR_N	I/O	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_RD_N	I/O	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_CS_N[7:0]	I/O	Yes	Use series termination resistor, 10Ω to 33Ω at the source. Use 10KΩ resistors pull-ups to ensure that the signal remains de-asserted.
EX_DATA[31:0]	I/O	No	
EX_BE_N[3:0]	I/O	No	
EX_IOWAIT_N	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_RDY_N[3:0]	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_PARITY[3:0]	I/O	No	
EX_REQ_N[3:1]	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_REQ_GNT_N	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_GNT_N[3:1]	O	No	
EX_GNT_REQ_N	O	No	
EX_SLAVE_CS_N	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_BURST	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.
EX_WAIT_N	TRI O	No	

3.3.2 Reset Configuration Straps

At power up or whenever RESET_IN_N is asserted, the Expansion-bus address outputs are switched to inputs and the state of the inputs are captured and stored in Configuration Register 0, bits 24 through 0. This occurs when PLL_LOCKED is de-asserted.

The strapping of Expansion-bus address pins can be done by placing external pull-down resistors at the required address pin. It is not required to use external pull-up resistors, by default upon reset all bits on Configuration Register 0 are set High, unless an external pull down is used to set them Low. For example to register a bit low or high in the Configuration Register 0, do the following:

Place an external 4.7-KΩ pull-down resistor to set a bit LOW.

No external pull-up is required, by default upon reset, bits are set HIGH.

The state of the boot-strapping resistor is register on the first cycle after the synchronous de-assertion of the reset signal. These bits can be read or written as needed for desired configurations. It is recommended that only Bit 31, Memory Map, be changed from 1 to 0 after execution of boot code from external flash.

For a complete bit description of Configuration Register 0, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Table 6. Boot/Reset Strapping Configuration (Sheet 1 of 2)

Name	Function	Description
EX_ADDR[24]	(Reserved)	(Reserved)
EX_ADDR[23:21]	Intel XScale® Processor Clock Set[2:0]	Allows changing Intel XScale® Processor clock speed. This overrides device fuse settings. However cannot be used to over-clock core speed.
EX_ADDR[20:17]	Customer	Customer-defined bits. (Might be used for board revision.)
EX_ADDR[16:11]	(Reserved)	(Reserved)
EX_ADDR[10]	IOWAIT_CS0	1 = EX_IOWAIT_N is sampled during the read/write expansion bus cycles for Chip Select 0. 0 = EX_IOWAIT_N is ignored for read and write cycles to Chip select 0 if EXP_TIMING_CS0 is configured to Intel mode. Typically, IOWAIT_CS0 must be pulled down to Vss when attaching a Synchronous Intel StrataFlash® on Chip Select 0 since the default mode for EXP_TIMING_CS0 is Intel mode and EX_IOWAIT_N is an unknown value for Synchronous Intel StrataFlash. If the board does not connect the Synchronous Intel StrataFlash WAIT pin to EX_WAIT_N (and the board guarantees EX_IOWAIT_N is pulled up), the value of IOWAIT_CS0 is a don't-care, since EX_IOWAIT_N will not be asserted. When EXP_TIMING_CS0 is reconfigure to Intel Synchronous mode during boot-up (for synchronous Intel chips), the expansion bus controller ignores EX_IOWAIT_N during read and write cycles since the WAIT functionality is determined from the EXP_SYNCINTEL_COUNT and EXP_TIMING_CS registers.
EX_ADDR[9]	EXP_MEM_DRIVE	Refer to table found in EX_ADDR[5].
EX_ADDR[8]	USB Clock	Controls the USB clock select. 1 = USB Host/Device clock is generated internally 0 = USB Device clock is generated from GPIO[0]. USB Host clock is generated from GPIO[1]. When generating a spread spectrum clock on OSC_IN, GPIO[0] can be driven from the system board to generate a 48-MHz clock for the USB Device and GPIO[1] can be driven from the system board to generate a 60-MHz clock for the USB Host.
EX_ADDR[7]	32_FLASH	Refer to table found in EX_ADDR[0]
EX_ADDR[6]	EXP_ARB	Configures the Expansion bus arbiter. 0 = External arbiter for Expansion bus. 1 = Expansion bus controller arbiter enabled
EX_ADDR[5]	EXP_DRIVE	Expansion bus low/medium/high drive strength. The drive strength depends on EXP_DRIVE and EXP_MEM_DRIVE configuration bits. B9. B5 --- 0 . . 0 Reserved 0 . . 1 Medium Drive 1 . . 0 Low Drive 1 . . 1 High Drive
EX_ADDR[4]	PCI_CLK	Sets the clock speed of the PCI Interface 0 = 33 MHz 1 = 66 MHz
EX_ADDR[3]	(Reserved)	(Reserved). EX_ADDR[3] must not be pulled down during address strapping.

Table 6. Boot/Reset Strapping Configuration (Sheet 2 of 2)

Name	Function	Description
EX_ADDR[2]	PCI_ARB	Enables the PCI Controller Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled
EX_ADDR[1]	PCI_HOST	Configures the PCI Controller as PCI Bus Host 0 = PCI as non-host 1 = PCI as host
EX_ADDR[0]	8/16_FLASH	Specifies the data bus width of the FLASH memory device found on Chip Select 0. The data bus is based upon bits 0 and 7 of **Configuration Register 0**. 32_FLASH 8/16_FLASH Data bus size B7 . B0 --- 0 . . 0 16-bit 0 . . 1 8-bit 1 . . 0 (Reserved) 1 . . 1 32-bit

3.3.3 8-Bit Device Interface

The IXP45X/IXP46X network processors support 8-bit-wide data bus devices (byte mode). For Intel interface cycles, the data lines and control signals can be connected as shown in Figure 3 on page 25 and Figure 4 on page 26. During byte mode accesses, the remaining data signals not being used EX_DATA[31:8], are driven by the processor to an unpredictable state on WRITE cycles and tri-stated during READ cycles.

When booting an 8-bit flash device, the expansion bus must be configured during reset to the 8-bit mode (see Configuration Register 0). To accomplish this, boot-strapping is required in certain address pins of the Expansion bus. For example, as in this case when booting of an 8-bit flash device, bit 0 and 7 of Configuration Register 0 must be set as follows:

Bit 0 = 1. By default this bit is set high when coming off reset or any time reset is asserted.

Bit 7 = 0. This can be done by placing an external 4.7-KΩ pull-down resistor to pin EX_ADDR[7].

If it is required to change access mode, after the system has booted, and during normal operation; the Timing and Control Register for Chip Select must be configured to perform the desired mode access. For a complete description on accomplishing this refer to the “Expansion Bus” chapter in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*.

3.3.4 16-Bit Device Interface

The IXP45X/IXP46X network processors support 16-bit wide data bus devices (16-bit word mode). For Intel interface cycles, the data lines and control signals can be connected as shown in Figure 3 on page 25 and Figure 4 on page 26. During word mode accesses, the remaining data signals not being used EX_DATA[31:16], are driven by the processor to an unpredictable state on WRITE cycles and tri-stated during READ cycles.

When booting a 16-bit flash device, the expansion bus must be configured during reset to the 16-bit mode (see Configuration Register 0). To accomplish this, boot-strapping is required in certain address pins of the Expansion bus.

For example, as in this case when booting of a 16-bit flash device, bit 0 and 7 of Configuration Register 0 must be set as follows:

- Bit 0 = 0.
  This can be done by placing an external 4.7-KΩ pull-down resistor to pin EX_ADDR[0].
- Bit 7 = 0.
  This can be done by placing an external 4.7-KΩ pull-down resistor to pin EX_ADDR[7].

If it is required to change access mode, after the system has booted, and during normal operation; the Timing and Control Register for Chip Select must be configured to perform the desired mode access. For a complete description on accomplishing this refer to the “Expansion Bus” chapter in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*.

3.3.5 32-Bit Device Interface

The IXP45X/IXP46X network processors support 32-bit wide data bus devices (32-bit word mode). For Intel interface cycles, the data lines and control signals can be connected as shown in Figure 3 on page 25 and Figure 4 on page 26.

When booting a 32-bit flash device, the expansion bus must be configured during reset to the 32-bit mode (see Configuration Register 0). To accomplish this, boot-strapping is required in certain address pins of the Expansion bus. For example, as in this case when booting of a 32-bit flash device, bit 0 and 7 of Configuration Register 0 must be set as follows:

- Bit 0 = 1.
  By default this bit is set high when coming off reset or any time reset is asserted.
- Bit 7 = 1.
  By default this bit is set high when coming off reset or any time reset is asserted.

If it is required to change access mode, after the system has booted, and during normal operation; the Timing and Control Register for Chip Select must be configured to perform the desired mode access. For a complete description on accomplishing this refer to the “Expansion Bus” chapter in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*.

Figure 3. 8/16/32-Bit Device Interface: No Byte-Enable

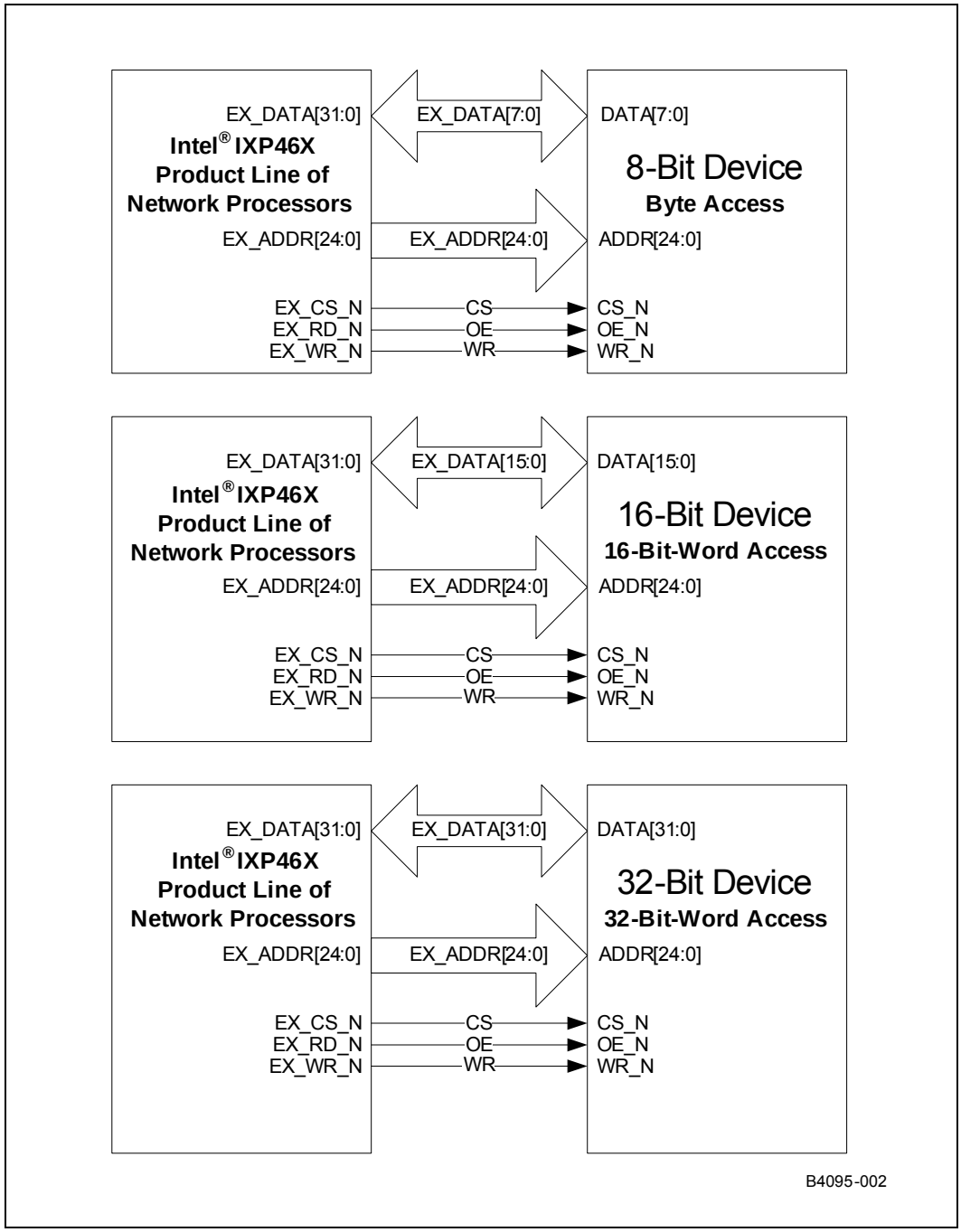
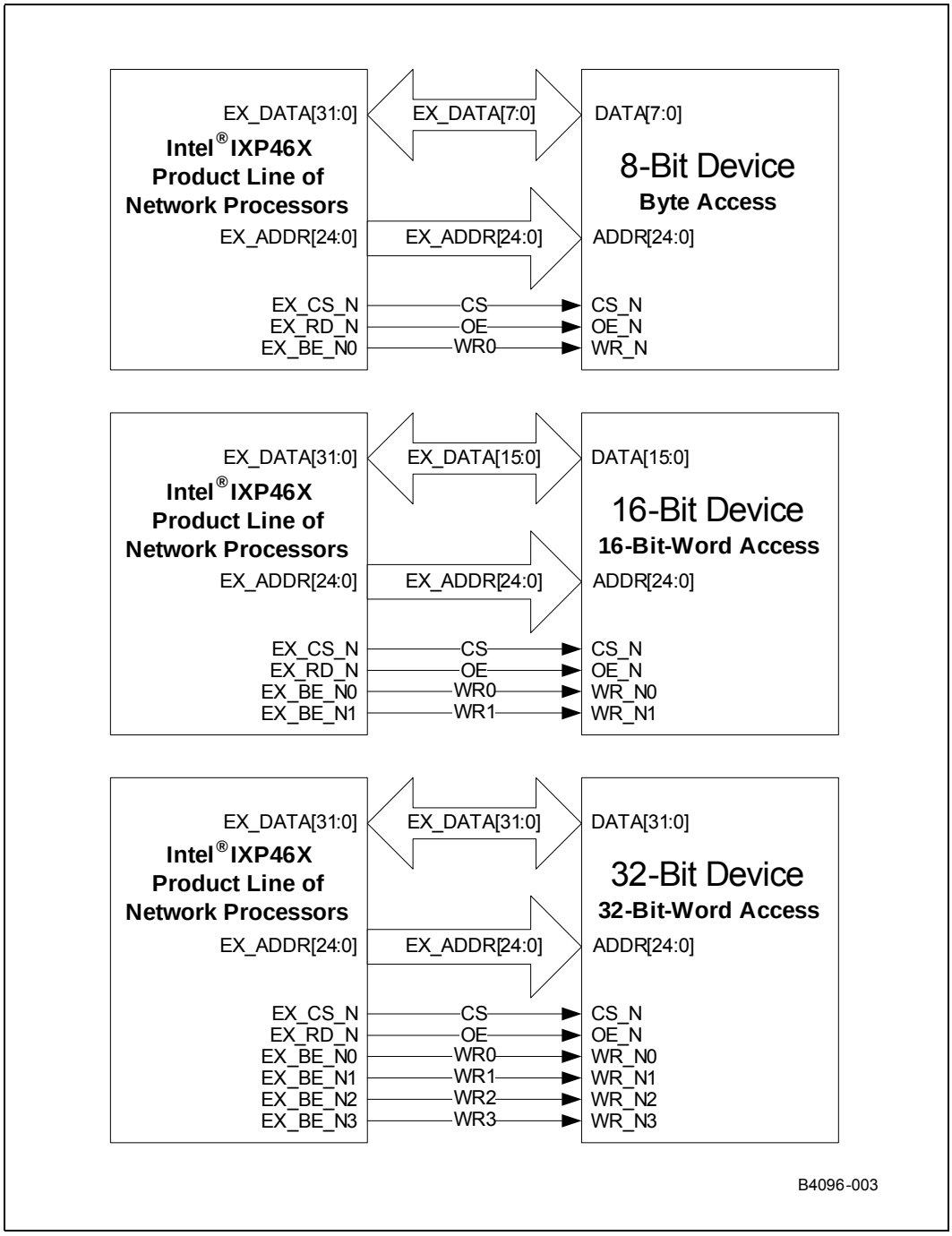


Figure 4. 8/16/32-Bit Device Interface: Byte Enable



3.3.6 Flash Interface

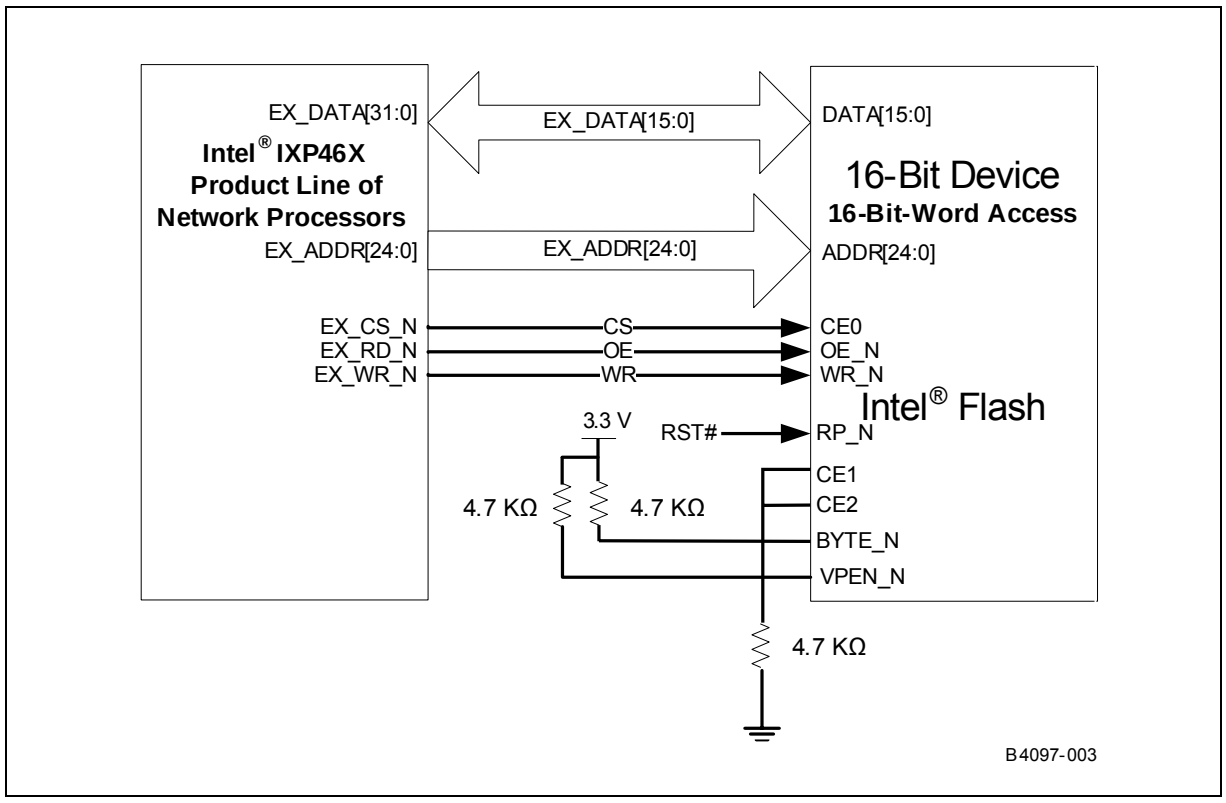
Figure 5 illustrates how a boot ROM is connected to the expansion bus. The flash (ROM) used in the block diagram is the Intel StrataFlash® memory device TE28F256J3D — 32-Mbyte, 16-bit, flash in the 56-TSOP package. The Intel StrataFlash memory TE28F256J3D is part of the 0.13-micron, 3.3-V Intel StrataFlash memory.

The E28F256J3D supports common flash interface (CFI). For information on migrating from J3 to J3D Intel StrataFlash memory, see the *Intel StrataFlash® Memory J3 to Intel® Embedded Flash Memory (J3 v.D) Conversion Guide - Application Note 835* (document 308555).

For information on migrating from J3 to P30 Intel StrataFlash memory, see the *Migration Guide for Intel StrataFlash® Memory (J3) to Intel StrataFlash® Embedded Memory (P30 and P33) - Application Note 835* (document 308555).

The example in Figure 5 shows a 16-bit flash memory device connected to the IXP45X/ IXP46X network processors. Boot-strapping is required in the address bus, both EX_ADDR[0] and EX_ADDR[7] need external, 4.7-KΩ pull-down resistors (not shown on diagram). The pull-down resistors sets Bits 0 and 7 low in the Configuration Register 0. This in turn sets the processor into a 16-bit-mode access.

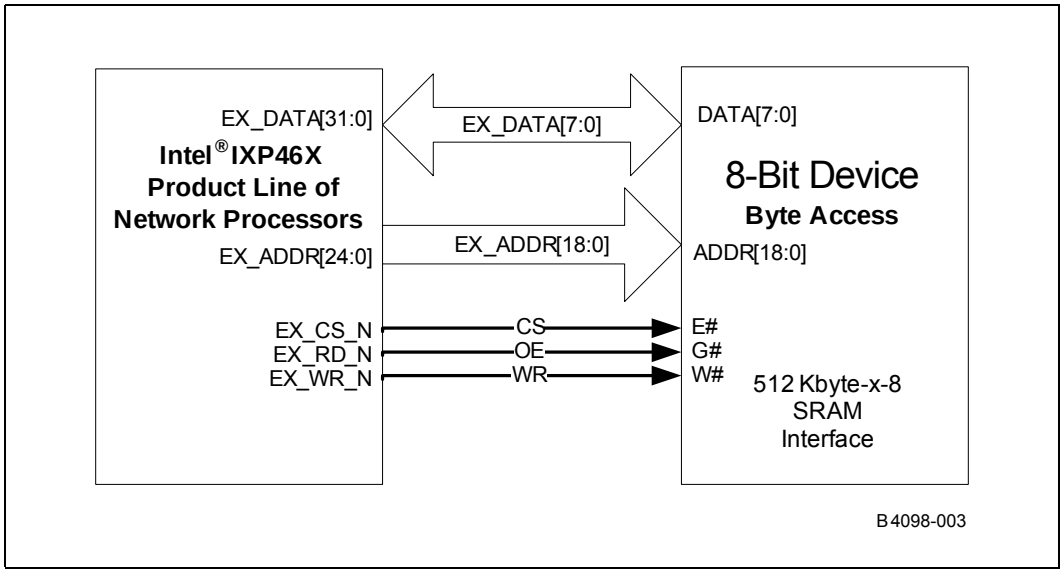
Figure 5. Flash Interface Example



3.3.7 SRAM Interface

A typical connection between an 8-bit SRAM memory device and the IXP45X/IXP46X network processors expansion bus is shown in Figure 6 on page 28. When attempting to communicate to this device, the Timing and Control Register for Chip Select must be configured for proper access. For more information, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Figure 6. Expansion Bus SRAM Interface



3.3.8 Design Notes

Care must be taken when loading the bus with too many devices. As more devices are added, the loading capacity adds up — to the point where timing can become critical.

To account for this, timing on the expansion bus may be adjusted in the Timing and Control Register for Chip Select. If an edge rises slowly due to low drive strength, the processors should wait an extra cycle before the value is read. For more information, see the documentation on Timing and Control Register for Chip Select bits [29:16] in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

3.4 UART Interface

The IXP45X/IXP46X network processors provide two dedicated, Universal Asynchronous Receiver/Transmitter Serial Ports (UARTs). These are high-speed UARTs, capable of supporting baud rates from 1,200 Baud to 921.6 KBaud.

The hardware supports a four-wire interface:

- Transmit Data
- Receive Data
- Request to Send
- Clear to Send

Note: The UART module does not support full modem functionality. However, this can be implemented, by using GPIO ports to generate DTR, DSR, RI, and DCD and making some changes to the driver.

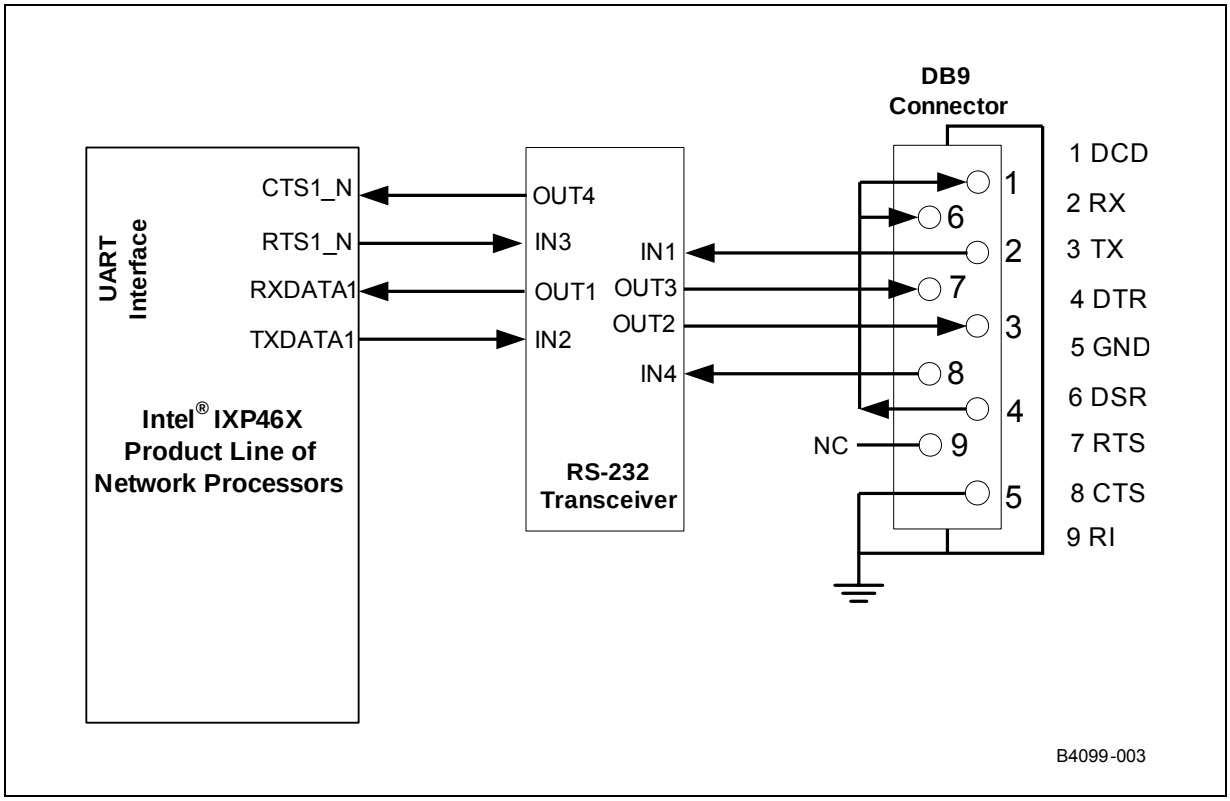
3.4.1 Signal Interface

Table 7. UART Signal Recommendations

Name	Input Output	Pull Up Down	Recommendations
RXDATA0	I	Yes	Serial data input Port 0. When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
TXDATA0	O	No	Serial data output Port 0.
CTS0_N	I	Yes	Clear-To-Send Port 0. \When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
RTS0_N	O	No	Request-To-Send Port 0.
RXDATA1	I	Yes	Serial data input Port 1. When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
TXDATA1	O	No	Serial data output Port 1.
CTS1_N	I	Yes	Clear-To-Send Port 1. When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
RTS1_N	O	No	Request-To-Send Port 1.

The following figure contain a typical four signal interface between the UART and an RS-232 transceiver driver, required to interface with external devices. Unused inputs to the RS-232 driver can be connected to ground. This avoids signals floating to undetermined states which can cause over heating of the driver leading to permanent damage.

Figure 7. UART Interface Example



3.5 MII/SMII Interface

The IXP45X/IXP46X network processors support a maximum of three Ethernet MACs. Depending on the IXP45X/IXP46X network processors part number used, various combinations can be used. For the various features that can be enable a variety of needs, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

All MACs contained in the NPEs are compliant to the IEEE 802.3 specification and handle flow control for the IEEE 802.3Q VLAN specification.

The Management Data Interface (MDI) supports a maximum of 32 PHY addresses. MDI signals are required to be connected to every PHY chip. Each PHY port is assign a unique address in the external PHY chip from 0 to 31, totaling a maximum of 32 PHY addresses. The maximum number of MACs supported by the IXP45X/IXP46X network processors is three.

The MII interface supports clock rates of 25 MHz for 100-Mbps operation or 2.5 MHz for 10-Mbps operation.

SMII interface supports clock rate of 125 MHz for 10/100-Mbps operation.

General PHY Ethernet devices routing guidelines can be found in Section 5.2.3, “SMII Signal Considerations” on page 67. For more detailed information, see the IEEE 802.3 specification.

3.5.1 Signal Interface MII

Table 8. MII NPE A Signal Recommendations

Name	Input/ Output	Pull Up Down	Recommendations
ETHA_TXCLK	I	Yes	Transmit Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_TXDATA[3:0]	O	No	Transmit Data.
ETHA_TXEN	O	No	Transmit Enable.
ETHA_RXCLK	I	Yes	Receive Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_RXDATA[3:0]	I	Yes	Receive Data. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_RXDV	I	Yes	Receive Data Valid. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_COL	I	Yes	Collision Detect. If operating in a full duplex mode and there is no requirement to use the Collision Detect signal, then the pin must be pulled low with a 10-KΩ resistor.
ETHA_CRS	I	Yes	Carrier Sense. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

Table 9. MII NPE B Signal Recommendations (Sheet 1 of 2)

Name	Input/ Output	Pull Up/ Down	Recommendations
ETHB_TXCLK	I	Yes	Transmit Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHB_TXDATA[3:0]	O	No	Transmit Data.
ETHB_TXEN	O	No	Transmit Enable.
ETHB_RXCLK	I	Yes	Receive Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHB_RXDATA[3:0]	I	Yes	Receive Data. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHB_RXDV	I	Yes	Receive Data Valid. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Table 9. MII NPE B Signal Recommendations (Sheet 2 of 2)

Name	Input/ Output	Pull Up/ Down	Recommendations
ETHB_COL	I	Yes	Collision Detect. If operating in a full duplex mode and there is no requirement to use the Collision Detect signal, then the pin must be pulled low with a 10-KΩ resistor.
ETHB_CRS	I	Yes	Carrier Sense. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals***.

Table 10. MII NPE C Signal Recommendations

Name	Input/ Output	Pull Up/ Down	Recommendations
ETHC_TXCLK	I	Yes	Transmit Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_TXDATA[3:0]	O	No	Transmit Data.
ETHC_TXEN	O	No	Transmit Enable.
ETHC_RXCLK	I	Yes	Receive Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_RXDATA[3:0]	I	Yes	Receive Data. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_RXDV	I	Yes	Receive Data Valid. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_COL	I	Yes	Collision Detect. If operating in a full duplex mode and there is no requirement to use the Collision Detect signal, then the pin must be pulled low with a 10-KΩ resistor.
ETHC_CRS	I	Yes	Carrier Sense. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in note 1 — only require pull-ups or pull-downs in the ***clock-input signals***.

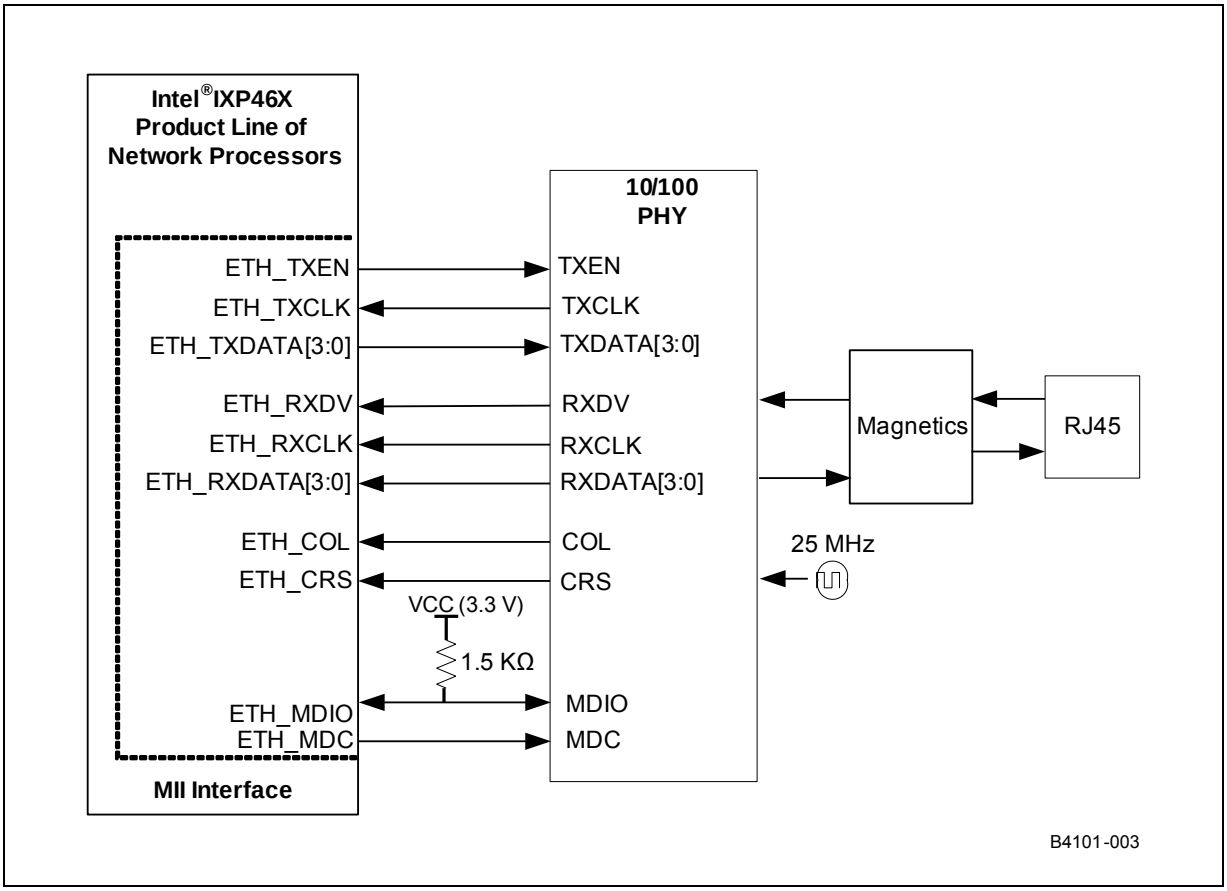
Table 11. MAC Management Signal Recommendations NPE A,B,C

Name	Input/ Output	Pull Up/ Down	Recommendations
ETH_mdio	I/O	Yes	NPE A,B,C Management data output. An external pull-up resistor of 1.5 KΩ is required on ETH_MDIO to properly quantify the external PHYs used in the system. For specific implementation, see the IEEE 802.3 specification. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETH_mdc	I/O	No	NPE A,B,C Management data clock.

3.5.2 Device Connection, MII

Figure 8 is a typical example of an Ethernet PHY device interfacing to one of the MACs via the MII hardware protocol.

Figure 8. MII Interface Example



3.5.3 Signal Interface, SMII

Serial Media Independent Interface (SMII) is a hardware feature to convey complete MII interface between a MAC and 10/100 PHY interface with two data pins per port and one synchronizing signal for multi PHYs.

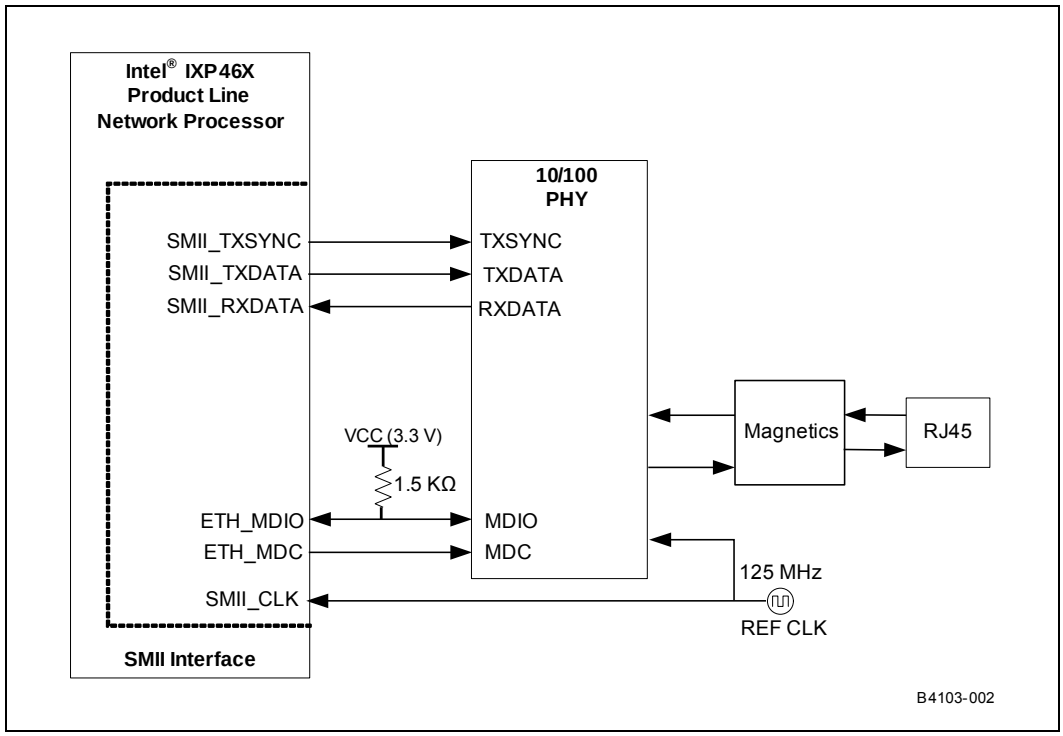
Table 12. SMII Signal Recommendations: NPE A, B, C

Name	Input/ Output	Pull Up/ Down	Recommendations
SMII_TXDATA[4]	O	No	NPE A Transmit Data Port 4.
SMII_RXDATA[4]	I	Yes	NPE A Received Data Port 4. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
SMII_CLK	I	Yes	NPE A,B,C Reference Clock, 125-MHz. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
SMII_TXDATA[0] / SMII_TXDATA[1] / SMII_TXDATA[2] / SMII_TXDATA[3]	O	No	NPE B Transmit Data Ports 3,2,1,0.
SMII_RXDATA[0] / SMII_RXDATA[1] / SMII_RXDATA[2] / SMII_RXDATA[3]	I	Yes	NPE B Transmit Data Ports 3,2,1,0. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. One special configuration exists for the board designer. When NPE B is configured in SMII mode of operation and a subset of the four SMII ports are utilized (i.e. All four are enabled but only two are being connected). The unused inputs must be tied high with a 10-KΩ resistor.
SMII_SYNC	O	No	NPE B Synchronous pulse.
ETH_MDIO	I/O	Yes	NPE A,B,C Management data output. An external pull-up resistor of 1.5 KΩ is required on ETH_MDIO to properly quantify the external PHYs used in the system. For specific implementation, see the IEEE 802.3 specification. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETH_MDC	I/O	No	NPE A,B,C Management data clock.
SMII_TXDATA[5]	O	No	NPE C Transmit Data Ports 5.
SMII_RXDATA[5]	I	Yes	NPE C Receive Data Ports 5. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

3.5.4 Device Connection, SMII

Figure 9. SMII Interface Example



3.6 GPIO Interface

The IXP45X/IXP46X network processors provide 16 general-purpose input/output pins for use in generating and capturing application specific input and output signals. Each individual pin can be programmed as either an input or output.

When programmed as an input, GPIO0 through GPIO12 can be configured to be an interrupt source. Interrupt sources can be configured to detect either active high, active low, rising edge, falling edge, or transitional. In addition, GPIO14 and GPIO15 can be programmed to provide a user-programmable clock out.

During reset, all pins are configured as inputs and remain in this state until configured otherwise, with the exception of GPIO15, which by default provides a clock output. The driver strength of GPIO pins is sufficient to drive external LEDs with a proper limiting resistor.

3.6.1 Signal Interface

Table 13. GPIO Signal Recommendations

Name	Input/ Output	Pull Up/ Down	Recommendations
GPIO[12:0]	I/O	Yes	General Purpose Input/Output. If used as an input interrupt, should be pull-up or pull-down, depending on the level of activation. For example: Active high, use a 10-KΩ pull-down resistor. Active low, use a 10-KΩ pull-up resistor. Should be pulled high through a 10-KΩ resistor when *not* used.
GPIO[13]	I/O	Yes	General Purpose Input/Output. Same recommendations as GPIO[12:0]
GPIO[14]	I/O	Yes	General Purpose Input/Output. Same recommendations as GPIO[12:0]. An additional feature includes Clock generation, max clock out 33.33 MHz., set as input by default.
GPIO[15]	I/O	Yes	General Purpose Input/Output. Same recommendations as GPIO[12:0]. An additional feature includes Clock generation, max clock out 33.33 MHz., set as output by default.

3.6.2 Design Notes

The drive strength for GPIO[15:14] is limited to 8 mA, while GPIO [13:0] can output up to 16 mA. When used for driving high current devices such as LEDs or relays, make sure to place current-limiting resistor or permanent damage to the IXP45X/IXP46X network processors driver might be done.

It is recommended that a 10-KΩ pull-up resistor be used when a GPIO port is configured as an input and not being used.

3.7 I²C Interface

The IXP45X/IXP46X network processors support I²C interface and protocol. The hardware-embedded block supports transfer rates in Standard-mode at up to 100 Kbps or Fast-mode at up to 400 Kbps, 7-bit addressing, and Master or Slave mode.

Note: The I2C block does not support 10-bit addressing mode.

Figure 10 shows the schematic for connecting the I²C interface to a 256-byte I²C EEPROM, 7-bit addressing mode (Philips* PC8582C-2T/03).

3.7.1 Signal Interface

Table 14. I2C Signal Recommendations

Name	Input Output	Pull Up Down	Recommendations
I2C_SCL	I/O	Yes	Serial Data. Use a 4.7-KΩ pull-up resistor.
I2C_SDA	I/O	Yes	Serial Clock. Use a 4.7-KΩ pull-up resistor.

3.7.2 Device Connection

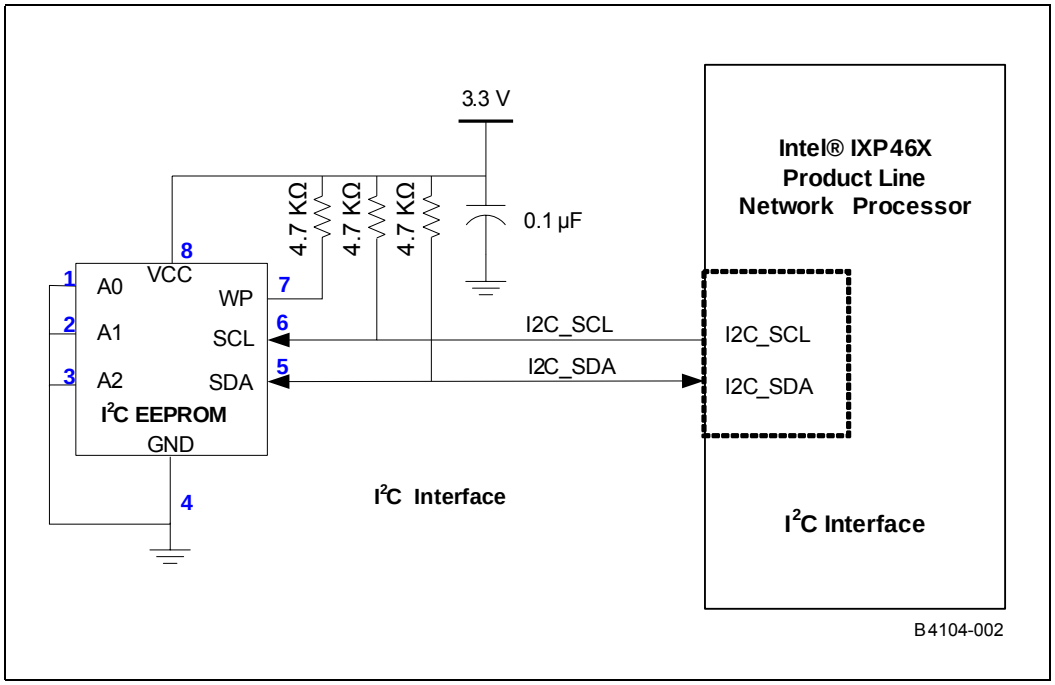
More information is available from the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet* and the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Note: Because of the characteristics of the I2C bus (Open Drain/Collector) pull-up resistors are required. Use 2 KΩ to 10 KΩ. resistors.

The *I²C-Bus Specification*, available from Philips Semiconductors*, states:

The external pull-up resistor connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit. The actual value of the pull-up is system dependent and a guide is presented in the *I²C-Bus Specification* on determining the maximum and minimum resistors to use when the system is intended for standard or fast-mode I²C bus devices.

Figure 10. I²C EEPROM Interface Example



3.8 USB Interface

There are two USB controllers in the IXP45X/IXP46X network processors — one is a Host controller and the other a Device controller.

The Host controller is a USB v2.0 module. It supports Low-Speed, 1.5 Mbps and Full-Speed, 12 Mbps, however, it does not support the High-Speed, 480 Mbps rate.

The Device controller supports USB v1.1 module. It supports most standard device requests issued by any USB host controller. It is an USB device-only controller. The interface supports Low-Speed, 1.5 Mbps and Full-Speed, 12 Mbps.

There are:

- Six isochronous endpoints (three input and three output)
- One control endpoint
- Three interrupt endpoints
- Six bulk endpoints (three input and three output)

General USB routing guidelines can be found in Section 5.2.5, “USB Considerations” on page 67. For more detailed information, see the *Universal Serial Bus Specification*, Revision 1.1.

3.8.1 Signal Interface

Table 15. USB Host/Device Signal Recommendations

Name	Input/ Output	Pull Up/ Down	Recommendations
USB_DPOS	I/O	Yes	Positive signal of the differential USB receiver/driver for the USB device interface. Use an 18Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor.
USB_DNEG	I/O	Yes	Negative signal of the differential USB receiver/driver for the USB device interface. Use an 18Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor.
USB_HPOS	I/O	Yes	Positive signal of the differential USB receiver/driver for the USB host interface. Use a 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor.
USB_HNEG	I/O	Yes	Negative signal of the differential USB receiver/driver for the USB host interface. Use a 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor.
USB_HPEN	O	No	Enable to the external VBUS power source
USB_HPWR	I	Yes	External VBUS power. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only required pull-ups or pull-downs in the ***clock-input signals*.**

A typical implementation of a USB interface Host down-stream is shown in Figure 11. The Host controller can not be used as a Device controller; however there is a second USB module with a Device controller capability that can be implementation for this application as shown in Figure 12. Note that depending on the data rate required, Low-speed or Full-speed, the 1.5K resistor shown near the device interface must be connected, either on the D+ or D-.

Speed configuration at the Device can be set as stated in note 1 and 2 bellow. For more details, refer to the *Universal Serial Bus Specification*, Revision 1.1.

Note:

1. If a 1.5-KΩ, pull-up resistor is connected to USB_DPOS line, the USB port is identified as Full-speed (12 Mbps).
2. If a 1.5-KΩ, pull-up resistor is connected to USB_DNEG line, the USB port is identified as Low-speed (1.5 Mbps).
3. The processors' USB drivers are CMOS. They require series termination resistors on both signals of the differential pair USB_DPOS and USB_DNEG. The value of the series resistor depends upon the variation of the driver's impedance.

To maintain signal integrity and minimize end-users termination mismatch, the IXP45X/IXP46X network processors require external series termination resistors. The value of terminating resistors is based on the operational speed and length of the transmission line. It is recommended to start with a 18-Ω resistor and adjust the value if required.

Note: In Figure 11, the series termination for the Host port is 20 Ω, however, Figure 12 recommends using 18 Ω for the Device port.

3.8.2 Device Connection

Figure 11. USB Host Down Stream Interface Example

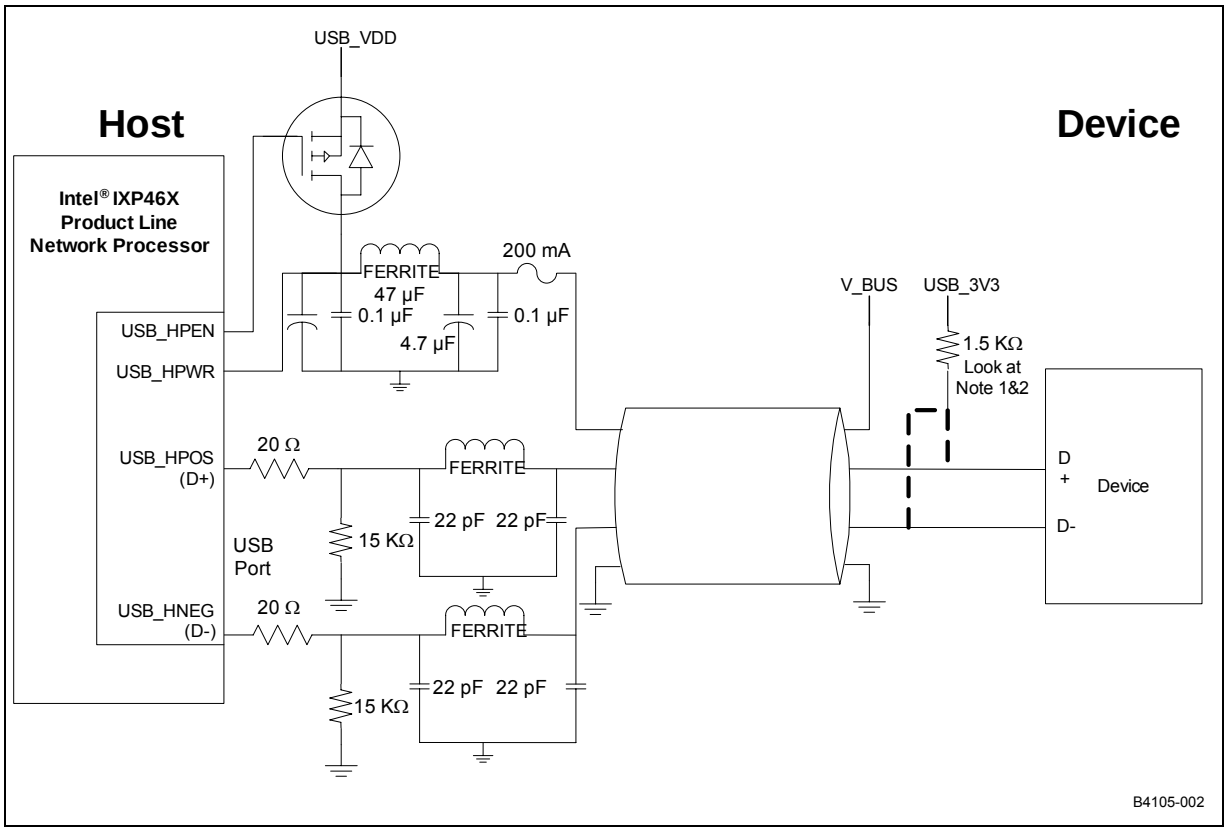
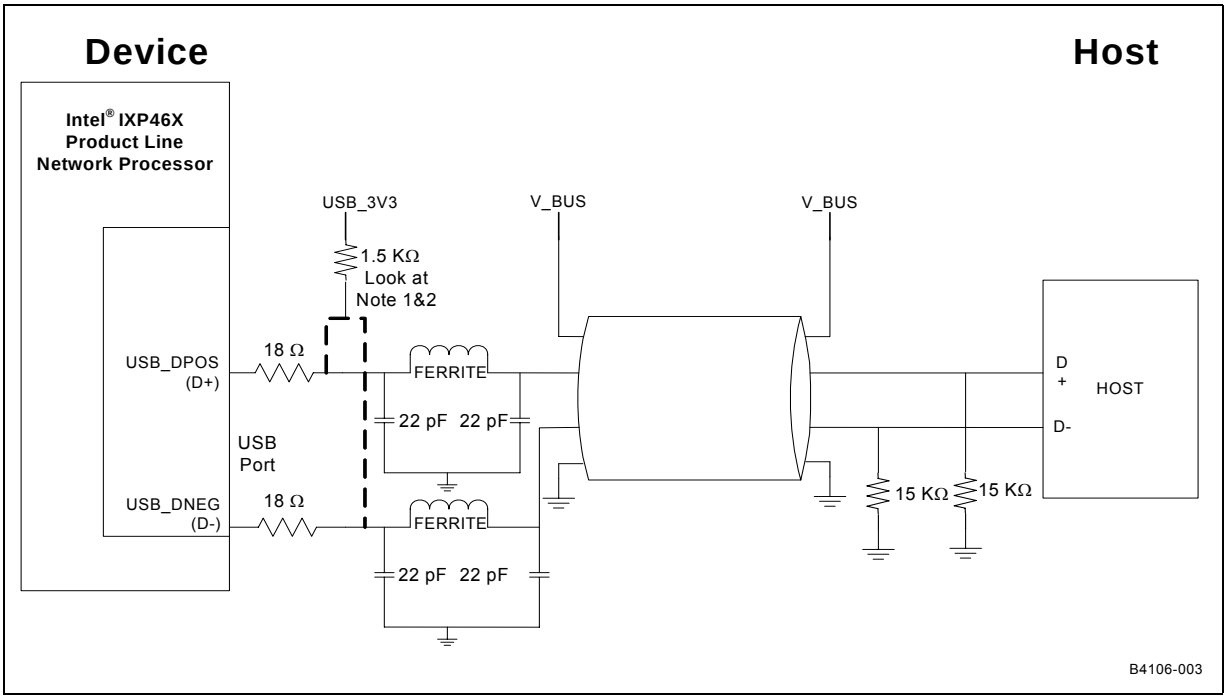


Figure 12. USB Device Interface Example



3.9 UTOPIA Level 2 Interface

The IXP45X/IXP46X network processors support the industry-standard UTOPIA Level 2 bus interface. A dedicated Network Processor Engine (NPE) handles segmentation and reassembly of ATM cells, CRC checking/generation, and transfer of data to/from memory. This allows parallel processing of data traffic on the UTOPIA interface, off-loading processor overhead required by the Intel XScale processor.

The UTOPIA module is configured as a master and can support single-PHY (SPHY) or multi-PHY (MPHY).

The IXP45X/IXP46X network processors are in compliance with the ATM Forum, *UTOPIA Level 2 Specification*, Revision 1.0. For optimal design results, the guidelines of the specification should be followed.

3.9.1 Signal Interface

Table 16. UTOPIA Signal Recommendations

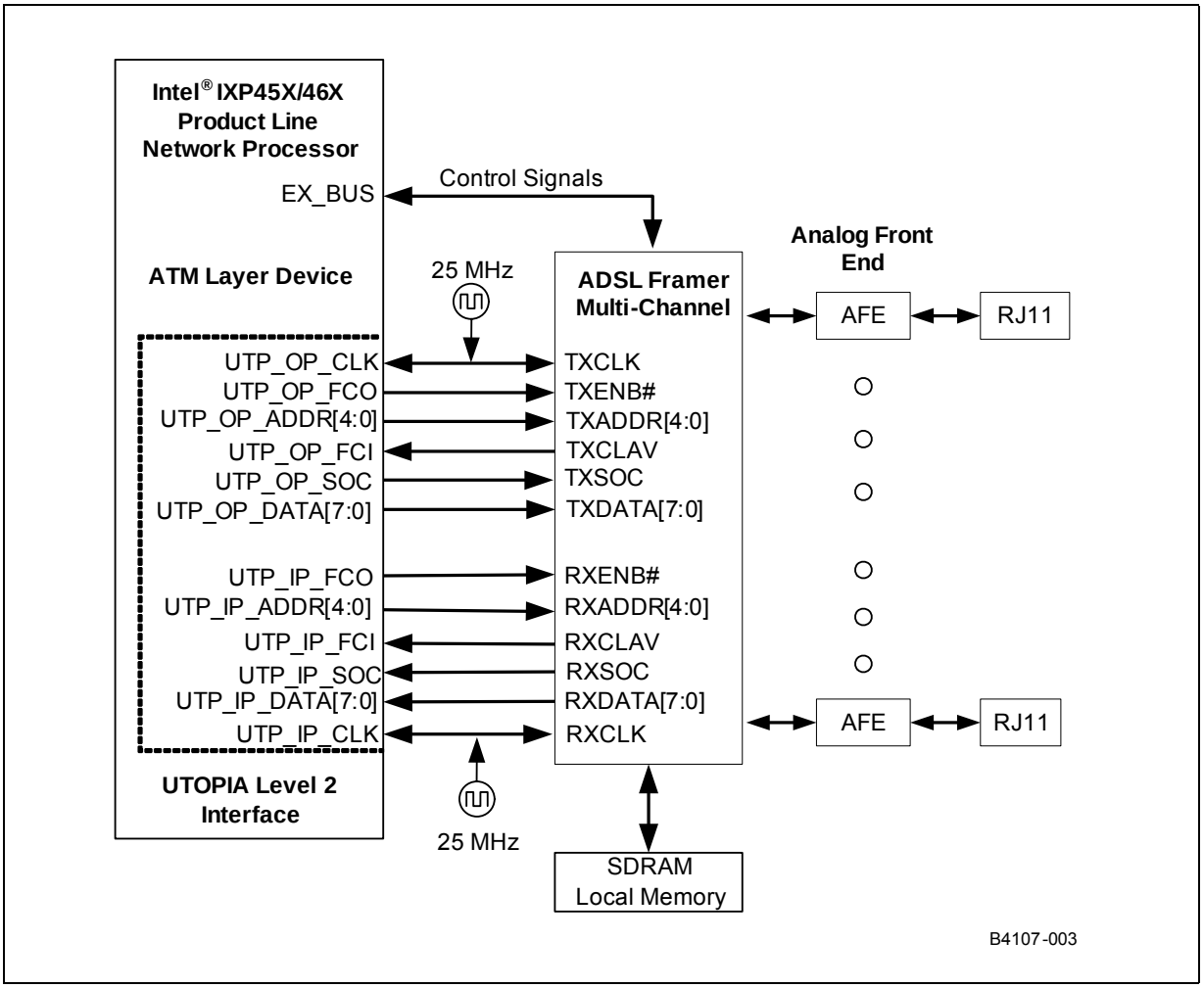
Name	Input/ Output	Pull Up/ Down	Recommendations
UTP_OP_CLK	I	Yes	UTOPIA Transmit clock input. Also known as UTP_TX_CLK. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_OP_FCO	O	Yes	UTOPIA flow control output signal. Also known as the TXENB_N signal. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_OP_SOC	O	Yes	Start of Cell. Also known as TX_SOC. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor.
UTP_OP_DATA[7:0]	O	No	UTOPIA output data.
UTP_OP_ADDR[4:0]	I/O	Yes	Transmit PHY address bus. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_OP_FCI	I	Yes	UTOPIA Output data flow control input: Also known as the TXFULL/CLAV signal. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_IP_CLK	I	Yes	UTOPIA Receive clock input. Also known as UTP_RX_CLK. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_IP_FCI	I	Yes	UTOPIA Input Data flow control input signal. Also known as RXEMPTY/CLAV. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_IP_SOC	I	Yes	Start of Cell. Also known as RX_SOC When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_IP_DATA[7:0]	I	Yes	UTOPIA input data. Also known as RX_DATA. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_IP_ADDR[4:0]	I/O	No	Receive PHY address bus.
UTP_IP_FCO	O	Yes	UTOPIA Input Data Flow Control Output signal: Also known as the RX_ENB_N. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

3.9.2 Device Connection

The following example shown in Figure 13 shows a typical interface to an ADSL Framer via the UTOPIA bus. Notice that depending on the framer used some control signals might be required which can be derived from the Expansion bus or the GPIO signals.

Figure 13. UTOPIA Interface Example



3.10 HSS Interface

NPE A has an integrated High-Speed Serial (HSS) module, whose primary function is to provide connectivity between the internal NPE A and the external HSS interface. There are two HSS ports that can directly interface to SLIC/CODEC devices for voice applications, or serial DSL framers. The HSS ports are software configurable to support various serial protocols, such as T1/ E1/J1, and MVIP. For a list of supported protocols, see the *Intel® IXP400 Software Programmer's Guide.*

3.10.1 Signal Interface

Table 17. High-Speed, Serial Interface 0

Name	Input Output	Pull Up Down	Recommendations
HSS_TXFRAME0	I/O	Yes	Transmit frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_TXDATA0	OD	Yes	Transmit data out. Open Drain Output. When this interface/signal is enabled and is either used or not used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor to V_{CCP}.
HSS_TXCLK0	I/O	Yes	Transmit clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXFRAME0	I/O	Yes	Receive frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXDATA0	I	Yes	Receive data input. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXCLK0	I/O	Yes	Receive clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features Enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

Table 18. High-Speed, Serial Interface 1

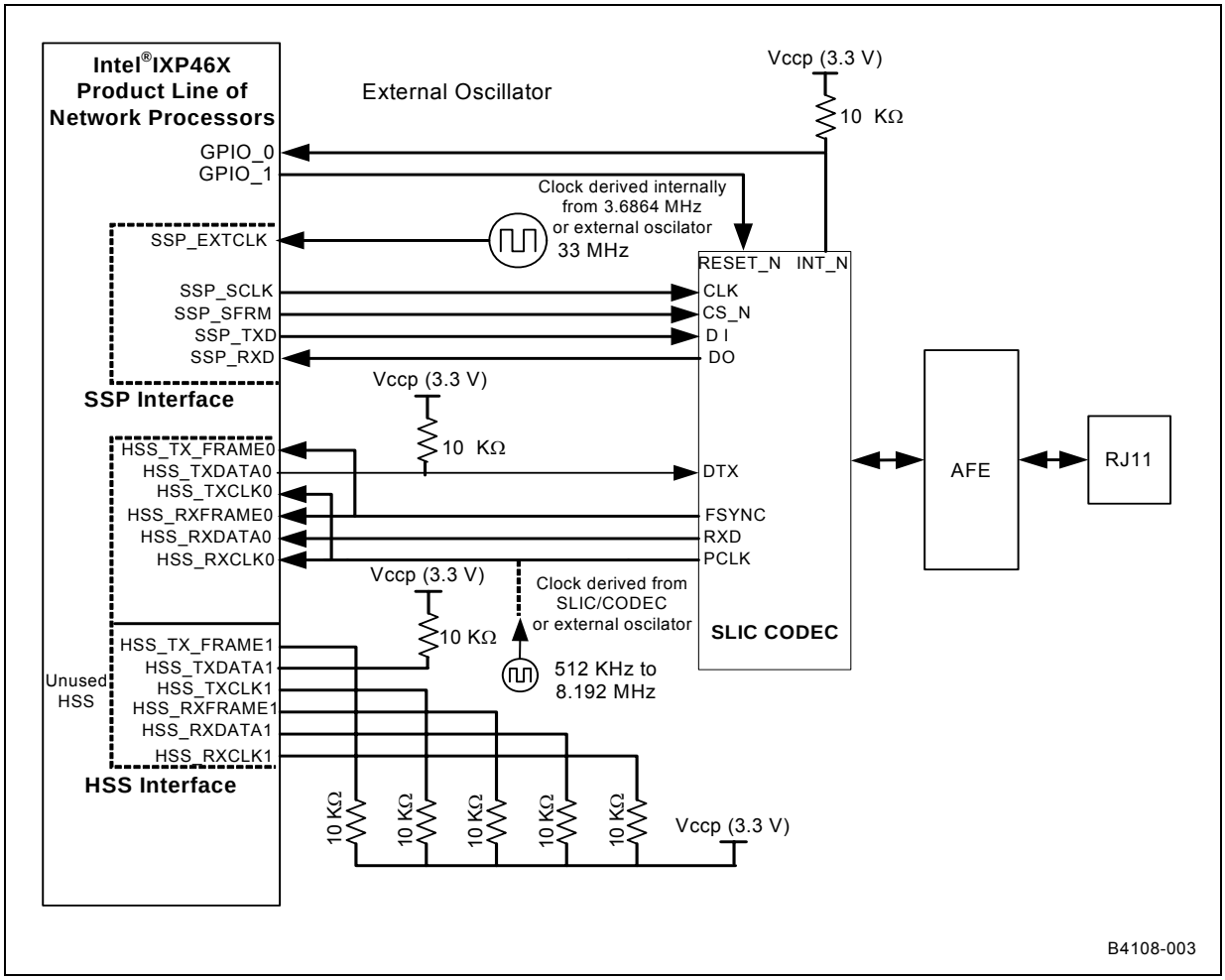
Name	Input Output	Pull Up Down	Recommendations
HSS_TXFRAME1	I/O	Yes	Transmit frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_TXDATA1	OD	Yes	Transmit data out. Open Drain output. When this interface/signal is enabled and is either used or not used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor to V_{CCP}.
HSS_TXCLK1	I/O	Yes	Transmit clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXFRAME1	I/O	Yes	Receive frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXDATA1	I	Yes	Receive data input. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXCLK1	I/O	Yes	Receive clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals*.**

3.10.2 Device Connection

Figure 14 shows a typical interface between the IXP45X/IXP46X product line and a SLIC CODEC, via the SSP and HSS ports, and a couple of GPIO signals.

Figure 14. HSS Interface Example



3.11 SSP Interface

The IXP45X/IXP46X network processors have a Synchronous Serial Peripheral Interface (SSP) module. Its primary function is to provide connectivity between the Intel XScale processor and an external SSP interface.

The SSP module supports National Microwire*, Texas Instruments* synchronous serial protocol (SSP), and Motorola* serial peripheral interface (SPI).

The clock rate can be selected from an internal, 3.6864-MHz source or external source fed at input pin SSP_EXTCLK. The clock can then be divided down anywhere from 7.2 KHz to 1.84 MHz by setting bits 15:08 in Control Register 0. For more information, see the SSP configuration registers in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

3.11.1 Signal Interface

Table 19. Synchronous Serial Peripheral Port Interface

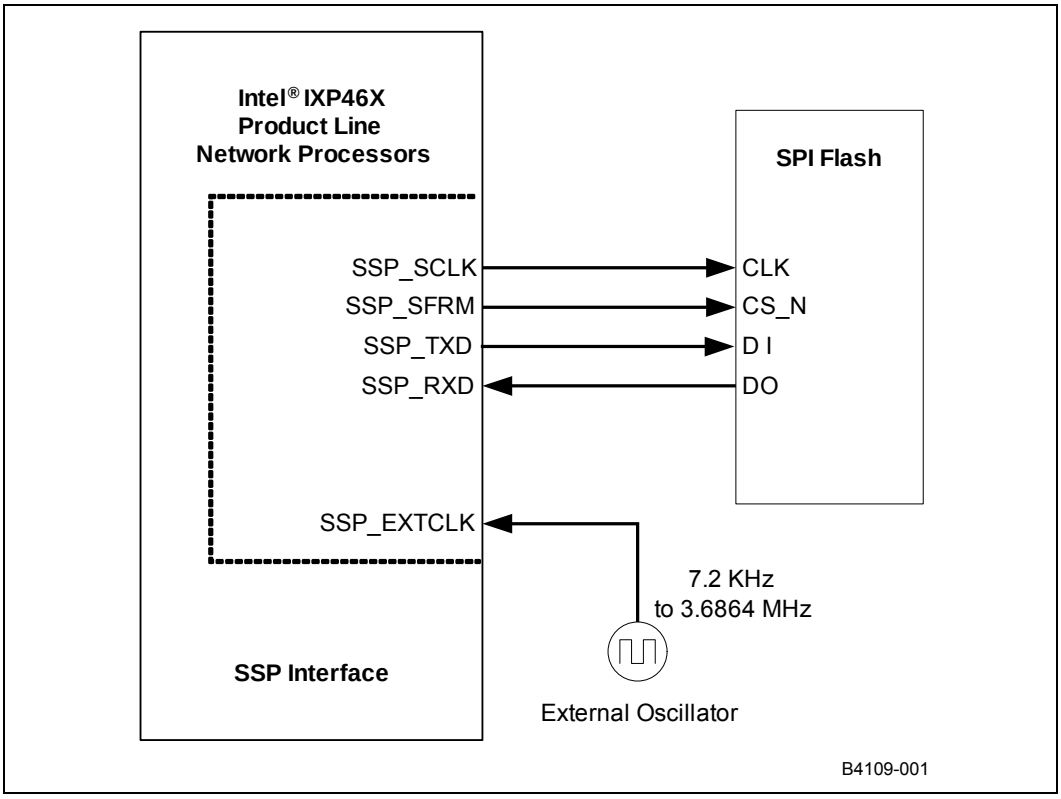
Name	Input/ Output	Pull Up/ Down	Recommendations
SSP_SCLK	O	No	Serial bit clock.
SSP_SFRM	O	No	Serial frame indicator.
SSP_TXD	O	No	Transmit data (serial data out).
SSP_RXD	I	Yes	Receive data (serial data in). Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
SSP_EXTCLK	I	Yes	External clock input. Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.

3.11.2 Device Connection

There are a number of devices available that can interface to SSP or SPI ports, these can range from RTC (Real-Time Clock), LCD (Liquid Crystal Displays), Digital Thermal Sensor to Flash memory devices.

One of the most common usage for SSP or SPI port, is serial flash code storage. Serial flash devices can be used to store board revision, serial numbers, or assembly information. Figure 15 provides an example of a Serial Flash device interface to the SSP port in the IXP45X/IXP46X network processors. For an additional example of SPI interface, refer to Figure 14, in which a SLIC is connected to the SSP and HSS ports.

Figure 15. Serial Flash and SSP Port (SPI) Interface Example



3.12 PCI Interface

The PCI Controller of the IXP45X/IXP46X network processors is an industry-standard, 32-bit interface, high-performance bus that operates at either 33 or 66 MHz (*PCI Local Bus Specification*, Rev. 2.2).

The PCI Controller supports operation as a PCI host and implements a PCI arbiter for a system containing up to four external PCI devices.

As indicated in Figure 16, a PCI transparent bridge is needed to support Compact PCI.

General PCI routing guidelines can be found in Section 6.2, "Topology" on page 71. For more detailed information, see the *PCI Local Bus Specification*, Rev. 2.2.

3.12.1 Signal Interface

Table 20. PCI Controller (Sheet 1 of 2)

Name	Input/ Output	Pull Up/ Down	Recommendations
PCI_AD[31:0]	I/O	Yes	PCI Address/Data bus. When this interface/signal is enabled and is not being used in a system design, the interface/ signal should be pulled high with a 10-KΩ resistor.
PCI_CBE_N[3:0]	I/O	Yes	PCI Command/Byte Enables. When this interface/signal is enabled and is not being used in a system design, the interface/ signal should be pulled high with a 10-KΩ resistor.
PCI_PAR	I/O	Yes	PCI Parity. When this interface/signal is enabled and is not being used in a system design, the interface/ signal should be pulled high with a 10-KΩ resistor.
PCI_FRAME_N	I/O	Yes	PCI Cycle Frame. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_TRDY_N	I/O	Yes	PCI Target Ready. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_IRDY_N	I/O	Yes	Initiator Ready. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_STOP_N	I/O	Yes	Stop. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_PERR_N	I/O	Yes	Parity Error. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_SERR_N	I/O	Yes	System Error. When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_DEVSEL_N	I/O	Yes	Device Select: When this interface/signal is enabled and is either being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

Table 20. PCI Controller (Sheet 2 of 2)

Name	Input/ Output	Pull Up/ Down	Recommendations
PCI_IDSEL	I	Yes	Initialization Device Select. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_REQ_N[3:1]	I	Yes	Arbitration Request. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_REQ_N[0]	I/O	Yes	Arbitration Request: When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_GNT_N[3:1]	O	No	Arbitration Grant.
PCI_GNT_N[0]	I/O	Yes	Arbitration Grant. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_INTA_N	O/D	Yes	Interrupt A. When this interface/signal is enabled and is either used or not used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_CLKIN	I	Yes	Clock input. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals*.**

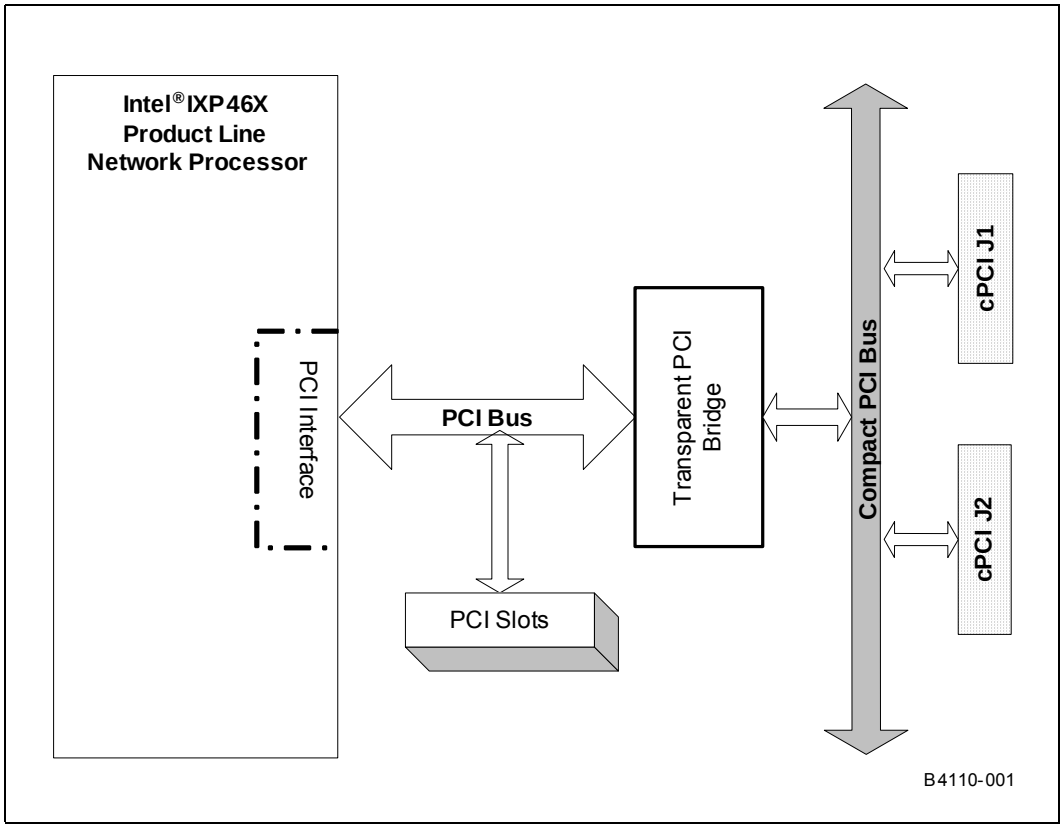
3.12.2 PCI Interface Block Diagram

When using the IXP45X/IXP46X network processors in Master mode, the PCI module can interface to up to four PCI cards (devices) at 33 MHz or two PCI cards at 66 MHz. The limitation to two cards (devices) at 66 MHz is due to load requirements to maintain signal integrity at the higher frequency.

The PCI-to-PCI bridge must be used in order to address the PCI requirement not to exceed one load per PCI connector unless it is through a PCI-to-PCI bridge.

The IDSEL signals on the PCI slots can be connected to one of the PCI_AD lines, preferable to the higher order address signals. Reset support can be accomplished by using one of the GPIO pins to generate a reset or through an external decoder of the Expansion bus.

Figure 16. PCI Interface



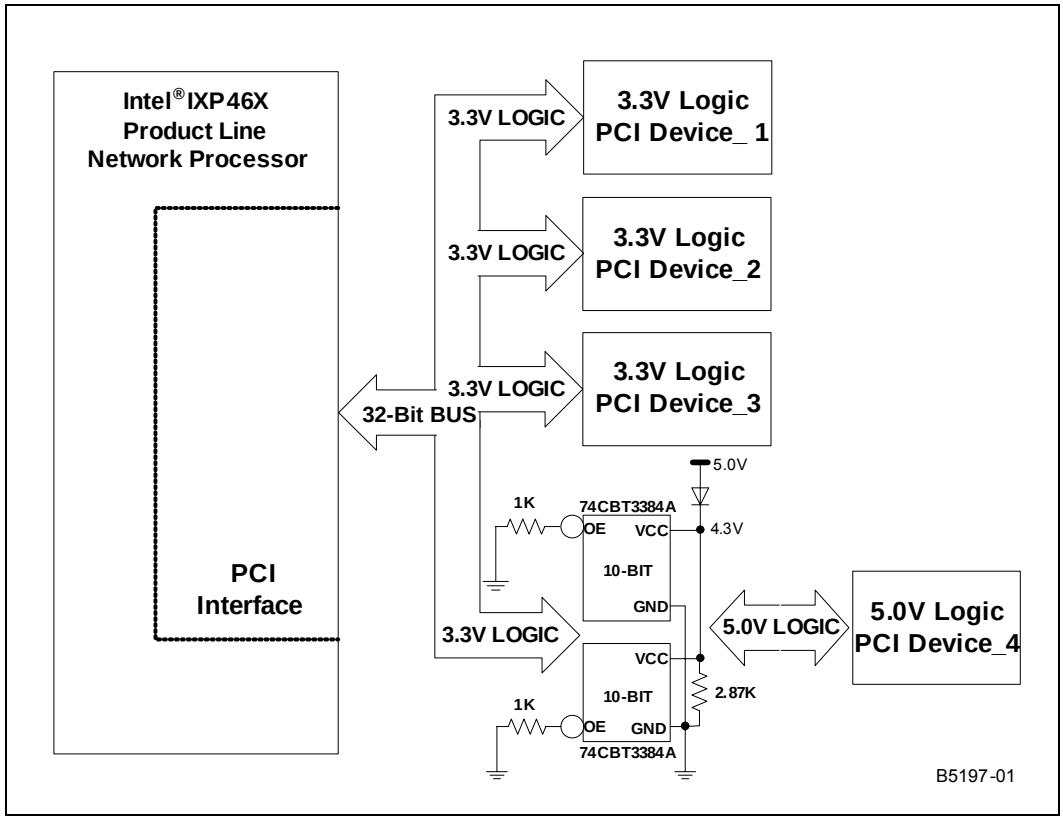
3.12.3 Supporting 5 V PCI Interface

It is possible to support 5 V PCI devices with the help of voltage logic translators. One option can be implemented with voltage level translator. The Texas Instruments* family of FET bus switches CBT devices can be a good solution. The 10-bit SN74CBT3384A has been proven to work very effectively with the Intel® IXP465 Network Processor. All control and DATA/ADDRESS signals (bidirectional and not) need to be translated before connecting the 3.3 V to the 5 V logic together. Signals which are not used, do not need to be translated, simply follow the recommendations described in Table 20.

Figure 17 shows a block diagram of the interface required to perform the conversion. Ensure that all signals connect to either of the two interfacing logic levels.

T_{PROP} (Bus Propagation Delay) is the maximum time for a complete flight. When you calculate T_{PROP}, you must include in your timing calculation the T_{PD} (Time for Propagation Delay) of the voltage translator. For details, refer to Section 6.2.

Figure 17. PCI 3.3 V to 5 V Logic Translation Interface



3.12.4 PCI Option Interface

The IXP45X/IXP46X network processors can be used in a design as a host or as an option device. This section describes how the IXP45X/IXP46X network processors can be connected as an option device to obtain proper functionality. There are slight differences in the hardware interface when designing for option mode. All routing and board recommendations described in previous sections of this document apply, however the design must use the device pin connections listed in Table 21.

Table 21. PCI Host/Option Interface Pin Description (Sheet 1 of 3)

Name	Host Input Output	Device-Pin Connection	Option Input Output	Description
PCI_AD[31:0]	I/O	All address/data signals need to be connected between the two devices.	I/O	PCI Address/Data bus
PCI_CBE_N[3:0]	I/O	Connect signals to same pins between the two devices.	I/O	PCI Command/Byte Enables
PCI_PAR	I/O	Connect signal to same pin between the two devices.	I/O	PCI Parity
PCI_FRAME_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	PCI Cycle Frame

Table 21. PCI Host/Option Interface Pin Description (Sheet 2 of 3)

Name	Host Input Output	Device-Pin Connection	Option Input Output	Description
PCI_TRDY_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	PCI Target Ready
PCI_IRDY_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Initiator Ready
PCI_STOP_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Stop
PCI_PERR_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Parity Error
PCI_SERR_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	System Error
PCI_DEVSEL_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Device Select
PCI_IDSEL	I	Connect one of the higher order PCI address signals to the Device. Connect a 10K pull-up resistor to the Host.	I	Initialization Device Select
PCI_REQ_N[3:1]	I	From the Option device, connect output signal PCI_REQ_N[0] to one of the PCI_REQ_N[3:0] inputs to the Host. Note: the PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.	I	Arbitration Request On the Option device, these signals are not used, they should be pulled high with a 10-KΩ resistor. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.
PCI_REQ_N[0]	I	From the Option device, connect output PCI_REQ_N[0] to one of the PCI_REQ_N[3:0] inputs to the Host. Note: the PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.	O	Arbitration Request On the Option device, this signal is an output and must be connected to one of the PCI_REQ_N[3:0] inputs to the Host. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.
PCI_GNT_N[3:1]	O	Connect one of the Host outputs PCI_GNT_N[3:0] to PCI_GNT_N[0] input to the Option. Note: the PCI_GNT_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.	O	Arbitration Grant On the Option device, these signals are not used, they should be pulled high with a 10-KΩ resistor.
PCI_GNT_N[0]	O	Connect one of the Host outputs PCI_GNT_N[3:0] to PCI_GNT_N[0] input to the Option. Note: the PCI_GNT_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.	I	Arbitration Grant On the Option device, this signal is an input and must be connected to one of the PCI_GNT_N[3:0] outputs of the Host. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where “n” must be the same number in the square bracket.

Table 21. PCI Host/Option Interface Pin Description (Sheet 3 of 3)

Name	Host Input Output	Device-Pin Connection	Option Input Output	Description
PCI_INTA_N	O/D	Connect PCI_INTA_N output from the Option to one of the GPIO input signals of the Host. The GPIO signal at the Host must be configure as an input interrupt level sensitive.	O/D	Interrupt A This interrupt is generated from the Option to one of the GPIO inputs to the Host. On the Host this signal is not used, it should be pulled high with a 10-KΩ resistor.
PCI_CLKIN	I	Clock must be connected to both devices. Trace lengths must be matched. Use point to point clock distribution.	I	Clock input

3.12.5 Design Notes

- The IXP45X/IXP46X network processors do not support the 5 V PCI signal interface by itself. Only the 3.3 V signal interface is supported without signal level conversion, however, it is possible to interface to 5 V logic when using a voltage level converter. See Figure 17 for details.
- The *PCI Local Bus Specification*, Rev. 2.2 requires that the bus is always “parked”, as some device is always driving the AD lines. There is need to use pull-ups on these signals. The specification states that the following control lines should be pulled up:
  - FRAME#
  - TRDY#
  - IRDY#
  - DEVSEL#
  - STOP#
  - SERR#
  - PERR#
  - LOCK#
  - INTA#
  - INTB#
  - INTC#
  - INTD#
- The processors’ GPIO pins can be used by PCI devices on PCI slots to request an interrupt from the processors’ PCI controller.
- PCI_INTA_N is used to request interrupts to external PCI Masters. This signal is an open collector and requires a pull-up resistor.

3.13 JTAG Interface

JTAG is the popular name for IEEE standards 1149.1-1990 and 1149.1a-1993, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, which provides support for:

- Board-level boundary-scan connectivity testing
- Connection to software debugging tools through the JTAG interface
- In-system programming of programmable memory and logic devices on the PCB

The interface is controlled through five dedicated test access port (TAP) pins: TDI, TMS, TCK, nTRST, and TDO, as described in the IEEE 1149.1 standard. The boundary-scan test-logic elements include the TAP pins, TAP controller, instruction register, boundary-scan register, bypass register, device identification register, and data-specific registers. These are described in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*.

The IXP45X/IXP46X network processors may be controlled during debug through a JTAG interface to the processor, the debug tools such as the Macraigor* Raven*, EPI* Majic*, Wind River Systems* visionPROBE* / visionICE* or various other JTAG tools plug into the JTAG interface through a connector.

3.13.1 Signal Interface

Table 22. Synchronous Serial Peripheral Port Interface

Name	Input/ Output	Pull Up/ Down	Recommendations
JTG_TMS	I	Yes	Test mode select. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.
JTG_TDI	I	Yes	Test Input data. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.
JTG_TDO	O	O	Test Output data.
JTG_TRST_N	I	Yes	Test Reset. When the JTAG interface is not being used, the signal must be pulled low using a 10-kΩ resistor.
JTG_TCK	I	Yes	Test Clock. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.

3.14 Input System Clock

The IXP45X/IXP46X network processors require a 33.33-MHz reference clock to generate all internal clocks required — including core clock — and the various buses running internally within the system.

3.14.1 Clock Signals

Table 23. Clock Signals

Name	Type*	Description
OSC_IN	I	Source must be a clock input of 33.33-MHz. Use a series termination resistor, 10 Ω to 33 Ω at the source.
OSC_OUT	O	No connect

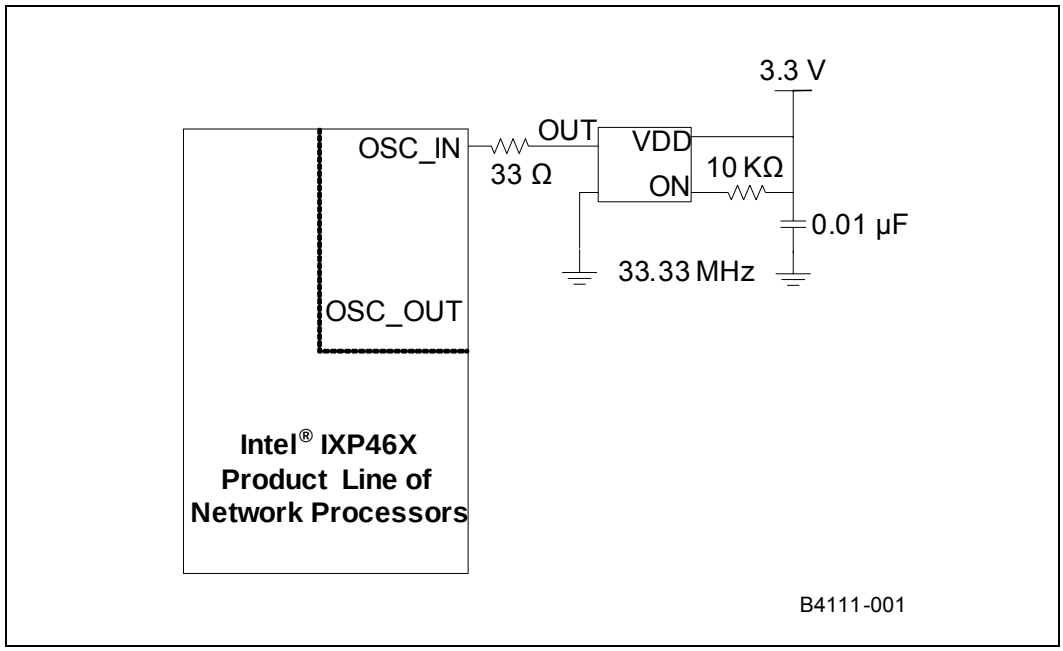
Note: For explanations of the **Type** column abbreviations, see Table 2 on page 17.

3.14.2 Clock Oscillator

When using an external clock oscillator to supply the 33.33-MHz reference system clock, connect the clock oscillator output to OSC_IN pin through a series termination of 33 Ω as shown in Figure 18. The series termination helps smooth the rise and fall edges of the clock and eliminate ringing. Leave the OSC_OUT pin un-connected.

3.14.3 Device Connection

Figure 18. Clock Oscillator Interface Example



3.15 Power

To enable low power system design, the IXP45X/IXP46X network processors have separate power supply domains for the processor core, DDR SDRAM memory, and input/output peripherals.

Table 24. Power Interface (Sheet 1 of 2)

Name	Nominal Voltage	Description
VCC	1.3 V	Core supply voltage. **Note:** If operating at 667MHz, core supply voltage must be increased to VCC = 1.5 V. For details, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
VCCP	3.3 V	I/O supply voltage.
VCCM	2.5 V	DDR memory interface supply voltage.
VSS	GND	Ground for supply voltages 3.3 V, 2.5 V, and 1.3/1.5 V.
OSC_VCCP	3.3 V	Supply voltage for peripheral (I/O) logic of analog oscillator circuitry. Require special power filtering circuitry. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
OSC_VSSP	GND	Ground for peripheral (I/O) logic of analog oscillator circuitry. Used in conjunction with the OSC_VCCP pins. Require special power filtering circuitry. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
OSC_VCC	1.3 V	Supply voltage for internal logic of the analog oscillator circuitry. Requires special power filtering circuitry. If operating at 667 MHz, this voltage must be increased to 1.5 V. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
OSC_VSS	GND	Ground for internal logic of the analog oscillator circuitry. Used in conjunction with the OSC_VCC pins. Require special power filtering circuitry. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

Table 24. Power Interface (Sheet 2 of 2)

Name	Nominal Voltage	Description
VCCPLL1	1.3 V	Supply voltage for internal logic of analog phase lock-loop circuitry. Requires special power filtering circuitry. If operating at 667 MHz, this voltage must be increased to 1.5 V. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
VCCPLL2	1.3 V	Supply voltage for internal logic of analog phase lock-loop circuitry. Requires special power filtering circuitry. If operating at 667 MHz, this voltage must be increased to 1.5 V. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
VCCPLL3	1.3 V	Supply voltage for internal logic of analog phase lock-loop circuitry. Requires special power filtering circuitry. If operating at 667 MHz, this voltage must be increased to 1.5 V. See the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

3.15.1 De-Coupling Capacitance Recommendations

It is common practice to place de-coupling capacitors between the supply voltages and ground. Placement can be near the input supply pins and ground, with one 100-nF capacitor per pin. Additional de-coupling capacitors can be place all over the board every 0.5” to 1.0”. This ensures good return path for currents and reduce power surges and high-frequency noise.

It is also recommended that 4.7-µF to 10-µF capacitors be placed every 2” to 3”.

3.15.2 VCC De-Coupling

Connect one 100-nF capacitor per each VCC pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.15.3 VCCP De-Coupling

Connect one 100-nF capacitor per each VCCP pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.15.4 VCCM De-Coupling

Connect one 100-nF capacitor per each VCCM pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.15.5 Power Sequence

Power sequence is crucial for proper functioning of the IXP45X/IXP46X network processors. For a complete description of power sequencing, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

3.15.6 Reset Timing

Proper reset timing is also a crucial requirement for proper functioning of the IXP45X/ IXP46X network processors. There are two reset signal PWRON_RESET_N and RESET_IN_N which required assertion sequence.

For a complete description of their functionality, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet* and its section titled “Reset Timings.” PWRON_RESET_N is used as a Power Good and RESET_IN_N is used for resetting internal registers.

The IXP45X/IXP46X network processors can be configured at reset de-assertion via external, pull-down resistors on the address expansion bus signals EX_ADDR[23:21]. For a complete description, see Section 3.3.2, “Reset Configuration Straps” on page 21.

4.0 General PCB Guide

4.1 PCB Overview

Beginning with components selection, this chapter presents general PCB guidelines. In cases where it is too difficult to adhere to a guideline, engineering judgment must be used. The methods are listed as simple DOs and DON'Ts.

This chapter does not discuss the functional aspects of any bus, or layout guides for any interfaced devices.

4.2 General Recommendations

It is recommended that boards based on the IXP45X/IXP46X network processors employ a PCB stackup yielding a target impedance of 50 Ω ± 10% with 5 mil nominal trace width. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces.

When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce cross-talk and settling time.

4.3 Component Selection

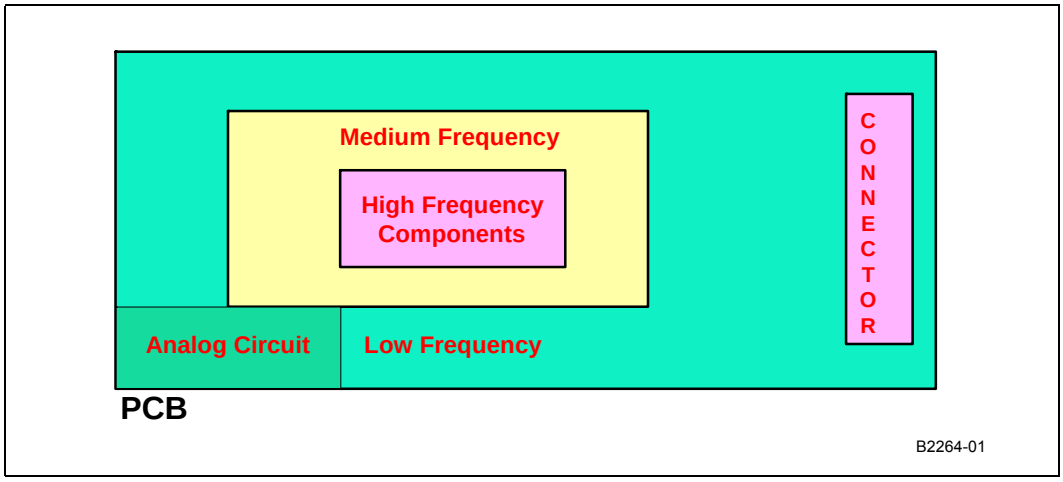
- Do not use components faster than necessary
  Clock rise (fall) time should be as slow as possible, as the spectral content of the waveform decreases
- Use components with output drive strength (slew-rate) controllable if available
- Use SMT components (not through-hole components) as through-hole (leaded) components have more stub inductance due to the protruding leads.
- Avoid sockets when possible
- Minimize number of connectors

4.4 Component Placement

As shown in Figure 19 on page 60, when placing components, put:

- High-frequency components in the middle
- Medium-frequency around the high-frequency components
- Low-frequency components around the edge of the printed circuit board

Figure 19. Component Placement on a PCB



- Place noisy parts (clock, processor, video, etc.) at least 1.5 – 3 inches away from the edge of the printed circuit board.
- Do not place noisy components close to internal/external cables
  - — Any loose cables picks up noise and act as an antenna to radiate that noise
  - — Be aware of the peak in-rush surge current into the device pins. This surge current may inject high-frequency switching noise into power planes of the printed circuit board.
- Place high-current components near the power sources.
- Do not share the same physical components (such as buffers and inverters) between high-speed and low-speed signals. Use separate parts.
- Place clock drivers and receivers such that clock trace length is minimized.
- Place clock generation circuits near a ground stitch location. Place a localized ground plane around the clock circuits and connect the localized plane to system ground plane.
- Install clock circuits directly on the printed circuit board, not on sockets.
- Clock crystals should lie *flat* against the board to provide better coupling of electromagnetic fields to the board.

4.5 Stack-Up Selection

Stack-up selection directly affects the trace geometry which, in turn, affects the characteristic impedance requirement for the printed-circuit board. Additionally, the “clean,” noise-free-planes design and placement is significantly important as components run at higher speeds requiring more power.

Considerations include:

- Low-speed, printed-circuit-board construction — for example two-layer boards:
  - — Advantages:
    - Inexpensive
    - Manufactured by virtually all printed-circuit-board vendors
  - — Disadvantages:

    - Poor routing density
    - Uncontrolled signal trace impedance
    - Lack of power/ground planes, resulting in unacceptable cross-talk
    - Relatively high-impedance power distribution circuitry, resulting in noise on the power and ground rails
- High-speed circuits require multi-layer printed circuit boards:
  - Advantages:
    - Controlled-impedance traces
    - Low-impedance power distribution
  - Disadvantages:
    - Higher cost
    - More weight
    - Manufactured by fewer vendors
- Symmetry is essential to keep the board stack-up symmetric about the center This minimizes warping
- For best impedance control, have:
  - No more than two signal layers between every power/ground plane pair
  - No more than one embedded micro-strip layer under the top/bottom layers
- For best noise control, route adjacent layers orthogonally. Avoid layer-to-layer parallelism.
- Fabrication house must agree on design rules, including:
  - Trace width, trace separation
  - Drill/via sizes
- The distance between the signal layer and ground (or power) should be minimized to reduce the loop area enclosed by the return current
  - Use 0.7:1 ratio as a minimum.
    For example: 5-mil traces, 7-mil prepreg thickness to adjacent power/ground.

Figure 20 gives an example for a six-layer and eight-layer board. For stripline (signals between planes), the stackup should be such that the signal line is closer to one of the planes by a factor of five or more. Then the trace impedance is controlled predominantly by the distance to the nearest plane.

Figure 20 and Figure 21 illustrate the proposed stackup for the six- and eight-layer boards.

Figure 20. 8-Layer Stackup

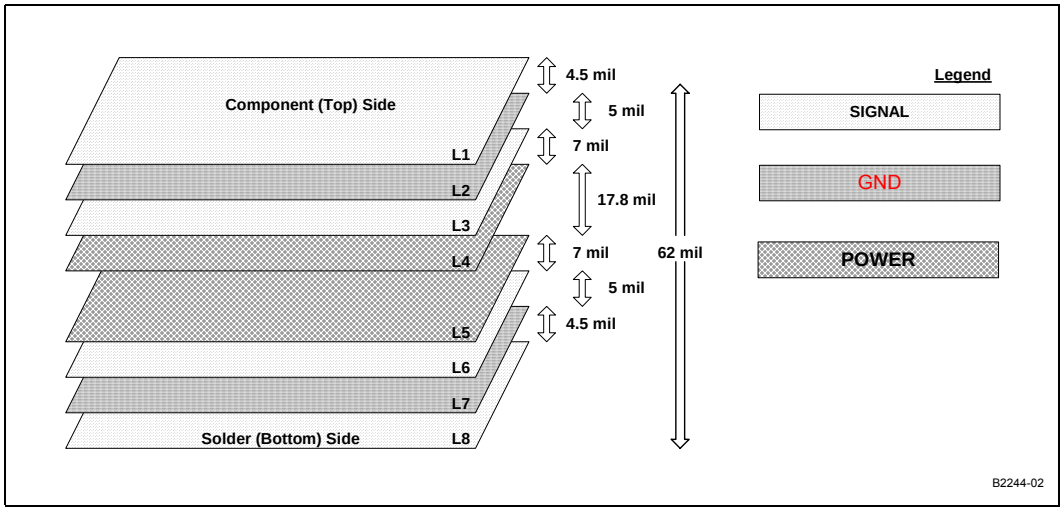
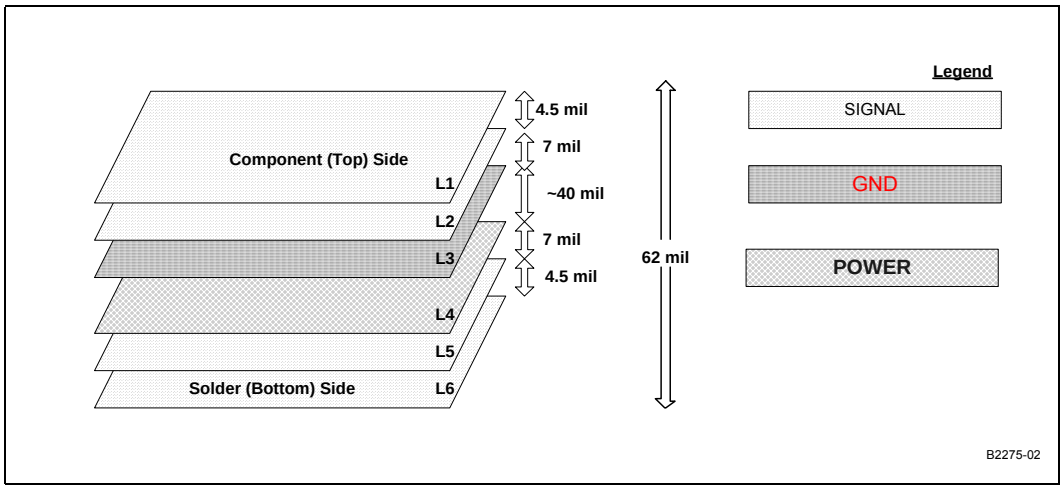


Figure 21. 6-Layer Stackup



- Fast and slow transmission line networks must be considered
- PCB-board velocities
- Board FR4 ~ 4.3
- Target impedance of 50 Ω ± 10%
- Trace width: 5 mils
- Signal Layers (1/2 oz. Copper)
- Power Layer (1 oz. Copper)
- Ground (GND) Layer (1 oz. Copper)

5.0 General Layout and Routing Guide

5.1 Overview

This chapter provides routing and layout guides for hardware and systems based on the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors.

The high-speed clocking required when designing with the processors requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid designers with board layout. In cases where it is too difficult to follow a design rule, engineering judgment must be used.

5.2 General Layout Guidelines

The layout guidelines recommended in this section are based on experience and knowledge gained from previous designs. Layer stacking varies, depending on design complexity, however following standard rules helps minimize potential problems dealing with signal integrity.

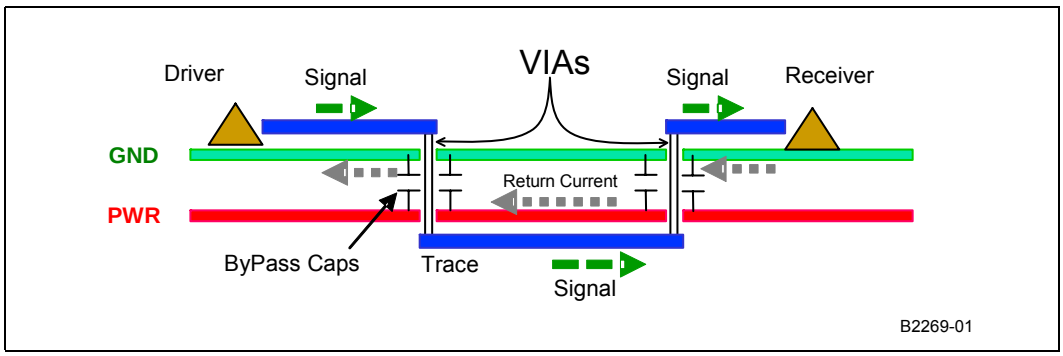
The following are well know documented recommendations that helps route a functional board:

- Providing enough routing layers to comply with minimum and maximum timing requirements of the IXP45X/IXP46X network processors and other components.
- Connectors, and mounting holes must be placed in a ways that will not interfere with basic design guidelines in this document.
- Provide uniform impedance throughout the board, specially for high speed areas such us clocking, DDR-SDRAM, PCI, device bus, etc.
- Place analog, high-voltage, power supply, low-speed, and high-speed devices in different sections of the board.
- Decoupling capacitors must be placed next to power pins.
- Series termination resistors must be placed close to the source.
- Analog and digital sections of the board must be physically isolated from each other. No common ground, power planes, and signal traces are allowed to cross-isolation zones. Use appropriately sized PCB traces for larger enough to handle peak current. Keep away from high-speed digital signals.
- Keep stubs as short as possible (preferably, the electrical length of the stub less than half of the length of the rise time of signal).
- All critical signals should be routed before all other non-critical signals.
- Do not route signals close to the edge of the board, power or ground planes. Route signal at least 50 to 100 mils away from the edge of the plane.
- Try to match buses to the same trace length and keep them in groups adjacent to each other, away from other signals.
- Route processor address, data and control signals using a “daisy-chain” topology.
- Minimize number of vias and corners on all high speed signals.
- Do not route under crystals or clock oscillators, clock synthesizers, or magnetic devices (ferrites, toroids).
- Maintain trace spacing consistent between differential pairs and match trace length.
- Keep differential signals away from long and parallel, high-speed paths, such as clock signals and data strobe signals.

- Do not place high-frequency oscillators and switching network devices close to sensitive analog circuits.
- Arrange the board so that return currents for high-speed traces never must jump between planes. Restrict traces to remain on either side of whichever ground plane they start out nearest. This allows the use of naturally grouped horizontal and vertical routing layers.

If signals change between layers, the reference voltage changes, as shown in Figure 22. This creates discontinuity in the path of the signal.

Figure 22. Signal Changing Reference Planes



The design in Figure 22, routes a signal on the top layer, close to GND plane, and provides a very good return current path. The signal then is routed to the bottom layer, close to the PWR plane, such that the return currents flows to the ground plane through bypass caps. Hence the path for the return currents is less inductive than in the previous case when the signal is routed on the top layer.

5.2.1 General Component Spacing

- Do not place components within 125 mils to the edge of the printed circuit board. For exact dimensions consult your manufacturing vendor.
- Keep a minimum spacing between via and the solder pad edges $\geq$ 25mil.
- Position devices that interface with each other close to one another to minimize trace lengths.

Figure 23. Good Design Practice for VIA Hole Placement

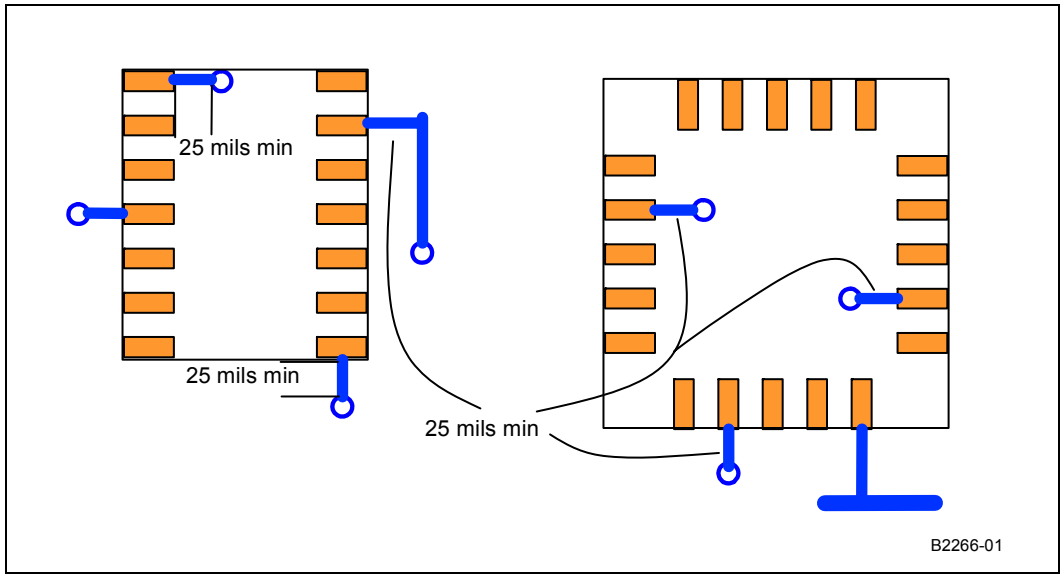


Figure 23 and Figure 24 show good and poor design practices for via placement on surface-mount boards.

Figure 25 shows minimum pad-to-pad clearance for surface-mount passive components and PGA or BGA components.

Figure 24. Poor Design Practice for VIA Placement

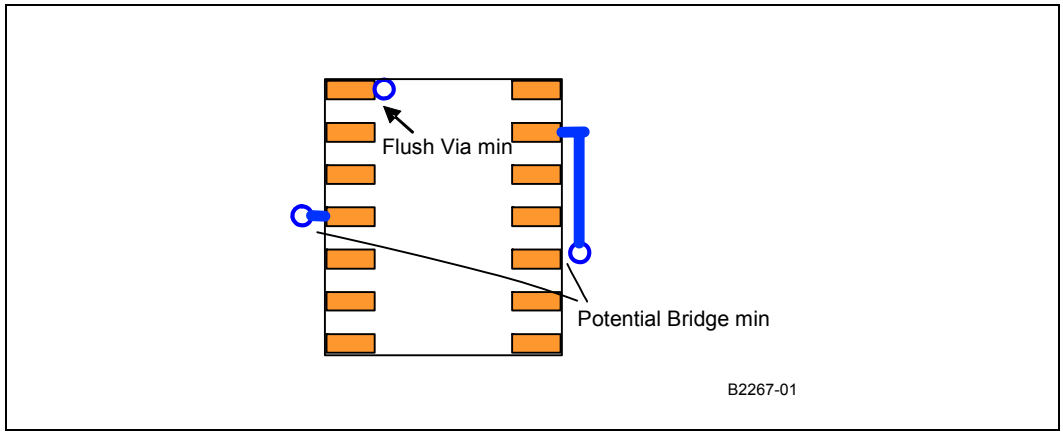
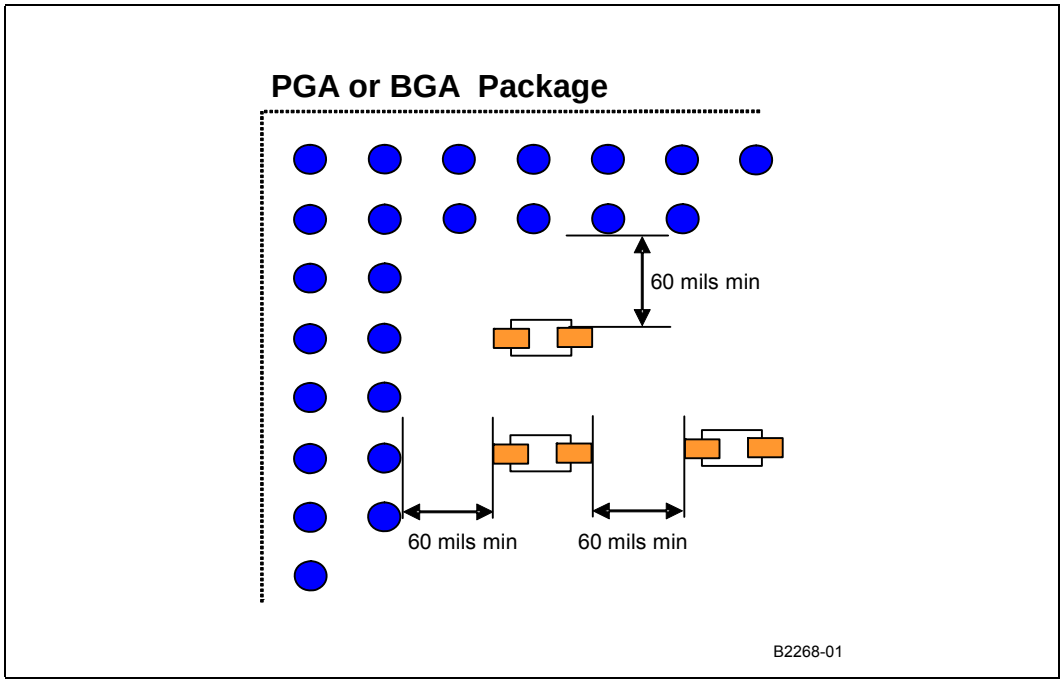


Figure 25. Pad-to-Pad Clearance of Passive Components to a PGA or BGA



5.2.2 Clock Signal Considerations

- Provide good return current paths for clock traces.
- Keep clock traces away from the edge of the board and any other high-speed devices or traces.
- Keep clock traces away from analog signals, including voltage reference signals.
- Clock signals should not cross over a split plane.
- Route clock signals in a single, internal layers and eliminate routing in multiple layers as much as possible.
- Do not route traces or vias under crystals or clock oscillators devices unless there is a plane between the trace and the component.
- Do not route parallel signal traces directly above or below clock traces unless there is a ground or at least a power plane separation between those layers.
- Route clock traces with a minimum number of vias.
- Space clock traces away from other signals three times the trace width on each side.
- Use guard traces when routing on top or bottom layers whenever possible. Guard traces must be connected to ground.
- Do not daisy-chain, instead use point-to-point clock distribution. Place a series termination resistor as close as possible to the source.
- Keep traces short to minimize reflections and signal degradation.
- Maintain control impedance for all clock traces, microstrip or stripline.
  - Be aware of propagation delays between a microstrip and stripline.

  - — Calculate capacitive loading of all components and properly compensate with a series or parallel terminations.
- Measure and match trace lengths for devices that interface with each other and have their clock derived from the same source.

  If traces must be long, treat them as transmission lines. Terminate clock traces to match trace impedance.
- If there is a power plane, instead of a ground plane, make sure that the power plane has adequate decoupling to ground, especially near clock drivers and receivers.

5.2.3 SMII Signal Considerations

SMII signals run at 125 MHz, single-ended and require proper trace-routing to achieve good signal integrity and impedance matching. The following recommendations help with designs:

- Do not route any of the SMII signals under the IXP45X/IXP46X network processors, or any other components, unless a ground or power plane isolates the signals.
- Minimize the number of vias to two per trace.
- Keep traces as short as possible and straight, away from other signals.
- Control impedance should maintain to 50 Ω.
- RX signals must have the same length and TX signals must have the same length.
  - — For the RX group, match the lengths for signals SMII_RX_SYNC, SMII_RX_DATA, and SMII_RX_CLK.
  - — For TX group, match lengths for signals SMII_TX_SYNC, SMII_TX_DATA, and SMII_TX_CLK.
- Avoid sharp corners, using 45° corners instead.

5.2.4 MII Signal Considerations

MII signals run at 25 MHz which makes them less critical that SMII. But these signals still require certain routing guide lines.

- Minimize the number of vias to two per trace.
- Keep traces as short as possible and straight, away from other signals.
- Control impedance should maintain to 50 Ω.
- Each group either RX or TX must be length match.
- Avoid sharp corners, using 45° corners instead.

5.2.5 USB Considerations

Follow the schematic sample shown in Section 3.8, “USB Interface” on page 38 and the recommended schematic interface.

The following are recommendations for routing differential pair signal required to by the USB interface:

- Traces can be routed in tightly couple structure with 5mil trace width and 10-mil air gap, or maintain air gap equal 2X trace width. It is recommended these be hand-routed.
- Match trace length for each differential pair.
- Avoid sharp corners, using 45° corners instead.

- Wherever possible, use a perfect symmetry within a differential pair.
- Minimize the number vias.
- Avoid routing other signals close by or in parallel to the differential pair, maintaining no less than 50 mil to any other signal.
- Maintain control impedance for each differential pair to 90 Ω +/- 15 Ω.
- Use high value ferrite beads (100 MHz/60 Ω – 100 MHz/240 Ω).

5.2.6 Cross-Talk

Cross-talk is caused by capacitance and inductance coupling between signals. It is composed of both backward and forward cross-talk components.

Backward cross-talk creates an induced signal on the network that propagates in the opposite direction of the aggressor signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software should be used to analyze your board layout for cross-talk problems.

- To effectively route signals on the PCB, signals are grouped (address, data, etc.).
  - The space between groups can be 3 w (where w is the width of the traces).
  - Space within a group can be just 1 w.
  - Space between clock signals or clock to any other signal should be 3 w. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.

5.2.7 EMI-Design Considerations

It is strongly recommended that good electromagnetic interference (EMI) design practices be followed when designing with the IXP45X/IXP46X network processors.

- Information on spread-spectrum clocking is available in *Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor: Spread-Spectrum Clocking to Reduce EMI Application Note.*
- Place high-current devices as closely as possible to the power sources.
- Proper termination of signals can reduce reflections, which may emit a high-frequency component that may contribute to more EMI than the original signal itself.
- Ferrite beads may be used to add high frequency loss to a circuit without introducing power loss at DC and low frequencies. They are effective when used to absorb high-frequency oscillations from switching transients or parasitic resonances within a circuit.
- Keep rise and fall times as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics which may radiate significantly.
- A solid ground is essential at the I/O connector to chassis and ground plane.
- Keep the power plane shorter than the ground plane by at least 5x the spacing between the power and ground planes.
- Stitch together all ground planes around the edge to the board every 100 to 200 mil. This helps reduce EMI radiating out of the board from inner layers.

5.2.8 Trace Impedance

All signal layers require controlled impedance of 50 Ω ±10 % microstrip or stripline (unless otherwise specified) where appropriate. Selecting the appropriate board stack-up to minimize impedance variations is very important.

When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces.

5.2.9 Power and Ground Plane

Power and ground planes should have sufficient de-coupling capacitors to ensure sustainable current needed for high-speed switching devices. (See Section 3.15.1, “De-Coupling Capacitance Recommendations” on page 56.)

- It is highly recommended to use sufficient internal power and ground planes.
- Due to the complexity of the IXP45X/IXP46X network processors, there are a number of power supplies required. It is appropriate to use power islands in the power plane under the processor, as it would be too expensive to have a power plane for each power source.
- Power islands must be large enough to include the required power supply decoupling capacitance, and the necessary connection to the voltage source and destination.
- Islands can be separated by a minimum of 20-mil air gap.
- Use at least one via per power or ground pin, wherever possible use more vias, depending on current drawn.
- Use at least one de-coupling capacitor per power pin and place it as close as possible to the pin.
- Minimize the number of traces routed across the air gaps between power islands.
  - Each crossing introduces signal degradation due to the impedance discontinuity.
  - For traces that must cross air gaps, route them on the side of the board next to a ground plane to reduce or eliminate signal degradation caused by crossing the gap.
  - When this is not possible, then route the trace to cross the gap at a right angle (90°).

6.0 PCI Interface Design Considerations

The Intel® IXP45X and Intel® IXP46X Product Line of Network Processors has a single, 32-bit PCI device module that runs at 33/66 MHz. This chapter describes some basic guidelines to help design hardware that interfaces with PCI devices.

The PCI module is compatible with the *PCI Local Bus Specification*, Rev. 2.2. For a complete functional description and physical requirements, see *PCI Local Bus Specification*, Rev. 2.2.

6.1 Electrical Interface

The electrical definition is restricted to 3.3 V signaling environment. The device is *not* 5 V tolerant. All devices interfacing with the PCI module need to operate at 3.3 V.

6.2 Topology

Interfacing devices need to be connected in a daisy-chain topology. When more than one device is in the bus, connecting stubs need to be kept as short as possible.

There is a limitation to the number of devices connected to the internal arbiter. If more than four devices are required to be connected, an external arbiter is required.

The system time budget must be satisfied for 66 MHz and 33 MHz cycles. It is expected that if the timing budget for 66 MHz clock cycles is satisfied, then the 33 MHz cycles also work. The following equation and timing parameters need to be met when routing a board that either interfaces to a single PCI device or up to four devices as shown in Figure 26.

$T_{CYC} \geq T_{VAL} + T_{PROP} + T_{SKEW} + T_{SU}$

where:

T_{VAL} = Valid Output Delay
T_{PROP} = Bus Propagation Delay (maximum time for complete flight)
T_{SKEW} = Total Clock Skew
T_{SU} = Input Setup Time

@33 MHz	T_{CYC} = 30 nSec	T_{VAL} = 11 nSec	T_{PROP} = 10 nSec	T_{SKEW} = 2 nSec	T_{SU} = 7 nSec
@66 MHz	T_{CYC} = 15 nSec	T_{VAL} = 6 nSec	T_{PROP} = 5 nSec	T_{SKEW} = 1 nSec	T_{SU} = 3 nSec

When defining the maximum length of segments A and B as shown in Figure 26, the calculation must:

- Include an additional trace length segment from the PCI connector to the input device within the expansion PCI card.
- Assume the segment to be 1.5 inch.
- Use trace propagation delay of 150 to 190 ps/in as specified by the PCI standard.

Figure 26. PCI Address/Data Topology

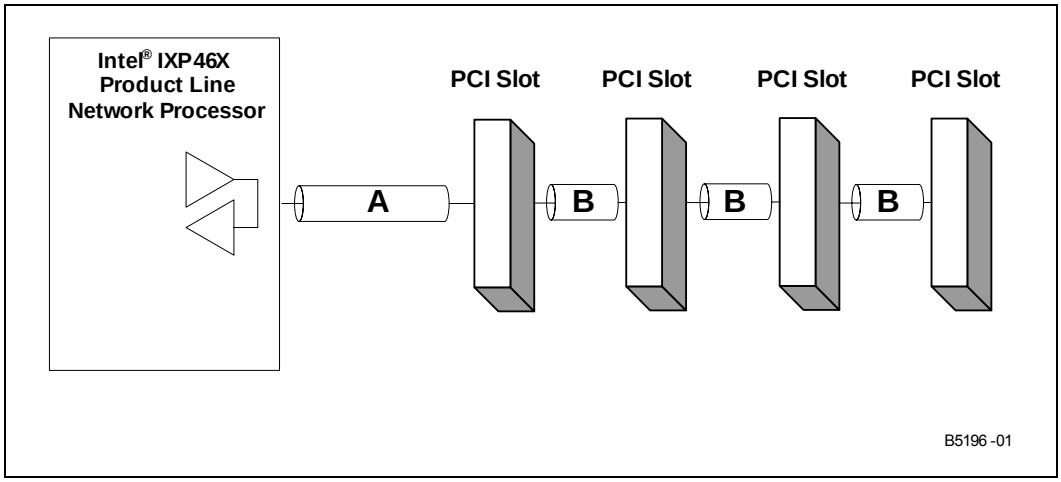


Table 25. PCI Address/Data Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Address/Data
Topology	Daisy Chain
Reference Plane	Ground
Characteristic Trace Impedance	55 Ω ±10%
Nominal Trace Width	5 mils
Nominal Trace Separation	10 mils
Spacing to Other Groups	20 mils
Limit the number of VIAS to 10 per Signal	10

6.3 Clock Distribution

In order to meet timing and avoid clock overloading, it is recommended to use point-to-point clock distribution as shown in Figure 27.

Clock skew between interfacing devices is very critical and must be met. The maximum skew must be measured between any two components. If designing a motherboard, the skew must be measured to the expansion card device and not to the PCI connector. Ensure that clock skew between all devices does not exceed the values in Section 6.2.

Figure 27. PCI Clock Topology

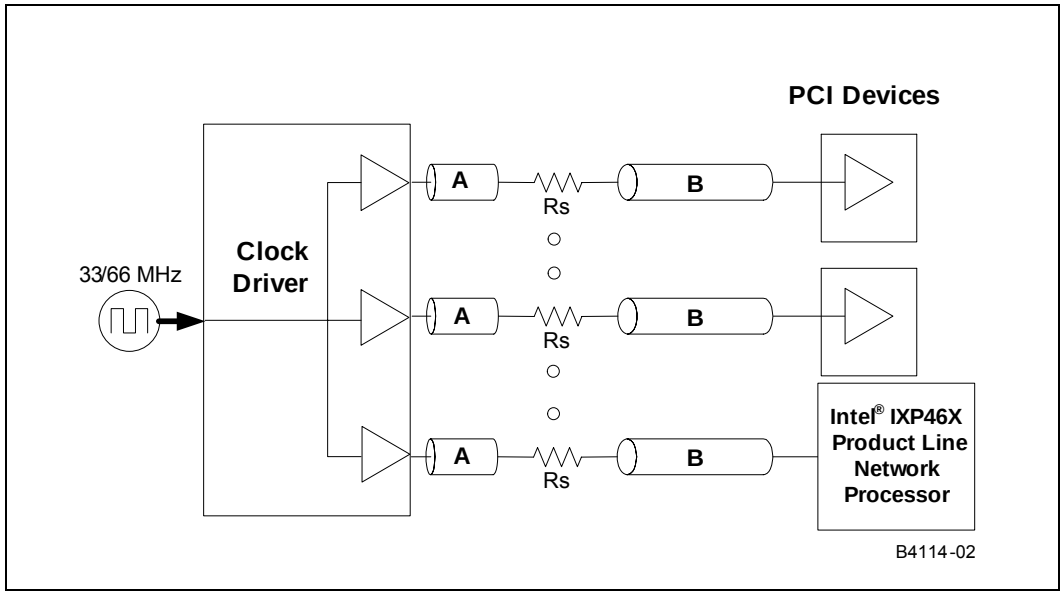


Table 26. PCI Clock Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Clock
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 Ω ±10%
Nominal Trace Width	5 mils
Nominal Trace Separation	10 mils
Spacing to Other Groups	20 mils
Trace length A	Maximum 300 mils
Trace length B	There is no limit as long as the trace length is maintained for each clock and that maximum clock skew is not violated.
Resistor Rs	22 Ω ±10%
Maximum VIAS	6

6.3.1 Trace Length Limits

Maximum trace lengths can be calculated for specific speeds at which the bus is intended to run. Typically, PCI boards with devices that can support up to 66 MHz are designed to function at up to 66 MHz, even if the design is originally intended to run at 33 MHz. This way, if design requirements change to 66 MHz, then timing is met at the higher frequency. In this case, the only additional requirement is to change the clock speed and the expansion bus initial strapping at the EX_ADDR[4] signal. If you are designing your board for 66 MHz and intend it to operate at 33 MHz, ensure that timing equations in Section 6.2 are met at 33 MHz and 66 MHz.

The limitations of the maximum trace length can be calculated with the equations shown in Section 6.2. Solve for T_{PROP} and use it to calculate the maximum trace length. This is a straight-forward calculation, but very critical to meet timing. It is recommended to keep the trace lengths as short as possible and not to exceed T_{PROP}.

Note: For acceptable signal integrity at up to 66 MHz, it is very important to design the PCB board with controller impedance in the range of 55 Ω ±10%.

6.3.2 Routing Guidelines

It is recommended to route signals with respect to an adjacent ground plane. If routing signals over power planes, ensure that the signals are referenced to a single power plane voltage level and not multiple levels. For example, you can route signals over a 3.3 V plane or a 5 V plane, but do not route the same signal over both planes. If signals are routed over split planes, you must connect the splitting planes with 0.01 µF, high-speed capacitors near the signal crossing the split. The capacitors should be placed no more than 0.25 inches from the point at which the signals cross the split.

This manual does not repeat all the guidelines that are already stated in the *PCI Local Bus Specification*, Rev. 2.2, instead you should refer to the specification when designing either a motherboard or an expansion card.

6.3.3 Signal Loading

Shared PCI signals must be limited to one load on each of the PCI slots. Any violation of expansion board or add-on device trace length or loading limits compromises system-signal integrity.

7.0 DDR-SDRAM

7.1 Introduction

This document is intended to be used as a guide for routing DDR, based on the Intel® IXDP465 Development Platform. It contains routing guidelines and simulation results for using x16 Thin Small Outline Package (TSOP) memory devices soldered onto the processor module.

As shown in Figure 28, the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors support two banks of 32-bit wide non-Error Correcting Code (non-ECC) or 40-bit wide (ECC) DDR-266 memory with the ability for single-bit error correction or multi-bit error detection (ECC). The IXP45X/IXP46X network processors support un-buffered DRAM only in densities of 128/256/512 Mbit or 1 Gbit. Table 27 lists the signal groups used for the DDR interface.

In this document, the term IXP45X/IXP46X product line refers to both the IXP46X network processors (with DDR ECC) and IXP45X network processors (without DDR ECC).

Table 27. DDR Signal Groups

Group	Signal Name	Description	No of Single Ended Signals
Clocks	DDRI_CK[2:0]	DDR-SDRAM Differential Clocks	0
	DDRI_CK_N[2:0]	DDR-SDRAM Inverted Differential Clocks	0
Data	DDRI_CB[7:0]	ECC Data	8
	DDRI_DQ[31:0]	Data Bus	32
	DDRI_DQS[4:0]	Data Strobes	5
	DDRI_DM[4:0]	Data Mask	5
Control	DDRI_CKE[1:0]	Clock Enable - one per bank	2
	DDRI_CS_N[1:0]	Chip Select - one per bank	2
Command	DDRI_MA[13:0]	Address Bus	14
	DDRI_BA[1:0]	Bank Select	2
	DDRI_RAS_N	Row Address Select	1
	DDRI_CAS_N	Column Address Select	1
	DDRI_WE_N	Write Enable	1
		Total	73

Figure 28. Processor-DDR Interface

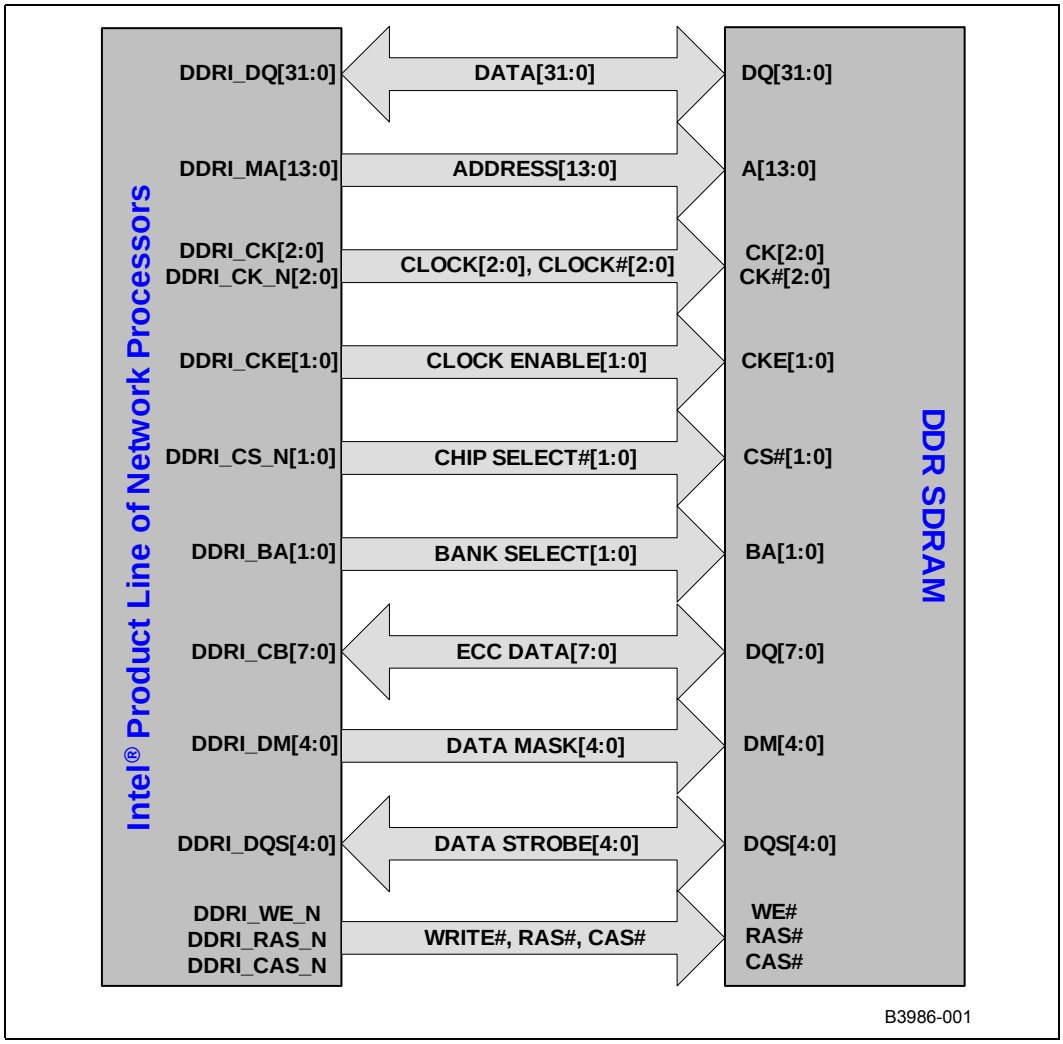


Table 28 provides a list of supported memory configurations that can be implemented for one or two banks. Notice that depending on the number of devices used, loading of the driving signals is affected. The most critical signal affected by the loading is the DDRI_CK (clock output). This signal has a very strict timing requirement defined in the JEDEC standard, therefore signal integrity of this signal is a must. The following table shows how to assign the number of devices per clock line for the various configuration. It also suggest to use a DDR SSTL zero delay clock driver when more than two devices per clock line are connected. From Table 28, any time the word “driver” appears, it is meant to let designers know that for that particular configuration, a clock driver is required. One recommended clock driver can be the Pericom PI6CV855 or a similar device. The Pericom device is highly used in DIMM memory modules that required to deliver clocks to many devices in a single module.

The best approach is to minimize the number of devices used to get the target total memory size required by design.

Besides assigning clock signals (DDRI_CK and DDRI_CK_N) to the memory devices, there are two more requirements, one implemented in hardware (termination) and the other implemented in software (configuration), these requirements are explained as follow:

- It is recommended to properly terminate the clock output signals by the Thevenin terminations scheme as shown in Figure 37. Simulation is recommended for cases that required deviation from the recommended topology, which include series termination and trace impedance.
- It is required to tune the drive strength of the clock driver to properly drive clocks out to loads of one or two memory devices, terminated with Thevenins termination scheme. Follow the recommendations described in Section 7.1.6, “Resistive Compensation Register (Rcomp)” on page 88.

Note that when simulating, the IBIS model representation of signals DDRI_CK[2:0] and DDRI_CK_N[2:0] has been created for the new Rcomp settings described in Section 7.1.6, “Resistive Compensation Register (Rcomp)” on page 88

Table 28. Supported Memory Configurations

DDR Device Density	Device Width	Number of DDR Devices (non-ECC)	Devices per Clock	Number of DDR Devices (ECC)	Devices per Clock	Number of Banks	Total Memory Size
128 Mbit	x8	4	2,2	5	2,2,1	1	64 Mbyte
128 Mbit	x8	8	Driver	10	Driver	2	128 Mbyte
128 Mbit	x16	2	1,1	3	1,1,1	1	32 Mbyte
128 Mbit	x16	4	2,2	6	2,2,2	2	64 Mbyte
256 Mbit	x8	4	2,2	5	2,2,1	1	128 Mbyte
256 Mbit	x8	8	Driver	10	Driver	2	256 Mbyte
256 Mbit	x16	2	1,1	3	1,1,1	1	64 Mbyte
256 Mbit	x16	4	2,2	6	2,2,2	2	128 Mbyte
512 Mbit	x8	4	2,2	5	2,2,1	1	256 Mbyte
512 Mbit	x8	8	Driver	10	Driver	2	512 Mbyte
512 Mbit	x16	2	1,1	3	1,1,1	1	128 Mbyte
512 Mbit	x16	4	2,2	6	2,2,2	2	256 Mbyte
1 Gbit	x8	4	2,2	5	2,2,1	1	512 Mbyte
1 Gbit	x8	8	Driver	10	Driver	2	1 Gbyte
1 Gbit	x16	2	1,1	3	1,1,1	1	256 Mbyte
1 Gbit	x16	4	2,2	6	2,2,2	2	512 Mbyte

Figure 29 shows the DDR memory interface of the IXP45X/IXP46X network processors using x16 devices with Error Correcting Code (ECC). Bank 0 is represented by DDR devices 1, 3, and 5. Bank 1 is represented by DDR devices 2, 4, and 6. Unused data inputs on the ECC devices (5 and 6) are pulled to ground through 10-KΩ resistors.

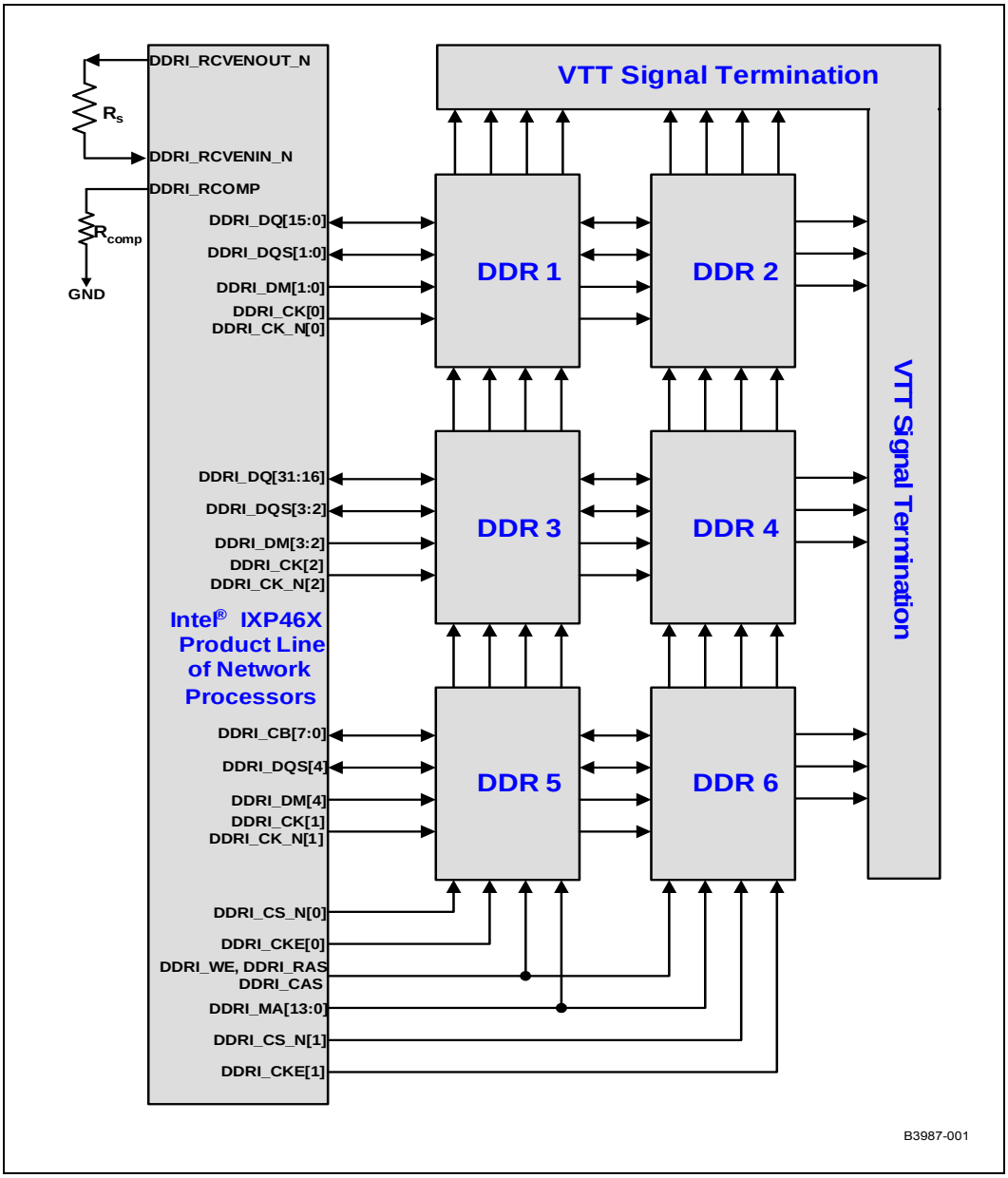
The VTT signal termination used for all signals, except clocks, is a series 60.4-Ω resistor to a 1.25-V DC power supply designed for DDR memory termination. The appropriate value for termination resistance should be verified through simulation for the specific topology as shown in "Simulation Results" on page 90. The supply chosen for this application was the TPS54672 from Texas Instruments*.

The DDRI_RCVENOUT_N signal must be connected to the DDRI_RCVENIN_N signal with a trace which is propagation delay length matched to the average delay of the clock (DDRI_CK[2:0]) plus data (DDRI_DQ[31:0]). A series terminating resistor (R_S) should be used to control overshoot and undershoot, as shown in Figure 49 on page 105.

A resistance value in the 25- to 50-Ω range should be used as it adds minimal propagation delay to the signal without adversely varying from the CLK plus DQ propagation delay average. The appropriate value for termination resistance should be verified through simulation for the specific topology.

The DDRI_RCOMP signal must be terminated through a 20-Ω, 1%, 0.1-W resistor (R_{comp}) to ground. This allows the DDR controller to make temperature and process adjustments.

Figure 29. Processor-DDR Interface: x16 Devices with ECC



7.1.1 Selecting VTT Power Supply

Selecting the minimum power requirement for VTT supply is a simple calculation that varies depending on the resistive value of RVTT terminating resistors. Since all RVTT has the same value, the power calculation becomes a simple, current times voltage times the number of terminating resistors used. Figure 30 shows an example of one terminating network, for which the following equation can be solved for the unknown:

Vout = 0 or 2.5V

VTT=1.25V

RVTT= 60Ω (we can assume this value)

N = 73 (from Table 27 obtain the total number of RVTT resistors)

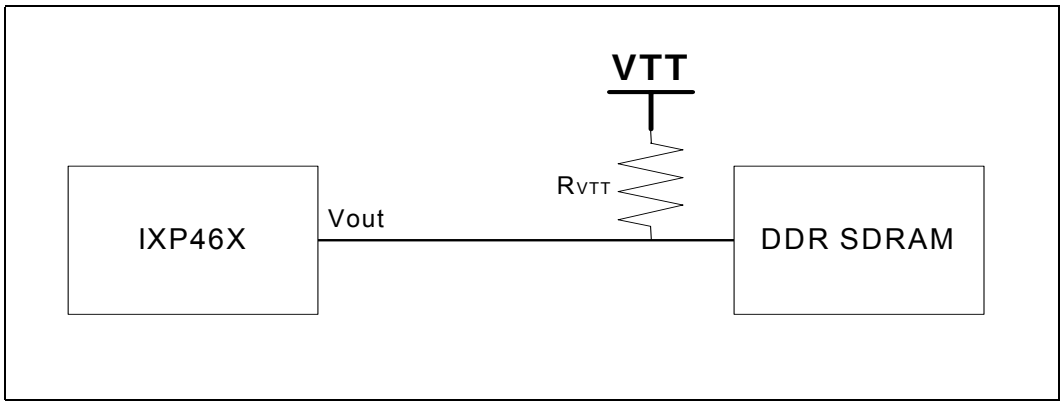
P = (V x I) x N= (Vout (- or +) VTT) x (VTT/RVTT) x N

P = (2.5V-1.25V) x (1.25V/60Ω) x 73

P = **1.9** Watt. Allow a 25% overhead. P = 1.9W + 1.9W x 0.25 = **2.38** Watt

It is very important to allow some overhead for the VTT power supply, just like any other power distribution allow some overhead in case the value of RVTT or simply for inrush current. The following figure shows the diagram of the current paths for the above equation.

Figure 30. VTT Terminating Circuitry



7.1.2 Signal-Timing Analysis

Figure 31. DDR Command and Control Setup and Hold

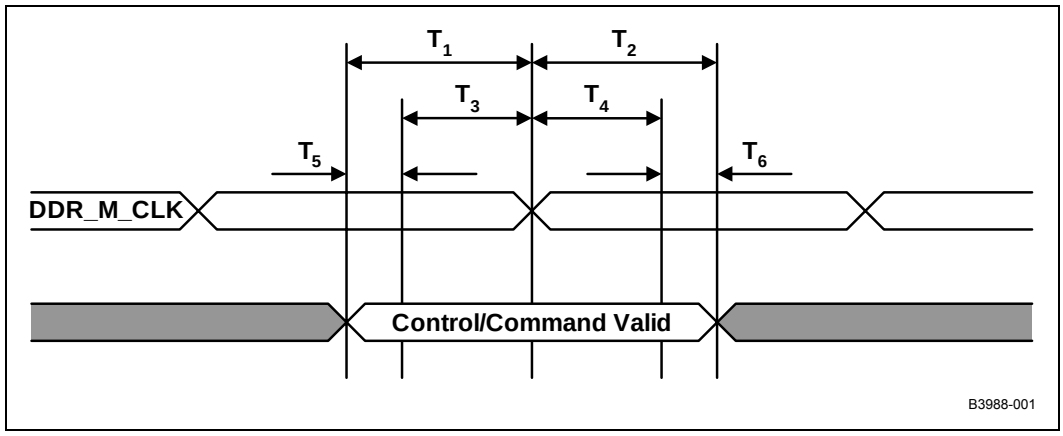


Table 29. DDR Command and Control Setup and Hold Values

Symbol	Parameter	Min	Max	Units	Notes
T_1	Output of IXP45X/IXP46X network processors valid for Command and Control signals prior to the transition of DDR_M_CLK	1.5		ns	1
T_2	Output hold time of IXP45X/IXP46X network processors for Command and Control signals after the transition of DDR_M_CLK	1.5		ns	1
T_3	Required Command and Control input setup time at DDR memory device	0.9		ns	1
T_4	Required Command and Control input hold time at DDR memory device	0.9		ns	1
T_5	Allowable setup time difference between IXP45X/IXP46X network processors Command and Control output and setup time required by DDR memory device		0.6	ns	1
T_6	Allowable hold time difference between IXP45X/IXP46X network processors Command and Control output and hold time required by DDR memory device		0.6	ns	1

Notes:
1. DDR_M_CLK represents the combined clock signal for DDRI_CK and DDRI_CK_N.

Figure 32. DDR Data to DQS Read Timing Parameters

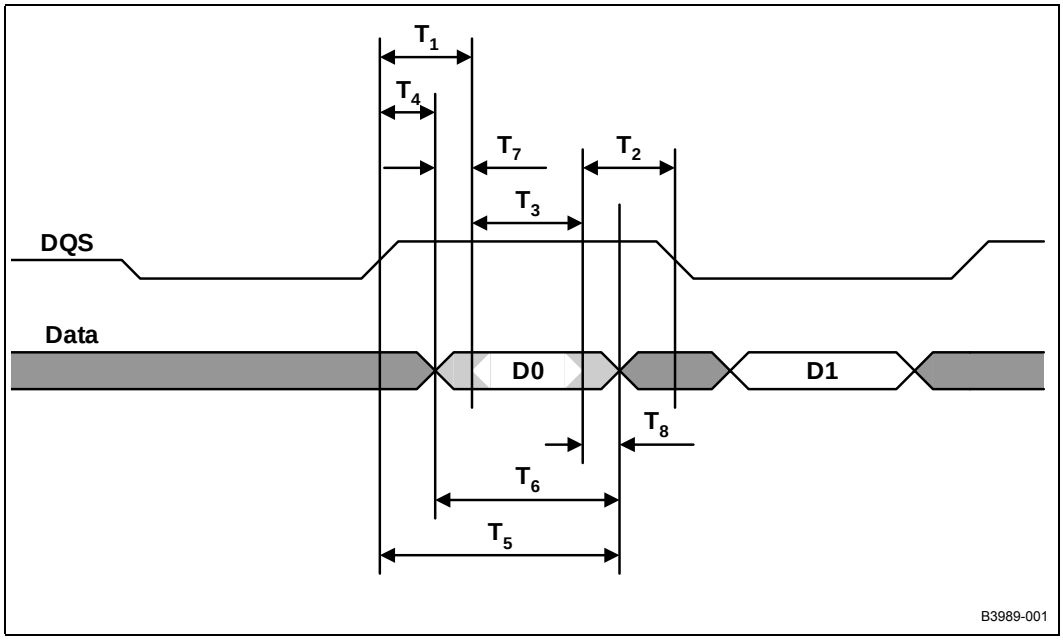


Table 30. DDR Data to DQS Read Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
T_1	IXP45X/IXP46X network processors delay for data group valid after any edge of DQS		0.75	ns	1
T_2	IXP45X/IXP46X network processors guaranteed time before data group begins to transition invalid prior to DQS		1.0	ns	1
T_3	Data valid window for IXP45X/IXP46X network processors	2.0		ns	1
T_4	DQ-DQS skew, DQS to last data group signal going valid from DDR memory device		0.5	ns	1
T_5	DQ-DQS hold, DQS to first data group signal going non-valid from DDR memory device	3.0		ns	1
T_6	Data valid window from DDR memory device	2.5		ns	1
T_7	Allowable data group to DQS difference for data going valid (T_1 - T_4)		0.25	ns	1
T_8	Allowable data group to DQS difference for data going invalid (T_5 - T_3 - T_1)		0.25	ns	1

Notes:
1. Data group signals consist of DDRI_DM[4:0], DDRI_DQ[31:0], and DDRI_CB[7:0].

Figure 33. DDR-Data-to-DQS-Write Timing Parameters

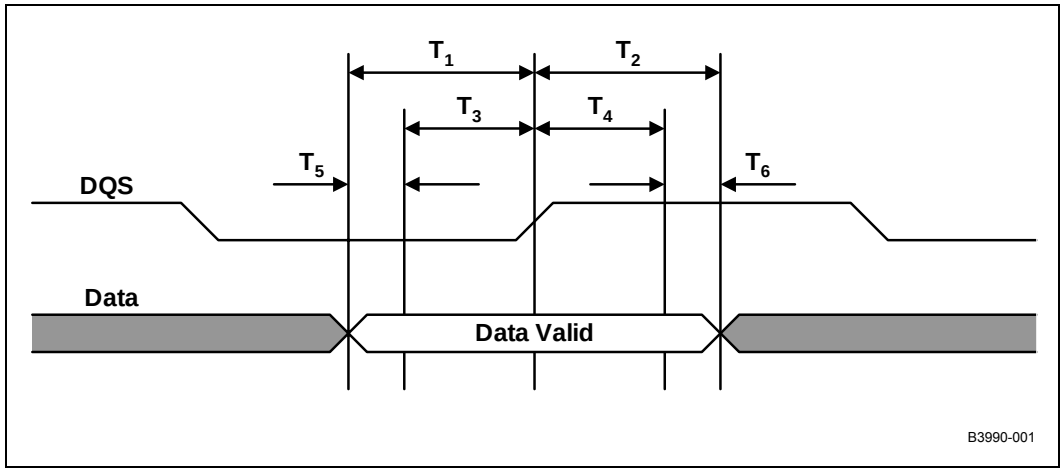


Table 31. DDR Data to DQS Write Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
T_1	IXP45X/IXP46X network processors output valid for data group signals prior to the transition of DQS	1.0		ns	1
T_2	IXP45X/IXP46X network processors output hold time for data group signals after the transition of DQS	1.0		ns	1
T_3	Required data group input setup time at DDR memory device	0.5		ns	1
T_4	Required data group input hold time at DDR memory device	0.5		ns	1
T_5	Allowable setup time difference between IXP45X/IXP46X network processors data group output and setup time required by DDR memory device		0.5	ns	1
T_6	Allowable hold time difference between IXP45X/IXP46X network processors data group output and hold time required by DDR memory device		0.5	ns	1

Notes:
1. Data group signals consist of DDRI_DM[4:0], DDRI_DQ[31:0], and DDRI_CB[7:0]

Figure 34. DDR-Clock-to-DQS-Write Timing Parameters

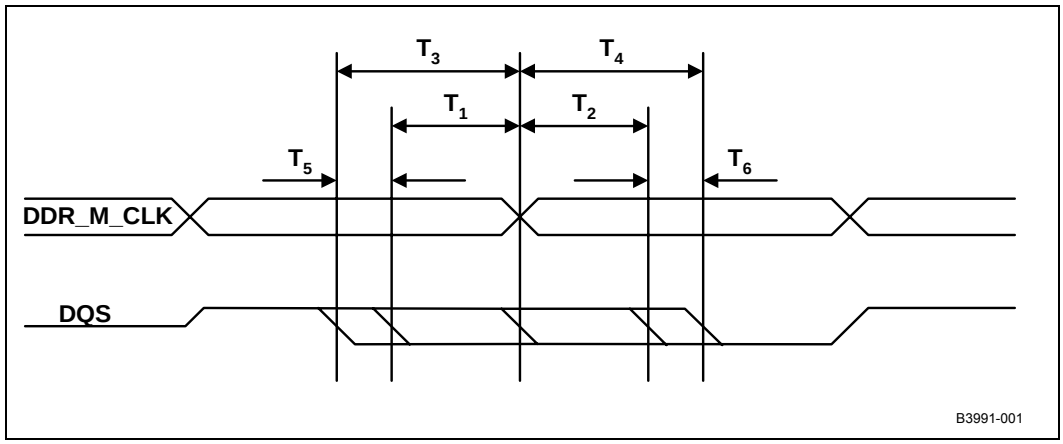


Table 32. DDR-Clock-to-DQS-Write Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
T_1	IXP45X/IXP46X network processors output valid for DDRI_DQS prior to the transition of DDR_M_CLK		1.4	ns	1
T_2	IXP45X/IXP46X network processors output hold time for DDRI_DQS after the transition of DDR_M_CLK		1.0	ns	1
T_3	Required write command to DQS latching transition at DDR memory device (early transition)		1.875	ns	1
T_4	Required write command to DQS latching transition at DDR memory device (late transition)		1.875	ns	1
T_5	Allowable difference between IXP45X/IXP46X network processors DDR_M_CLK output and first DQS transition (early transition)		0.475	ns	1
T_6	Allowable difference between IXP45X/IXP46X network processors DDR_M_CLK output and first DQS transition (late transition)		0.875	ns	1

Notes:
1. DDR_M_CLK represents the combined clock signal for DDR_CK and DDR_CK_N.

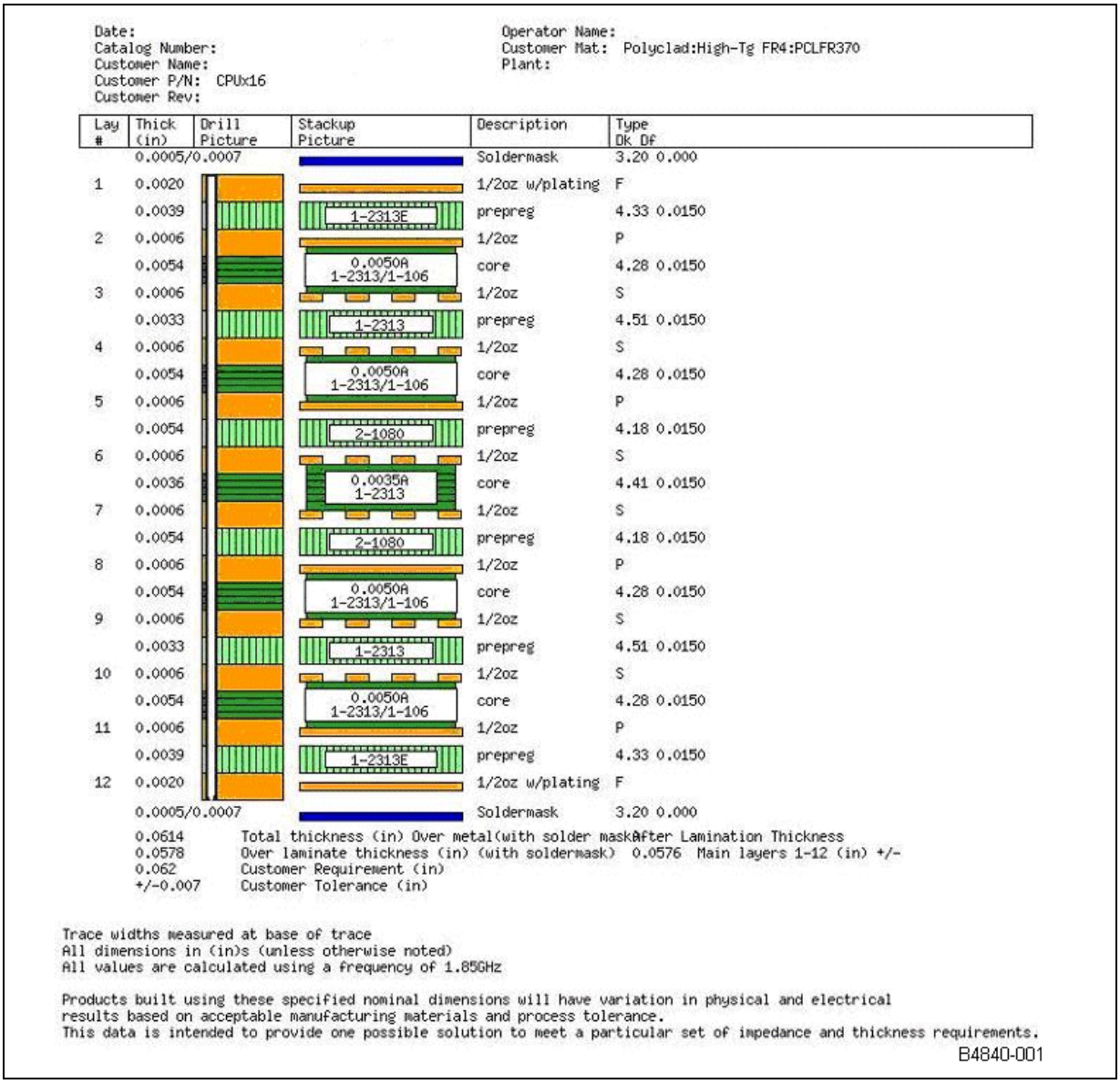
7.1.3 Printed Circuit Board Layer Stackup

The layer stackup used for the IXDP465 platform x16 Processor Module is shown in Figure 35 on page 85. The example is for a 12-layer, printed circuit board with eight signal layers and four plane layers.

- Layers 5 and 8 are used as digital ground planes
- Layers 2 and 11 are used as split planes for the different voltage references (3.3 V and 2.5 V).

Details on the voltage reference layout are available in the CAD database or Gerber files database for the IXDP465 platform x16 Processor Module.

Figure 35. Printed Circuit Board Layer Stackup



7.1.4 Printed Circuit Board Controlled Impedance

Controlled impedance for each layer of the IXDP465 platform x16 Processor Module is necessary to provide proper matching from driver to receiver(s) for improved signal integrity and higher reliability in the signal analysis results obtained through simulation. As indicated in Figure 36 on page 86, Layers 4, 6, 7, and 9 are impedance controlled for clock routing (60-Ω, single-ended' 120-Ω, differential) as well as all other DDR signals (50 Ω, single-ended). Layers 3 and 10 are also impedance controlled for 50-Ω, single-ended traces.

Figure 36. Printed Circuit Board Controlled Impedance

Date:
Catalog Number:
Customer Name:
Customer P/N: CPUx16
Customer Rev:

Operator Name:
Customer Mat: Polyclad:High-Tg FR4:PCLFR370
Plant:

Impedance Constraint Information

Imp #	Imp Type Name	Picture	Aff Lyr	Line Width	Design Width	Cntr-to -Cntr	Ref Plane Top	Ref Plane Bot	Per in tpd ps Atten dB	Rdc Rac ohms	L pH G umhos C pF	Targ ohms	Predict ohms
1	EC Stripline		4	0.0034 0.0034	0.0035 0.0035	0.014	2	5	175 0.28	0.359 2.180	11019 484 2.8	120 + / - 12	120.20
2	Stripline		4	0.0038	0.004		2	5	175 0.28	0.319 2.014	10541 505 2.9	60 + / - 6	60.30
3	Stripline		3	0.0057	0.0057		2	5	175 0.26	0.208 1.504	8786 608 3.5	50 + / - 5	50.21
4	Stripline		4	0.0057	0.0057		2	5	175 0.26	0.348 2.064	10960 478 2.7	50 + / - 5	50.21
5	EC Stripline		6	0.0035 0.0035	0.0035 0.0035	0.014	5	8	173 0.27	0.348 2.064	10960 478 2.7	120 + / - 12	120.38
6	Stripline		6	0.004	0.004		5	8	173 0.27	0.302 1.871	10384 504 2.9	60 + / - 6	59.96
7	Stripline		6	0.0059	0.0059		5	8	173 0.25	0.200 1.401	8694 602 3.5	50 + / - 5	50.18
8	EC Stripline		7	0.0035 0.0035	0.0035 0.0035	0.014	5	8	173 0.27	0.348 2.064	10960 478 2.7	120 + / - 12	120.38
9	Stripline		7	0.004	0.004		8	5	173 0.27	0.302 1.871	10384 504 2.9	60 + / - 6	59.96
10	Stripline		7	0.0059	0.0059		8	5	173 0.25	0.200 1.401	8694 602 3.5	50 + / - 5	50.18
11	EC Stripline		9	0.0034 0.0034	0.0035 0.0035	0.014	11	8	175 0.28	0.359 2.180	11019 484 2.8	120 + / - 12	120.20
12	Stripline		9	0.0038	0.004		11	8	175 0.28	0.319 2.014	10541 505 2.9	60 + / - 6	60.30
13	Stripline		9	0.0057	0.0057		11	8	175 0.26	0.208 1.504	8786 608 3.5	50 + / - 5	50.21
14	Stripline		10	0.0057	0.0057		11	8	175 0.26	0.208 1.504	8786 608 3.5	50 + / - 5	50.21

Trace widths measured at base of trace
All dimensions in (in)s (unless otherwise noted)
All values are calculated using a frequency of 1.85GHz

Products built using these specified nominal dimensions will have variation in physical and electrical results based on acceptable manufacturing materials and process tolerance.
This data is intended to provide one possible solution to meet a particular set of impedance and thickness requirements.

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7.1.5 Timing Relationships

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width, spacing geometries, and typical routed lengths for each signal group. These parameters are recommended to achieve optimal signal integrity and timing.

All signal groups are length matched to the DDR clocks. The clocks on the processor module are length matched to within ±10 mils of each other. Once this overall clock length for any given DDR differential clock is determined, the command and control signals can be routed to within the timing specified. A simple summary of the timing results for each signal group is provided Table 33 on page 87.

Control/Command Group to Clock Summary:

- The maximum allowable difference from any command/control signal to the clock is ±0.6 ns.
  - Figure 31 on page 81
  - Table 29 on page 81

Data Group to Strobe Summary:

- The more restrictive data group to strobe timing occurs for read operations
  - Table 30 on page 82
  - Table 31 on page 83
- The maximum allowable difference from any data group signal to the strobe is ±0.25 ns.
  - Figure 32 on page 82
  - Table 30 on page 82

Strobe to Clock Summary:

- The maximum allowable difference from any data strobe signal to the clock is -0.475 ns to +0.875 ns
  - Figure 34 on page 83
  - Table 32 on page 84

These are absolute maximum ratings for length mismatch based in ideal printed board conditions (exact signal propagation delays, ideal signal integrity with no reflections or settling, zero rise/fall times, etc.) In order to compensate for these non-ideal conditions, more restrictive length matching conditions should be used based on signal integrity analysis and simulation to provide a buffer zone and avoid possible variations in silicon or printed circuit board manufacture.

Table 33. Timing Relationships

Signal Group	Absolute Minimum Length	Absolute Maximum Length
Control to Clock	Clock – 600 ps	Clock + 600 ps
Command to Clock	Clock – 600 ps	Clock + 600 ps
Data to Strobe	Strobe – 250 ps	Strobe + 250 ps
Strobe to Clock	Clock – 475 ps	Clock + 875 ps

In addition to any trace length differentials which must be considered between signal groups, differences in the package length between signals should be considered when determining the total propagation delay of the signals. When using the IBIS model for signal analysis, package characteristics are included in the simulation results.

7.1.6 Resistive Compensation Register (Rcomp)

Critical signals such as the differential clock drivers used for driving clock out to memory devices is very critical. The JEDEC standard has a very critical requirement for the crossing of the differential clock signals which required proper termination and drive strength of the signals. Therefore, in order to comply with this requirement, two recommendations have been made.

- Use Thevenin termination as shown in Figure 37. It is important that the series termination and impedance matching is strictly follow.
- Configuration of the Rcomp circuit.

The steps to follow and the order in which they need to occur to configure Rcomp are described in section “DDRI SDRAM Initialization” of the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*. Here is a recap of the two registers that are required to be overwritten with the new value:

- Override default value of register DDR_RCOMP_CSR3 with 0x0000 1000Hex
- Override default value of register DDR_DRIVE3 with 0x0002 08F0Hex

Note that this configuration only affects the SDRAM differential clock driver for all three outputs DDRI_CK[2:0] and DDRI_CK_N[2:0].

Refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual* for the complete sequence of steps to follow to configure the SDRAM DDRI memory module.

Note that when simulating, the IBIS model representation of signals DDRI_CK[2:0] and DDRI_CK_N[2:0] has been created for the new Rcomp settings described in this section.

7.1.7 Routing Guidelines

7.1.7.1 Clock Group

The clock signal group includes the differential clock pairs DDRI_CK[2:0] and DDRI_CK_N[2:0].

Here are some tips on how to route the differential clock pairs:

- Ensure that DDR clocks are routed on a single internal layers, except for pin escapes.
- A ground plane must be adjacent to the layer where the signals are routed.
- Minimize the number of vias used, but ensure that the same number of vias are used in the positive and negative trace.
- It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks.
- Traces must be routed for differential mode impedance of 120 Ω.
- Surface layer routing should be minimized (top or bottom layers).
- It is recommended to perform pre- and post-layout simulation.

Table 34 provides routing guidelines for signals within this group.

Table 34. Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group Members	DDRI_CK[2:0] and DDRI_CK_N[2:0]
Topology	Differential Pair Point to Point (1 Driver, 2 Receivers)
Single Ended Trace Impedance (Z_o)	60 Ωs
Differential Mode Impedance (Z_{diff})	120 Ωs
Nominal Trace Width[1]	Internal (Strip Line) 3.5 mils, External (Micro Strip) 5 mils
Nominal Pair Spacing (edge to edge) [2]	Internal (Strip Line) 10.5 mils, External (Micro Strip) 10 mils
Minimum Pair to Pair Spacing	Any layer 20mils
Minimum Spacing to Other DDR Signals	20.0 mils
Minimum Spacing to non-DDR Signals	25.0 mils
Maximum Via Count	4 per trace 8 per differential pair
DDRI_CK to DDRI_CK_N Length Matching	Match total length to +/- 10 mils between clocks

Notes:
1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

7.1.7.2 Data, Command, and Control Groups

The data, command, and control signal groups include all signals other than the clock group signals. The groups should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all signals. Surface layer routing should be minimized. The following table provides routing guidelines for signals within these groups.

Table 35. Data, Command, and Control Group Routing Guidelines

Parameter	Definition
Signal Group Members	DDRI_CB[7:0], DDRI_DQ[31:0], DDRI_DQS[4:0], DDRI_DM[4:0], DDRI_CKE[1:0], DDRI_CS_N[1:0], DDRI_MA[13:0], DDRI_BA[1:0], DDRI_RAS_N, DDRI_CAS_N, DDRI_WE_N
Topology	Single-Ended, Point-to-Point (1 Driver, 6 Receivers max)
Single Ended Trace Impedance (Z_o)	50 Ω
Nominal Trace Width[1]	Layers 3, 4, 6, 7, 9, and 10: 5.7 mils
Minimum Spacing to DDR Clock Signals	20.0 mils
Minimum Spacing to other DDR Signals	10.0 mils
Minimum Spacing to non-DDR Signals	25.0 mils
Maximum Via Count	6 per signal
Length Matching	See Table 33 on page 87

Notes:
1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.

7.2 Simulation Results

This section contains the simulation results for each of the DDR signal groups. Each of the signal groups may have different overall topologies based on the number of banks and ECC usage.

Each signal group simulated below uses a two-bank, 32-bit data bus with ECC based on 16-bit DDR devices.

7.2.1 Clock Group

The clock signal group includes the differential clock pairs DDRI_CK[2:0] and DDRI_CK_N[2:0]. The following simulation was constructed for the 2 bank x16 device configuration where each clock would have two receivers.

Table 36 identifies the transmission line lengths for the clock topology shown in Figure 37 on page 91. These lengths were chosen as realistic goals given the IXP45X/ IXP46X network processors to DDR device body to body separation of no more than 500 mils.

Table 36. Clock Group Topology Transmission Line Characteristics

Transmission Line	Length
TL1 (T_{pd} = 175 ps/in)	~100 mils
TL2 (T_{pd} = 175 ps/in)	~1300 mils
TL3 (T_{pd} = 175 ps/in)	~50 mils
TL4, TL5 (T_{pd} = 175 ps/in)	~300 mils

Figure 37. DDR Clock Topology: Two-Bank x16 Devices

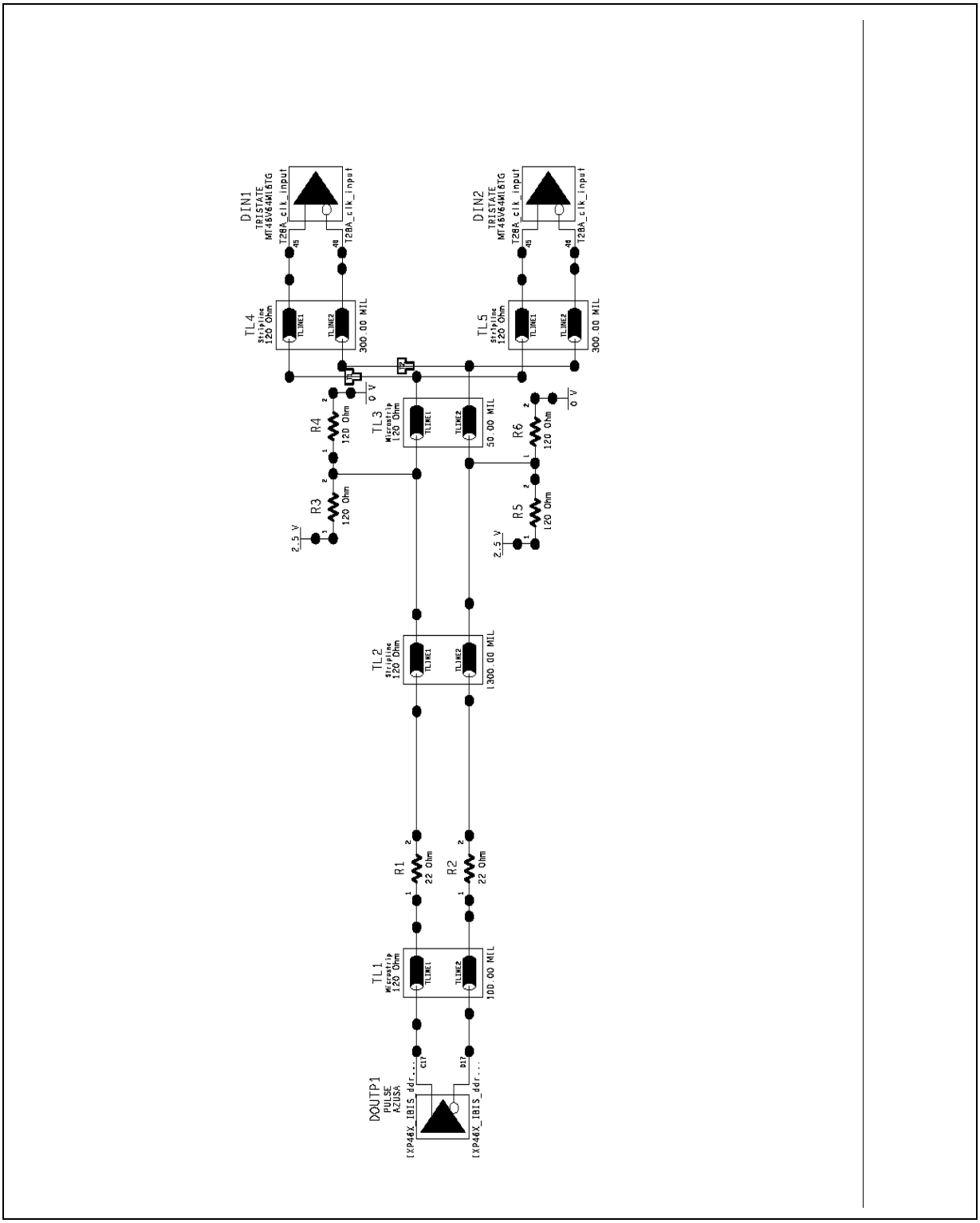
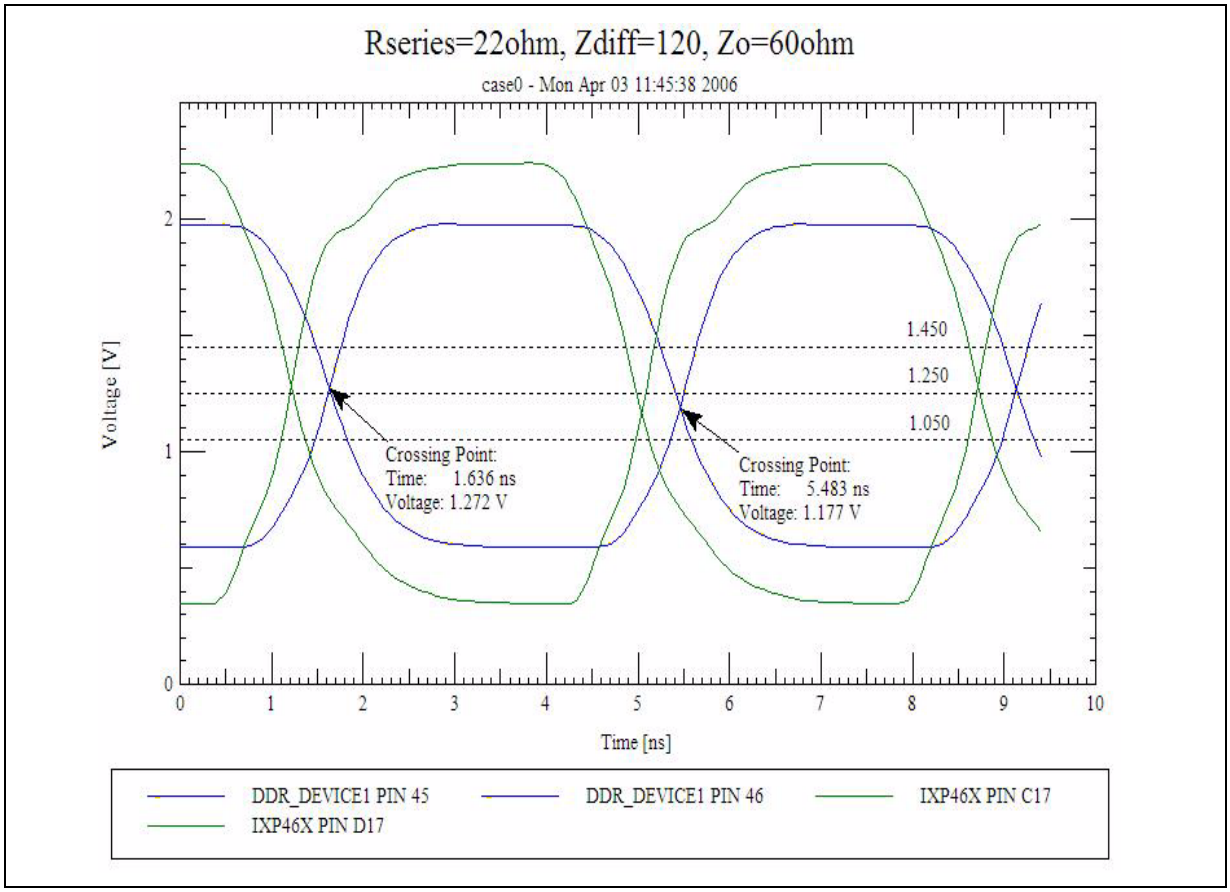


Figure 38. DDR Clock Simulation Results: Two-Bank x16 Devices



The differential-clock-circuit simulation in Figure 38 shows that the voltage waveform meets the DDR device input voltage requirements. The crossing point for the clock input must occur between $V_{ix(min)}$ =1.05 V and $V_{ix(max)}$ =1.45 V and have a minimum peak to peak swing of 700 mV. The receiver input waveform must also not exceed a maximum voltage of $V_{in(max)}$ =2.8 V or the minimum voltage of $V_{in(min)}$ =-0.3 V.

Waveform results for device DDR_DEVICE2 is not shown as it is identical to that of device DDR_DEVICE1 due to symmetry. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

7.2.2 Data Group

The data signal group includes the signals DDRI_CB[7:0], DDRI_DQ[31:0], DDRI_DQS[4:0], and DDRI_DM[4:0]. The following simulations were constructed for the 2 bank x16 device configuration where each signal would have two receivers where only one is active for a read or write.

Table 37 identifies the transmission line lengths for the data (DDRI_DQ5) topology shown in Figure 39 on page 94. These lengths were chosen as realistic goals given the IXP45X/IXP46X network processors to DDR device body to body separation of no more than 500 mils.

Table 37. Data Group Topology Transmission Line Characteristics

Transmission Line	Length
TL1 (T_{pd} = 175 ps/in)	~600 mils
TL2 (T_{pd} = 175 ps/in)	~50 mils
TL3 (T_{pd} = 175 ps/in)	~1,100 mils
TL4 (T_{pd} = 175 ps/in)	~50 mils
TL5, TL6 (T_{pd} = 175 ps/in)	~300 mils
TL7, TL8 (T_{pd} = 175 ps/in)	~800 mils

Figure 39. DDR Data Topology: Two-Bank x16 Devices

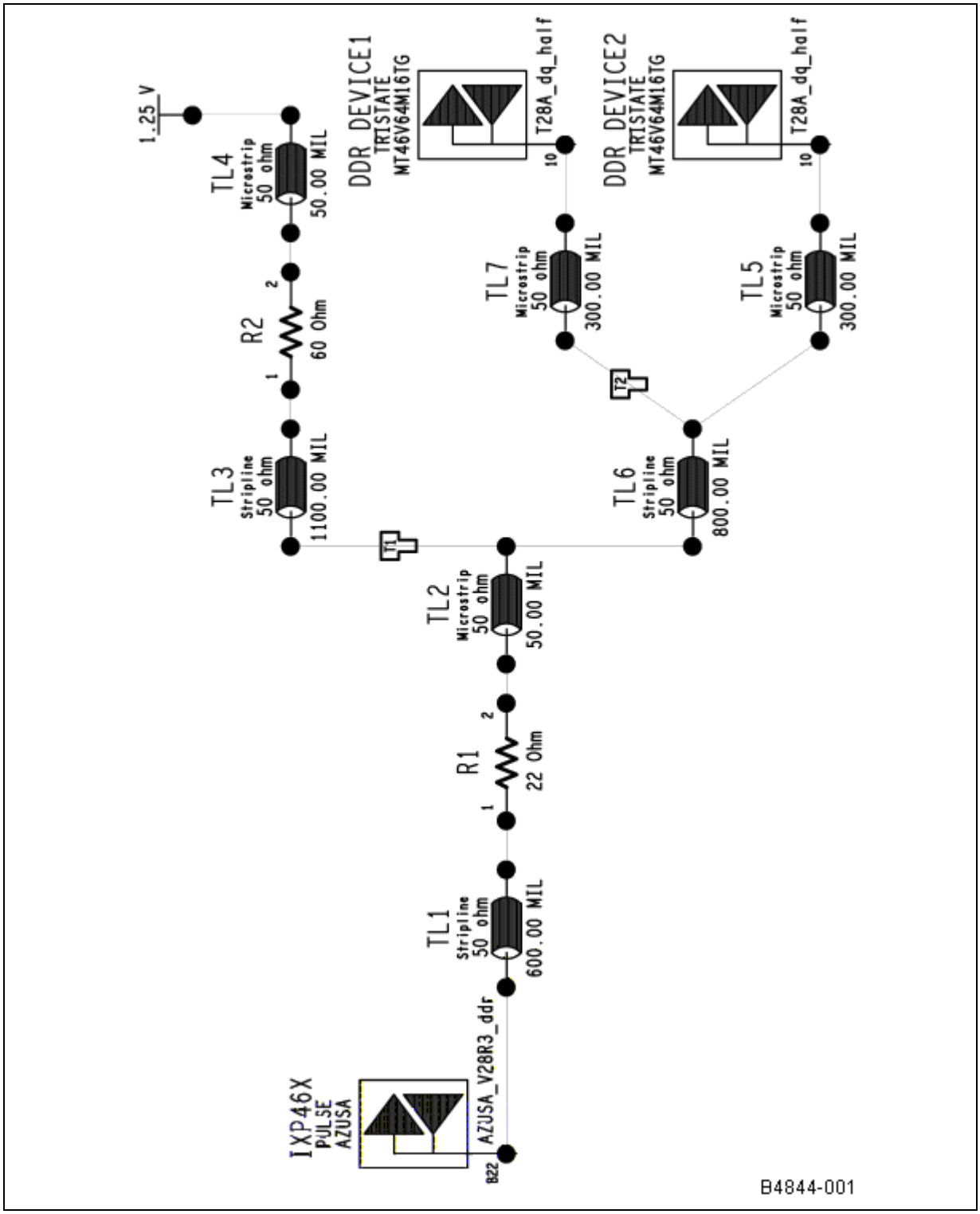
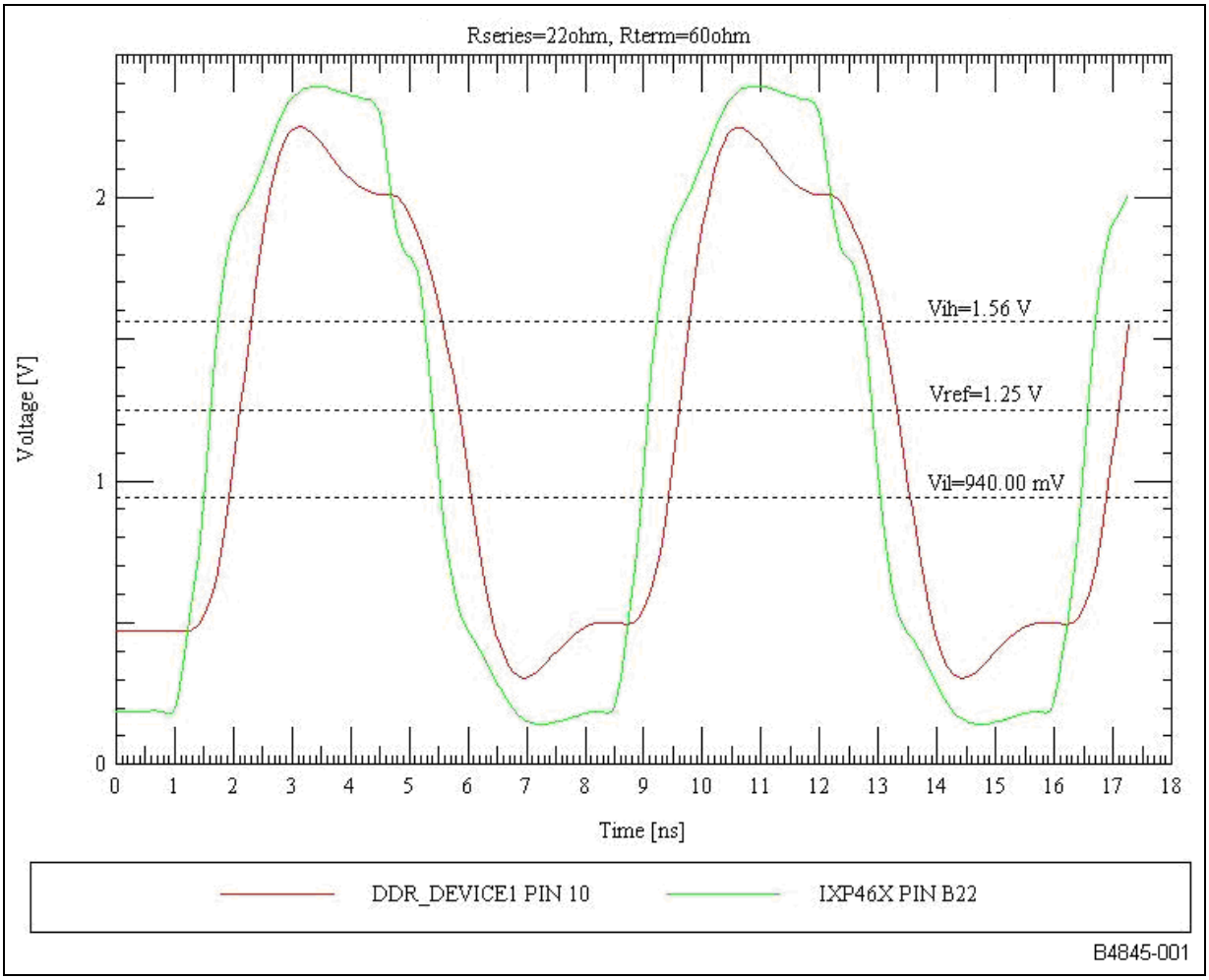


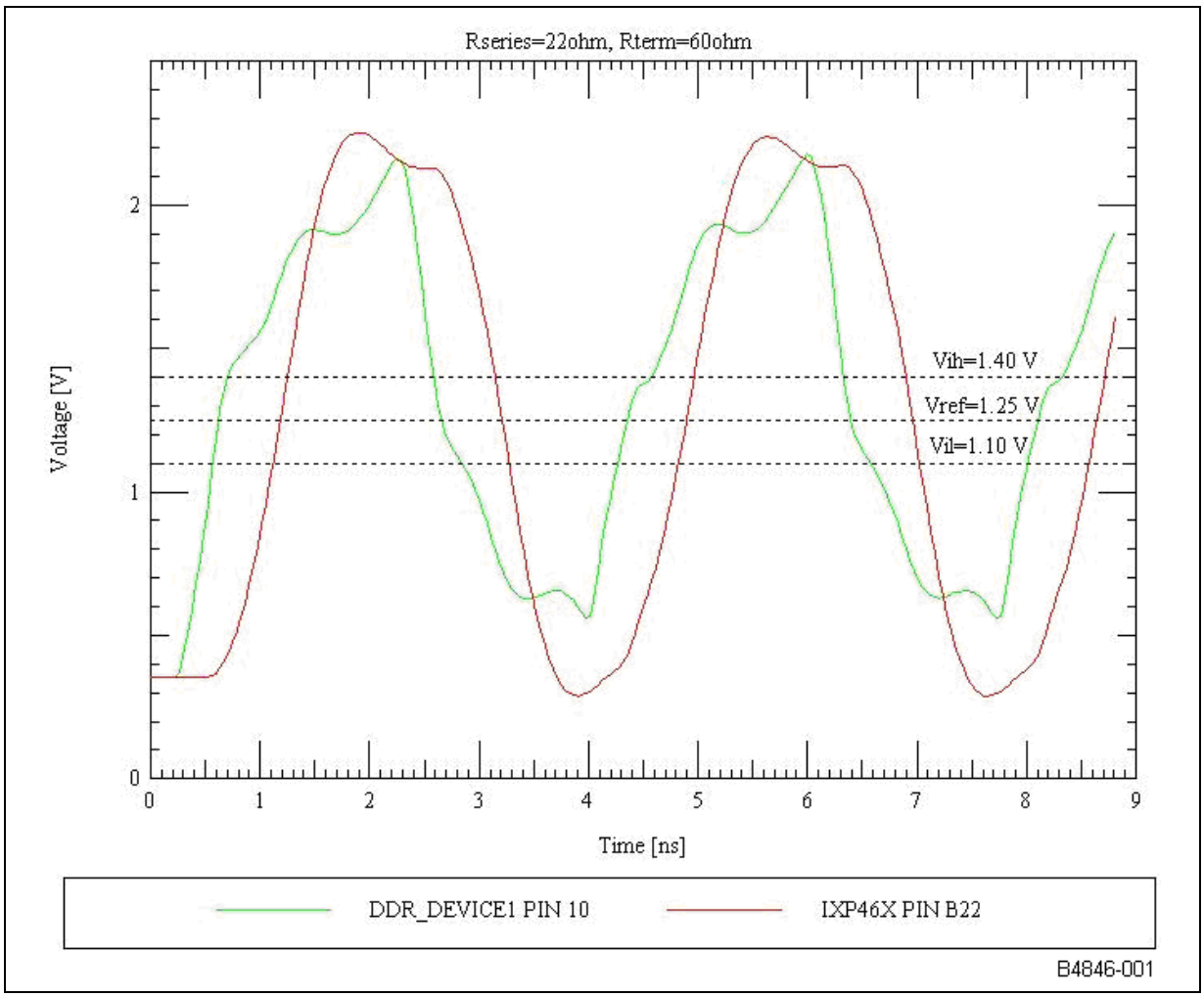
Figure 40. DDR Data Write Simulation Results: Two-Bank x16 Devices



The data-circuit simulation results in Figure 40 show that the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.310 or 940 mV and $V_{ih(min)}$ of V_{ref} + 0.310 or 1.56 V are easily achieved at the receiver (DDR_DEVICE1). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ =-0.3 V.

Waveform results for DDR_DEVICE2 are not shown as it is identical to that of device DDR_DEVICE1 due to symmetry. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

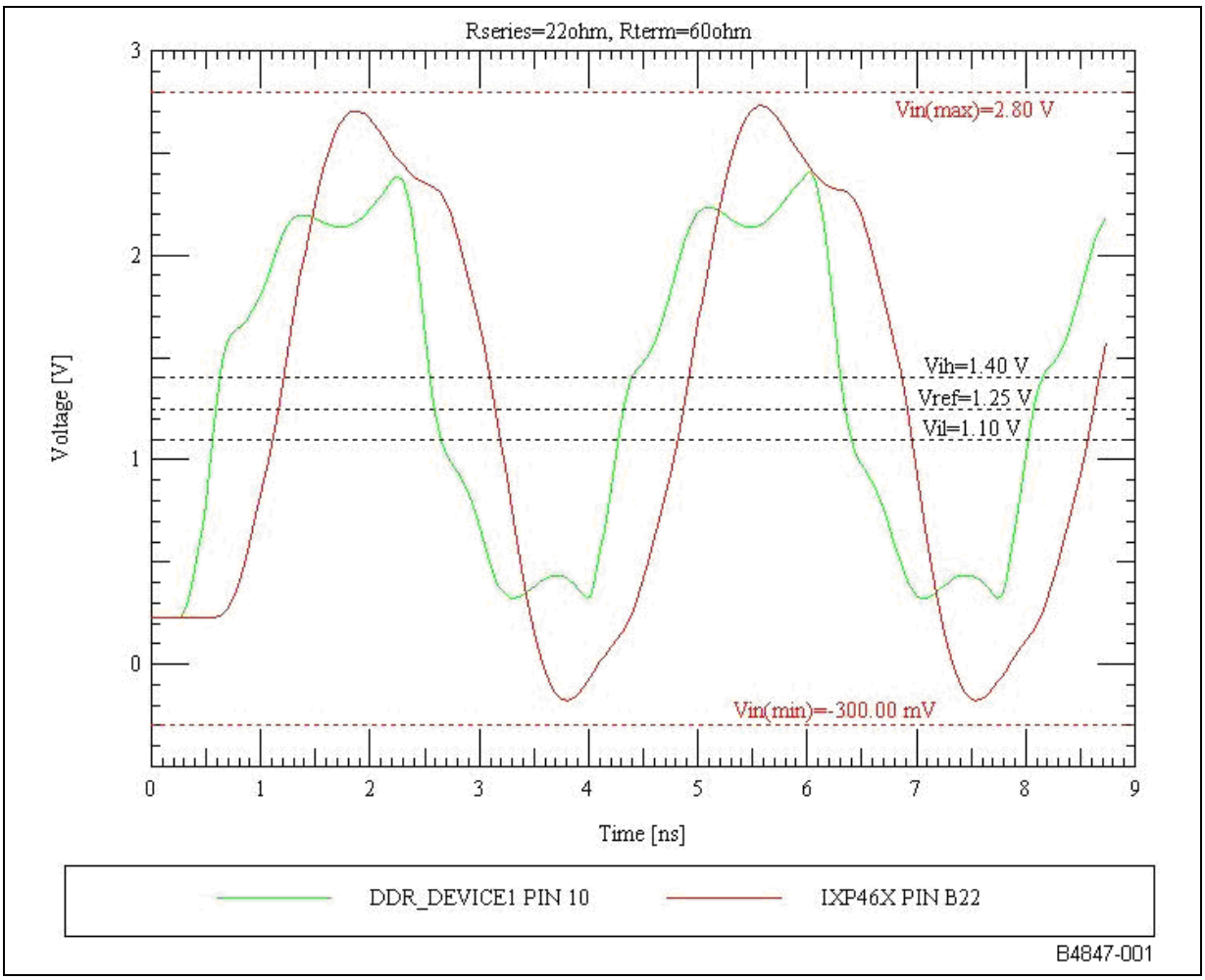
Figure 41. DDR Data Read Simulation Results: Two-Bank x16 Devices (Reduced Drive Strength)



The simulation results in Figure 41 are for the data circuit with a DDR device using reduced drive strength and shows that the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.150 or 1.10 V and $V_{ih(min)}$ of V_{ref} + 0.150 or 1.40 V are easily achieved at the receiver (IXP45X/IXP46X network processors). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ =2.8 V or the minimum voltage of $V_{in(min)}$ =-0.3 V.

Waveform results for DDR_DEVICE2 are not shown as it is not relevant when reading from DDR_DEVICE1. Due to the symmetry of the topology, waveform results when reading from DDR_DEVICE2 would be identical to those when reading from DDR_DEVICE1. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

Figure 42. DDR Data Read Simulation Results: Two-Bank x16 Devices (Full Drive Strength)



The simulation results in Figure 42 are for the data circuit with a DDR device using full drive strength and show that the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.150 or 1.10 V and $V_{ih(min)}$ of V_{ref} + 0.150 or 1.40 V are easily achieved at the receiver (IXP45X/IXP46X network processors). However, the receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V and the waveforms at the IXP45X/IXP46X network processors are close to these limits. A larger series resistor could be used to attenuate the signal, but the results of doing so might have an adverse effect on write operations.

Waveform results for DDR_DEVICE2 are not shown as it is not relevant when reading from DDR_DEVICE1. Due to the symmetry of the topology, waveform results when reading from DDR_DEVICE2 would be identical to those when reading from DDR_DEVICE1. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

7.2.3 Control Group

The control signal group includes the signals DDRI_CS[1:0] and DDRI_CKE[1:0]. The following simulations were constructed for the 2 bank x16 device configuration where each signal would have three receivers.

Table 38 identifies the transmission line lengths for the chip select (CS0) topology shown in Figure 43 on page 98. These lengths were chosen as realistic goals given the IXP45X/IXP46X network processors to DDR body to body separation of no more than 500 mils.

Table 38. Control Group Topology Transmission Line Characteristics

Transmission Line	Length
TL1 (T_{pd} = 175 ps/in)	~ 600 mils
TL2 (T_{pd} = 175 ps/in)	~ 50 mils
TL3 (T_{pd} = 175 ps/in)	~ 1,100 mils
TL4 (T_{pd} = 175 ps/in)	~ 50 mils
TL5, TL6, TL7 (T_{pd} = 175 ps/in)	~ 800 mils
TL8, TL9, TL10 (T_{pd} = 175 ps/in)	~ 300 mils

Figure 43. DDR Control (CS0) Topology: Two-Bank x16 Devices

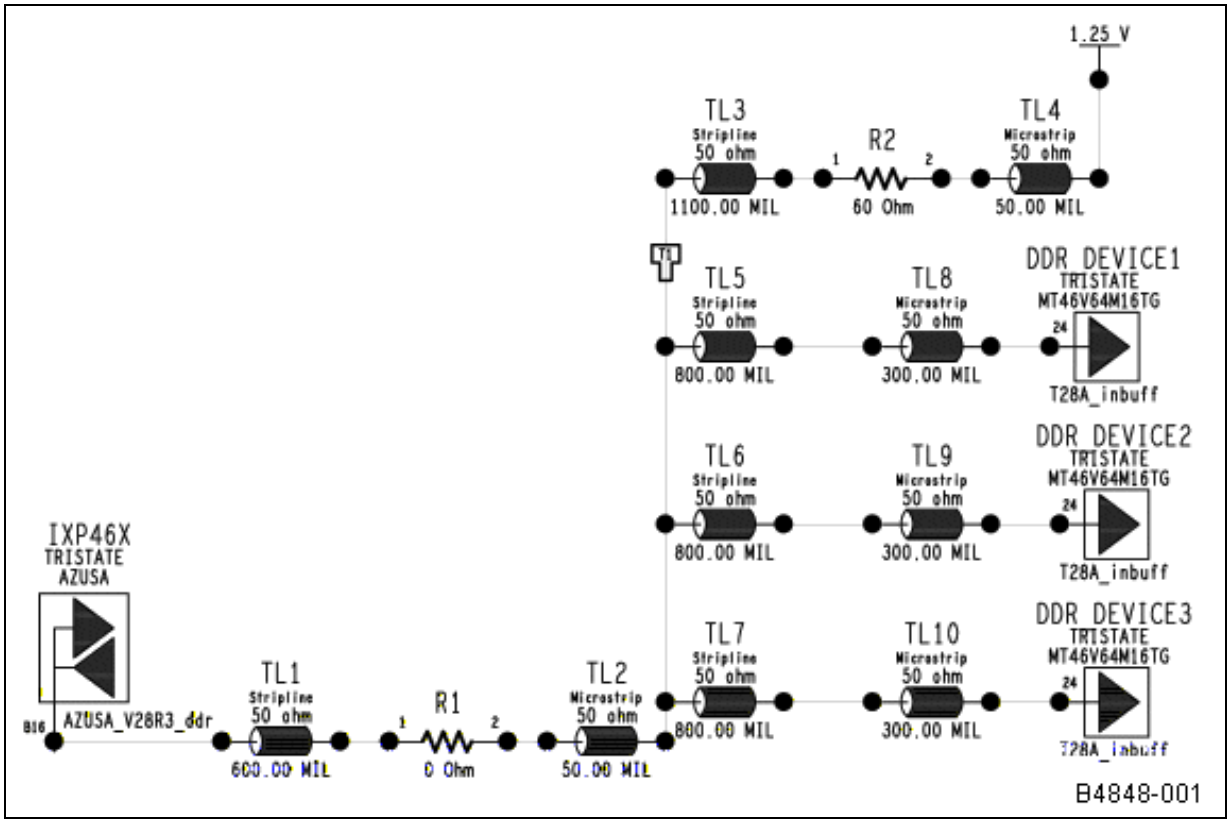
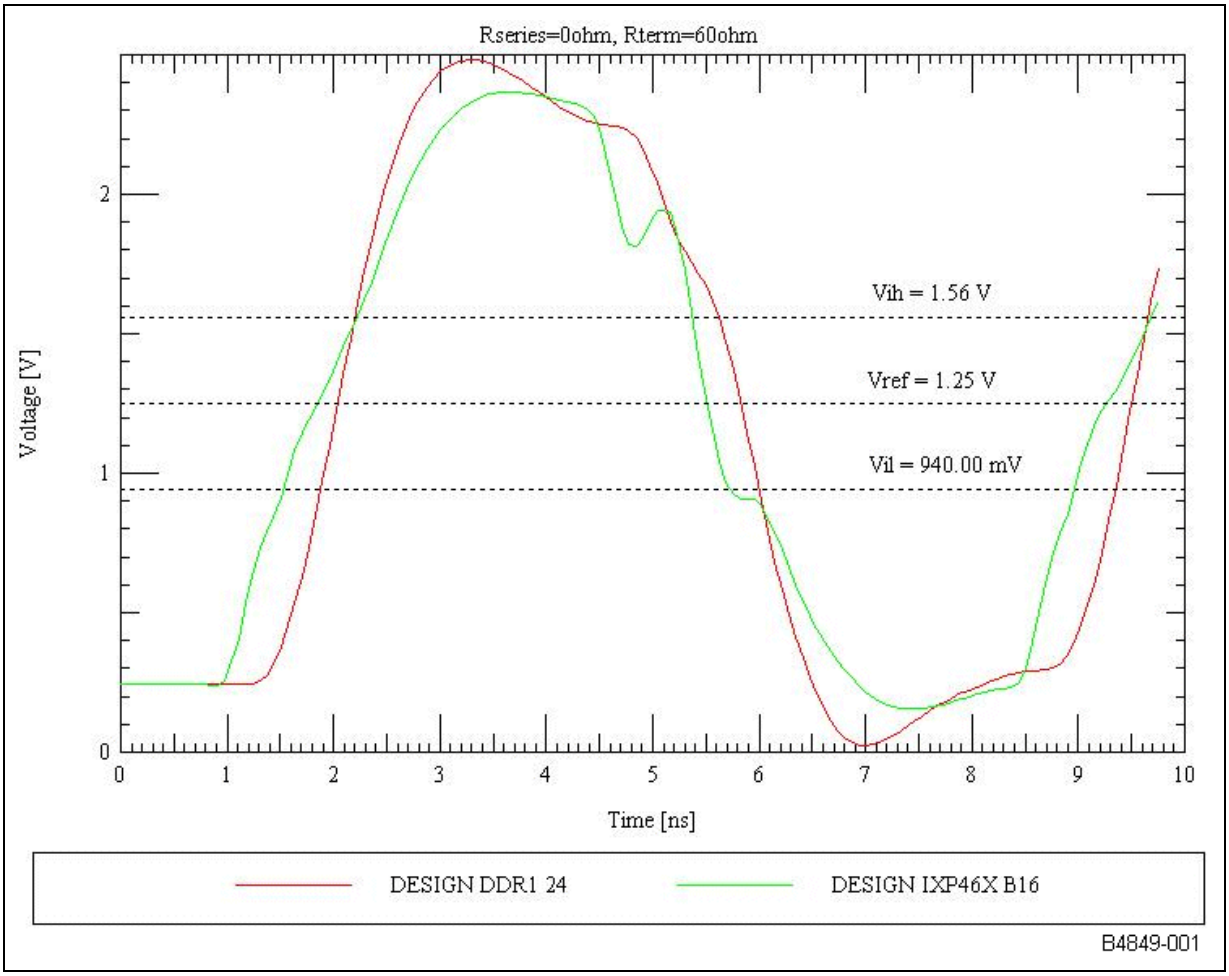


Figure 44. DDR RAS Simulation Results: Two-Bank x16 Devices



The simulation results in Figure 44 are for the control circuit and show that the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.310 or 940 mV and $V_{ih(min)}$ of V_{ref} + 0.310 or 1.56 V are easily achieved at the receiver (DDR_DEVICE1). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V.

Waveform results for DDR_DEVICE2 and DDR_DEVICE3 are not shown as it is identical to that of DDR_DEVICE1 due to symmetry. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

7.2.4 Command Group

The command signal group includes the signals DDRI_MA[13:0], DDRI_BA[1:0], DDRI_RAS, DDRI_CAS and DDRI_WE. The following simulations were constructed for the 2 bank x16 device configuration where each signal would have six receivers.

Table 39 identifies the transmission line lengths for the address (DDRI_MA3) topology shown in Figure 45 and Figure 47. These lengths were chosen as realistic goals given the IXP45X/IXP46X network processors to DDR body to body separation of no more than 500 mils.

Table 39. Command Group Topology Transmission Line Characteristics

Transmission Line	Length
TL1 (T_{pd} = 175 ps/in)	~ 600 mils
TL2 (T_{pd} = 175 ps/in)	~ 50 mils
TL3 (T_{pd} = 175 ps/in)	~ 1,100 mils
TL4 (T_{pd} = 175 ps/in)	~ 50 mils
TL5, TL8, TL11 (T_{pd} = 175 ps/in)	~ 800 mils
TL6, TL7, TL9, TL10, TL12, TL13 (T_{pd} = 175 ps/in)	~ 300 mils

Figure 45. DDR Command (MA3) Topology: Two-Bank x16 Devices

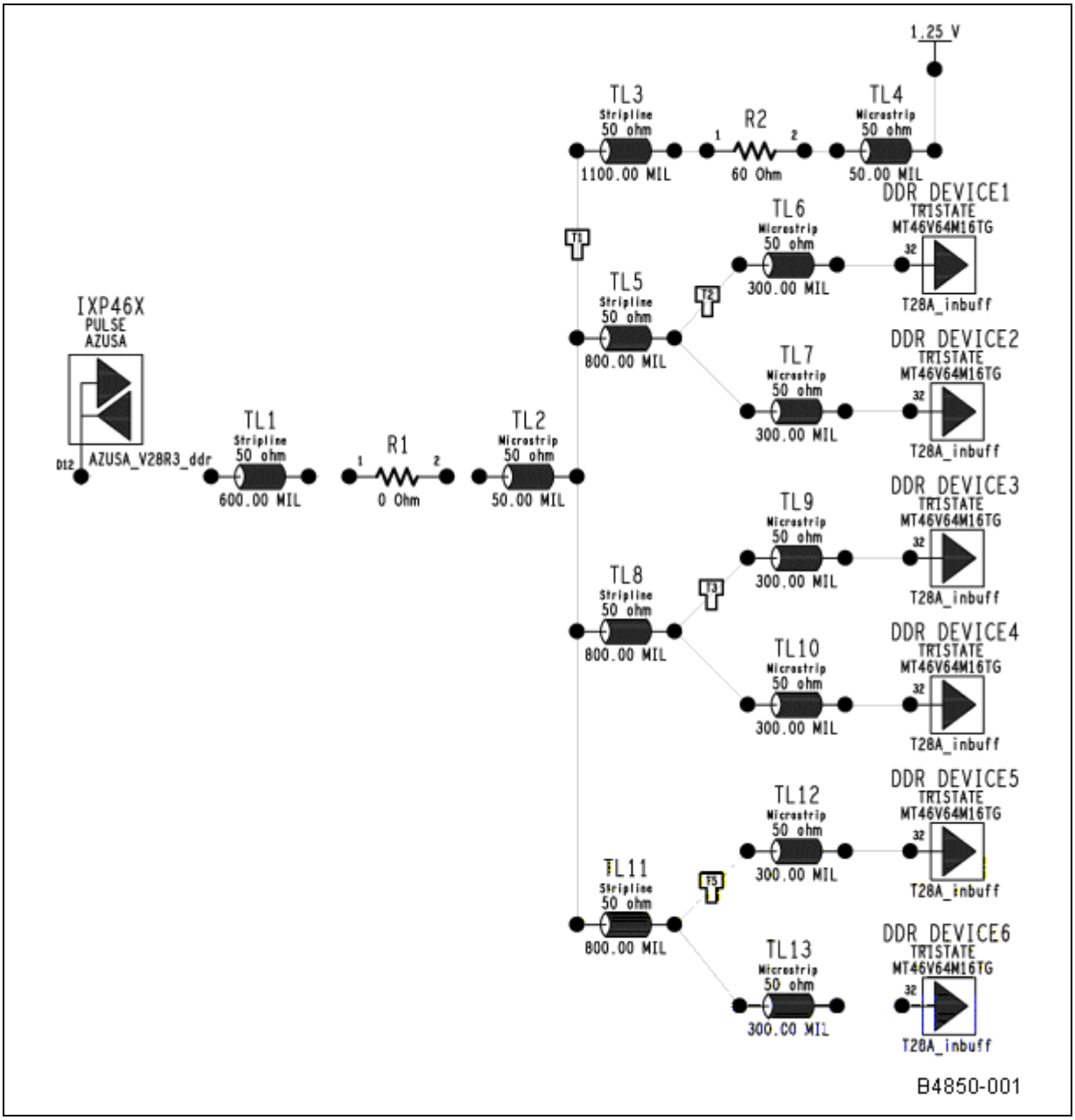
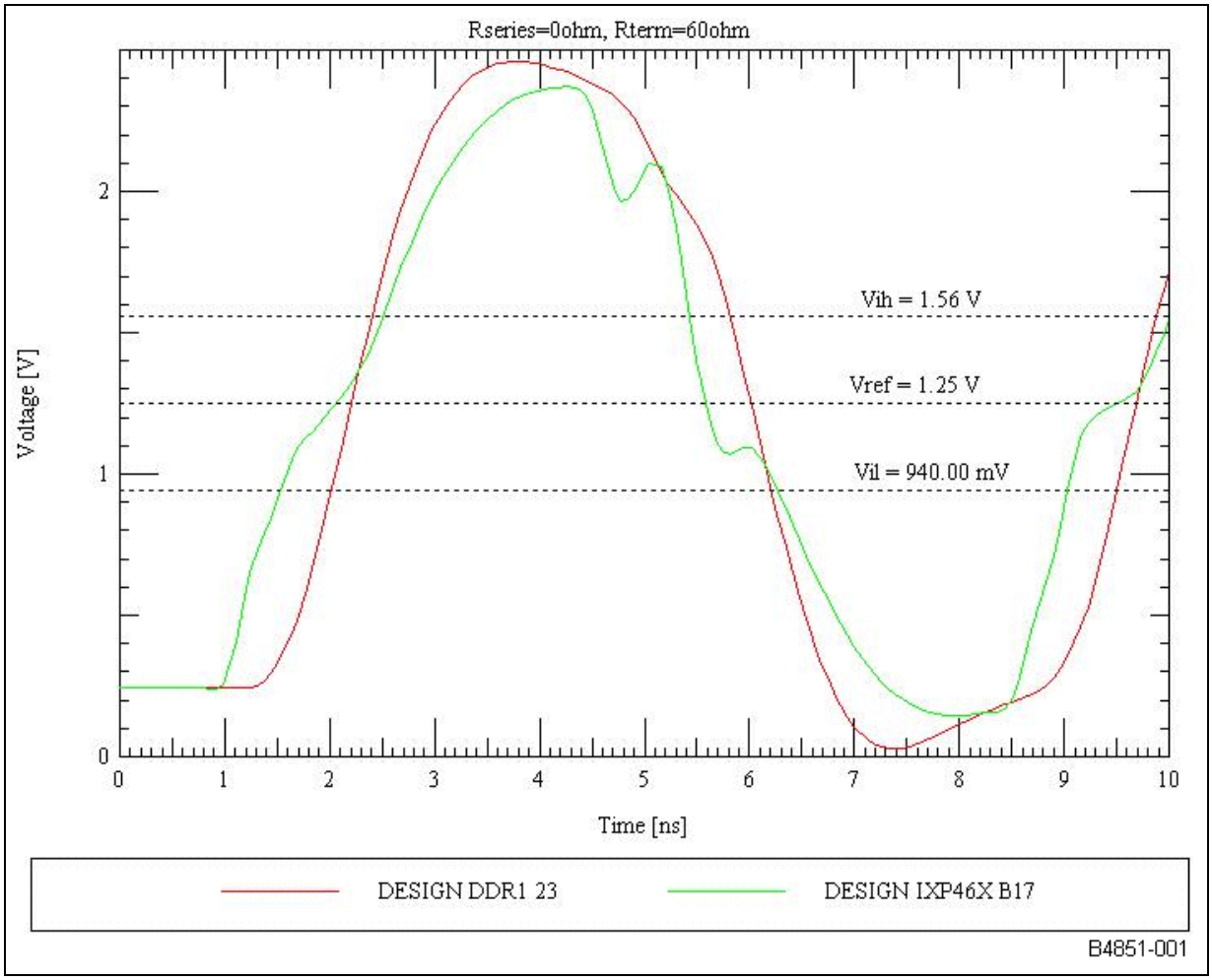


Figure 46. DDR Address Simulation Results: Two-Bank x16 Devices



The simulation results in Figure 46 are for the address circuit and show that the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.310 or 940 mV and $V_{ih(min)}$ of V_{ref} + 0.310 or 1.56 V are easily achieved at the receiver (DDR_DEVICE1). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V.

Waveform results for devices DDR_DEVICE2 through DDR_DEVICE6 are not shown as they are identical to that of device DDR_DEVICE1 due to symmetry. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

Figure 47. DDR Command (RAS) Topology: Two-Bank x16 Devices

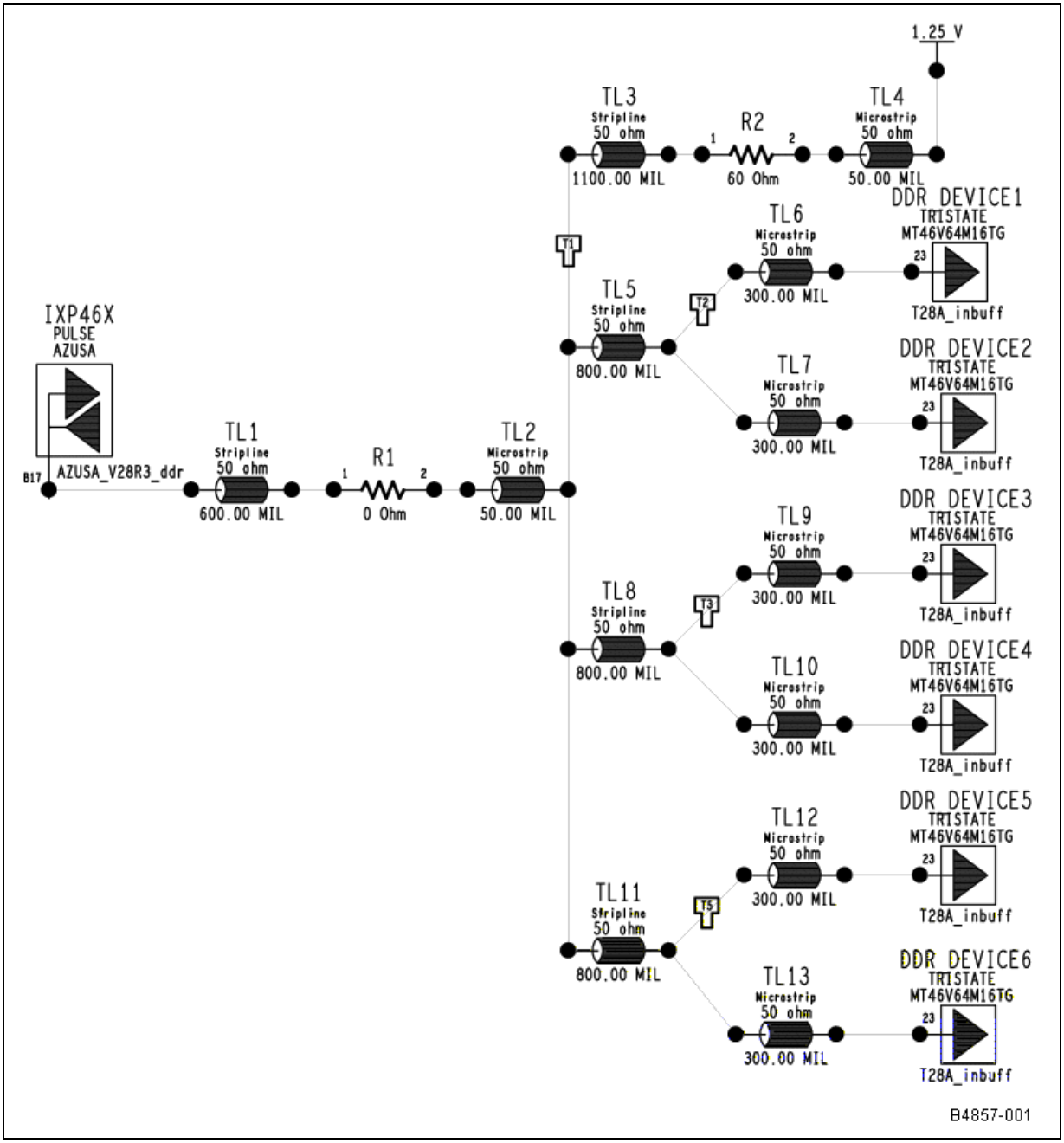
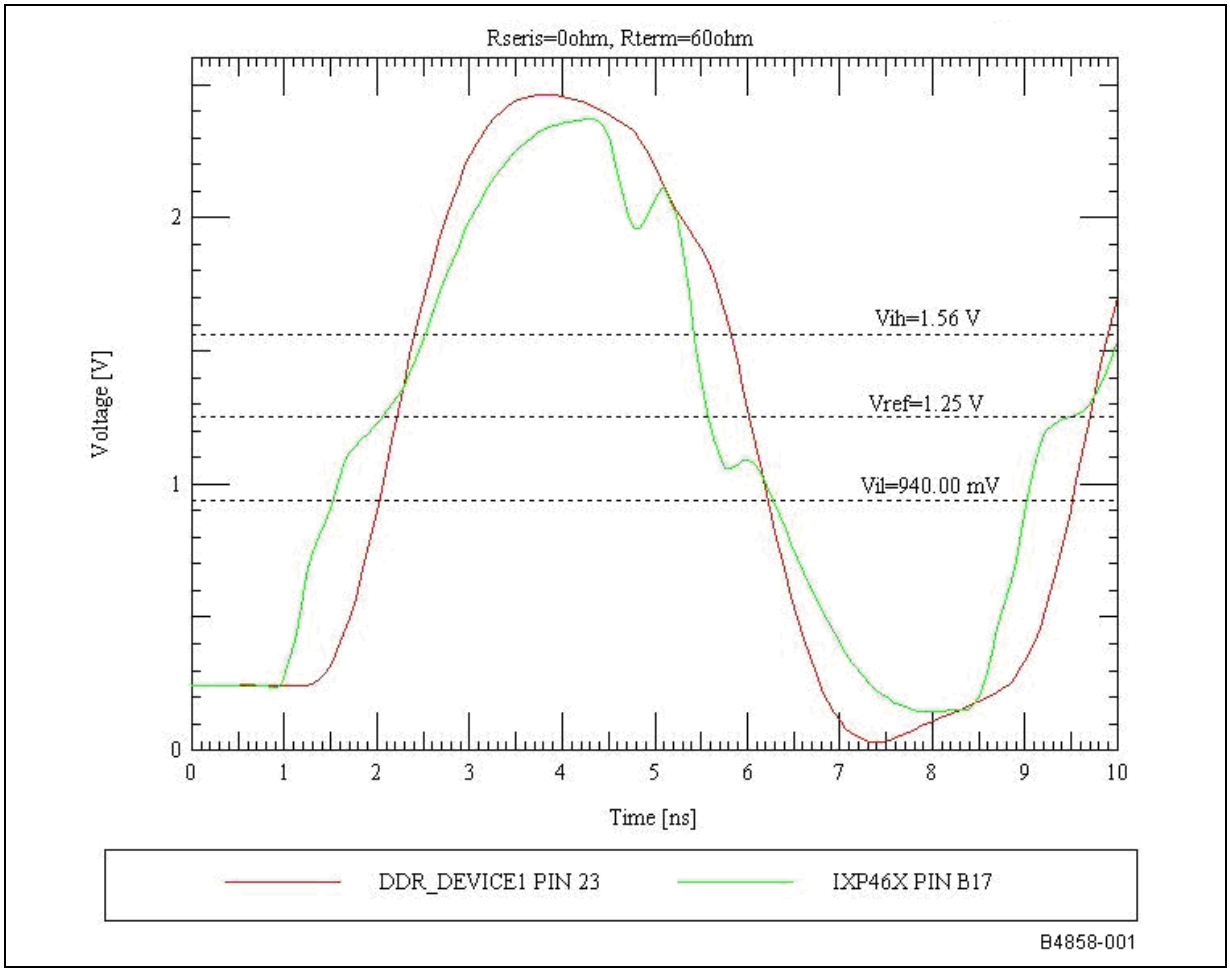


Figure 48. DDR RAS Simulation Results: Two-Bank x16 Devices



The simulation results in Figure 48 are for the RAS circuit, the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.310 or 940 mV and $V_{ih(min)}$ of V_{ref} + 0.310 or 1.56 V are easily achieved at the receiver (DDR_DEVICE1). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V.

Waveform results for devices DDR_DEVICE2 through DDR_DEVICE6 are not shown as they are identical to that of device DDR_DEVICE1 due to symmetry. When final routing data is available, simulation results for all receivers are analyzed as variations in routing may result in differences. These differences should be minimal.

7.2.5 RCVENIN and RCVENOUT

The Receive Enable In (RCVENIN) and Receive Enable Out (RCVENOUT) should be connected and routed to match the length of the clock signal plus the average data signal trace. This length matching is important to insure the signal propagation delay of RCVENIN/RCVENOUT is the same as that for the clock plus average DQ length.

Table 40 identifies the transmission line lengths for the RCVENIN/RCVENOUT topology shown in Table 49. These lengths were chosen from the previous clock and data group simulation topologies.

Table 40. Control Group Topology Transmission Line Characteristics

Transmission Line	Length
TL1 (T_{pd} = 175 ps/in)	~1,700 mils
TL2 (T_{pd} = 175 ps/in)	~1,700 mils

Figure 49. DDR RCVENIN/RCVENOUT Topology

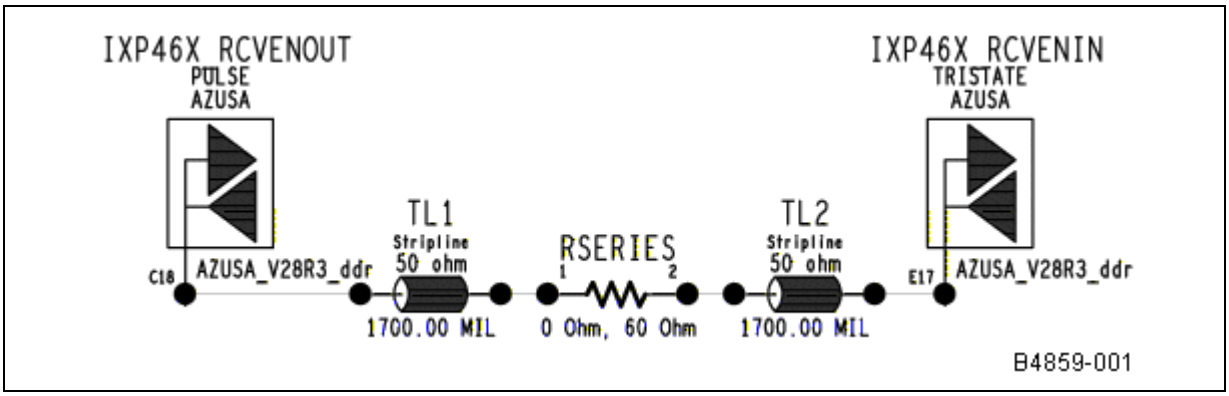
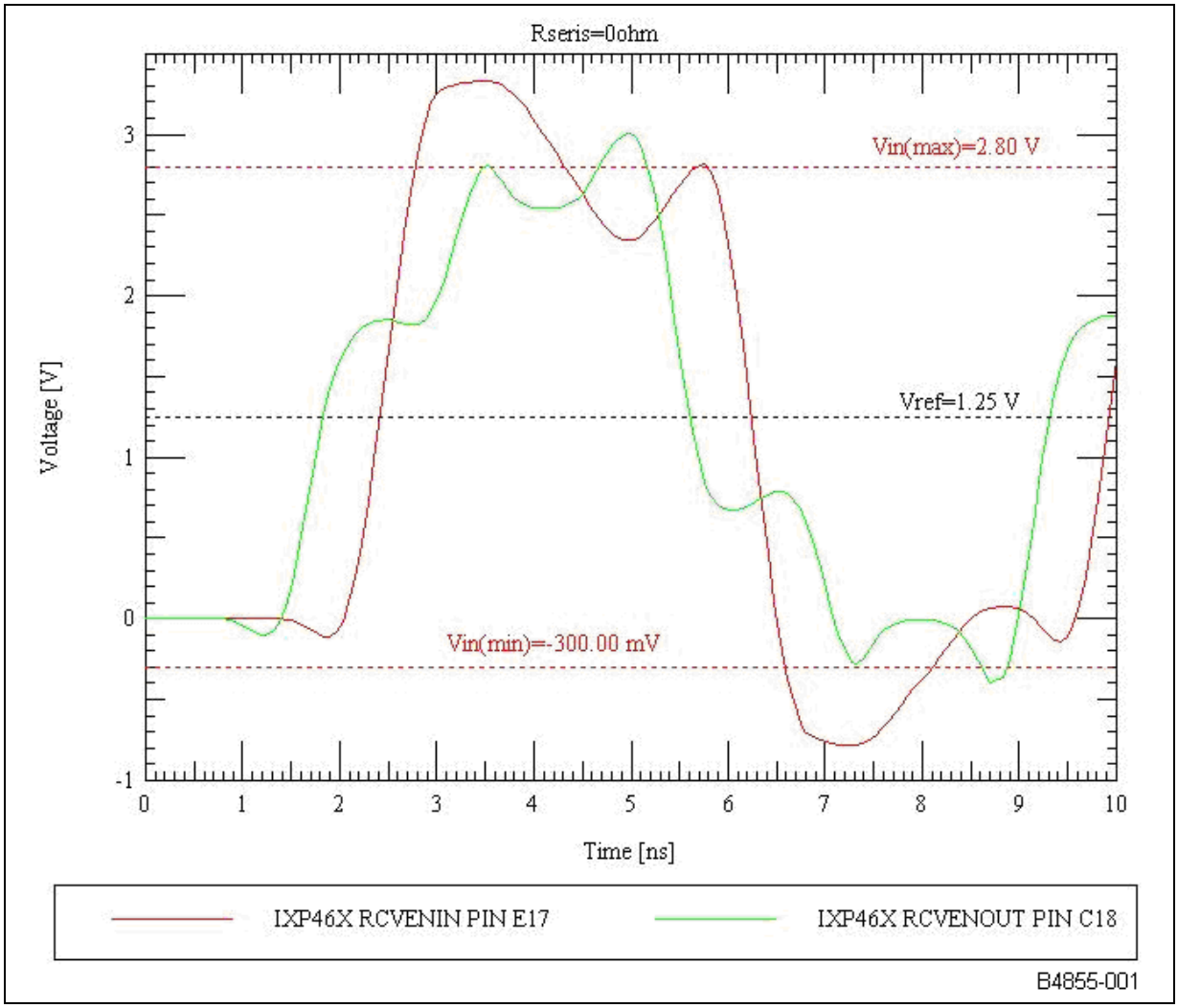
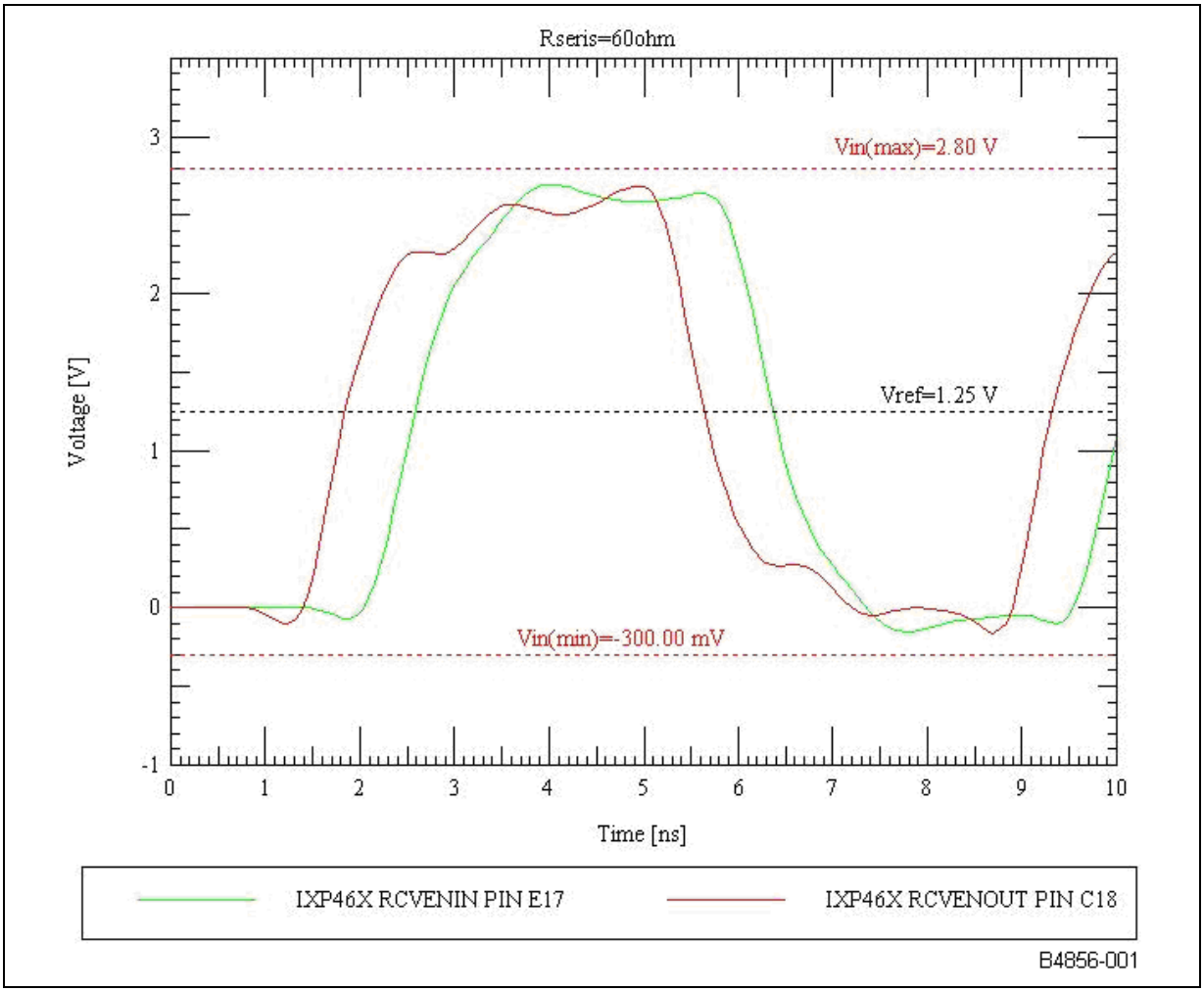


Figure 50. DDR RCVENIN/RCVENOUT Simulation Results (Rseries = 0 Ω)



The simulation results in Figure 50 are for the RCVENIN/RCVENOUT circuit with a 0-Ω series resistor, the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.150 or 1.10 V and $V_{ih(min)}$ of V_{ref} + 0.150 or 1.40 V are easily achieved at the receiver (RCVENIN). However, the receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V and the waveforms at the IXP45X/IXP46X network processors are outside of these limits. A different series resistor should be chosen. The results of using a 60-Ω resistor are shown in Figure 51.

Figure 51. DDR RCVENIN/RCVENOUT Simulation Results (Rseries = 60 Ω)



The simulation results in Figure 51 are for the RCVENIN/RCVENOUT circuit, the voltage waveform meets the DDR device input voltage requirements. $V_{il(max)}$ of V_{ref} – 0.150 or 1.10 V and $V_{ih(min)}$ of V_{ref} + 0.150 or 1.40 V are easily achieved at the receiver (RCVENIN). The receiver waveform must also not exceed a maximum voltage of $V_{in(max)}$ = 2.8 V or the minimum voltage of $V_{in(min)}$ = -0.3 V.