



# **Advanced/RH LPX Motherboard Technical Product Specification**

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# Advanced/RH Technical Product Specification

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# Introduction

The Advanced/RH motherboard integrates the latest advances in processor, memory, and I/O technologies into a standard LPX form factor that provides leading edge technology. This combination of high integration and high performance makes the Advanced/RH motherboard the ideal platform for the increasing requirements of today's (and tomorrow's) desktop applications in the corporate workspace.

The flexible LPX design will accept Pentium® processors operating at 75 MHz, 90 MHz, 100 MHz, 120 MHz, 133 MHz, 150 MHz and 166 MHz as well as future Pentium processors. The processor subsystem is complemented by a Revision 2.1 Card Edge Low Profile (CELP 2.1) socket that accepts either a 256 KB or 512 KB second level write-back cache module using pipelined synchronous burst technology. There is also an option for having 256 KB of Pipeline Burst SRAM soldered onto the motherboard. If cache memory is soldered on the motherboard, the CELP socket will not be installed. Only one type of cache may be used on the Advanced/RH motherboard. The memory subsystem is designed to support up to 512 MB of EDO DRAM (for improved performance) or standard Fast Page DRAM in standard 72-pin SIMM† sockets. A Type 7 Pentium OverDrive® socket provides an upgrade to future OverDrive processors.

The Advanced/RH motherboard utilizes Intel's 82430HX PCIset to provide increased integration and performance over other motherboard designs. The Intel 82430HX PCIset contains an integrated PCI Bus Mastering IDE controller with two high performance IDE interfaces for up to four IDE devices (such as hard drives, CD-ROM readers, and so forth). The 82430HX PCIset coupled with the integration of the industry's latest peripherals gives the user a robust computing platform.

Complementing the 82439HX PCI controller is the 82371SB PIIX3 ISA bridge, offering new technology like USB expandability. The PIIX3 performs as a host on the Universal Serial Bus, and in the middle of 1996 Advanced/RH will provide connectors to accommodate USB peripherals.

ATI† 264-VT video, with fast SGRAM video memory, provides excellent performance advantages over alternate solutions using EDO memory. ATI Media Connector modules, supplied by ATI Technologies, can be used to accelerate hardware MPEG and provide the tuner capabilities that previously required an entire add in card. Memory expansion modules, also supplied by ATI, can upgrade the motherboard from 1MB to 2 or 4 MB of SGRAM.

The National PC87306B Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports, one EPP/ECP capable parallel port, a Real Time Clock, keyboard controller, and support for an IrDA† compatible infrared interface.

To provide for the increasing number of multimedia applications, a Creative† VIBRA16S audio CODEC is integrated onto the motherboard. Either consumer audio or business audio is selected by the OEM. Consumer audio will not have onboard jacks, like business audio, but will provide audio connections via an audio riser card. Either audio solution is provided by the VIBRA16S audio controller, and it provides 16-bit stereo, Sound Blaster Pro† compatible audio with full duplex capabilities to meet the demands of interactive multimedia applications. PCI and ISA expansion slots are supported by a connector on the motherboard designed to accept a riser card.

In addition to superior hardware capabilities, a full set of software drivers and utilities are available to allow advanced operating systems such as Microsoft† Windows† 95 to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Windows 95-ready Plug 'N' Play, Advanced Power Management (APM) with application restart, software-controlled power supply shutdown, and full duplex audio are all provided by software available for the Advanced/RH.

## ***MOTHERBOARD MANUFACTURING OPTIONS***

The following manufacturing options are available. Details for each option are found in the corresponding section of this specification.

### ***AUDIO SUBSYSTEM***

- Business audio
- Consumer audio
- No audio

### ***VIDEO SUBSYSTEM***

- ATI VT graphic controller
- ATI CT graphic controller

### ***CACHE SUBSYSTEM***

- Soldered SRAM
- CELP socket

### ***UNIVERSAL SERIAL BUS***

- USB
- No USB

## BOARD LEVEL FEATURES

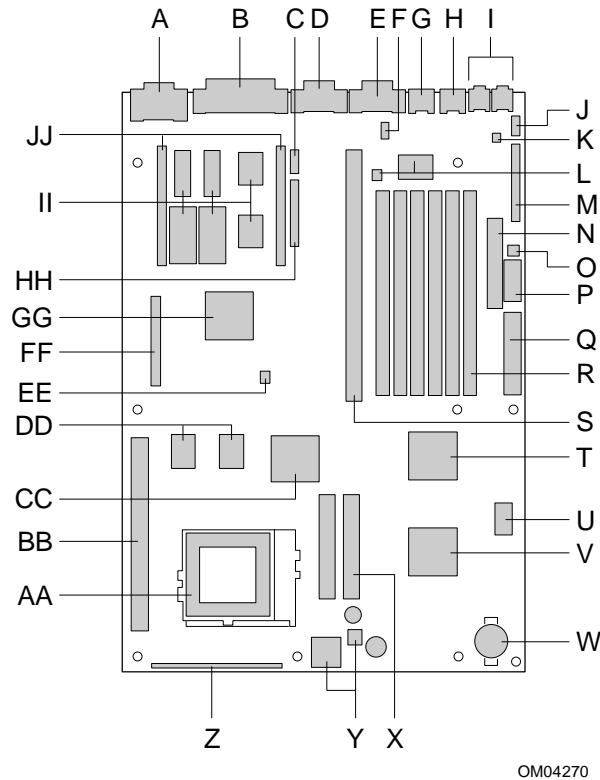


Figure 1. Advanced/RH Motherboard Features

- |  |   |
|--|---|
| A – VGA <sup>†</sup> connector   | S – PCI / ISA expansion connector             |
| B – Parallel port connector  | T – National PC87306B I/O controller          |
| C – COM2 Header  | U – Flash BIOS                                |
| D – COM2, or Dual in-line USB Connector                                    | V – PCI ISA/IDE Xcelerator (PIIX3)            |
| E – COM1 connector   | W – Battery for the Real-time clock           |
| F – Four Pin CD-ROM audio connector  | X – Two PCI IDE interfaces                    |
| G – PS/2 <sup>†</sup> Mouse port   | Y – CPU 3.3v voltage regulator                |
| H – PS/2 Keyboard port   | Z – Front Panel I/O connector                 |
| I – Two 3.5 mm Audio Jacks (mic in, line out)                              | AA – Socket 7 Pentium Processor socket        |
| J – Eight Pin Wave table upgrade connector                                 | BB – Celp 2.1 connector cache module socket   |
| K – 3 Pin Modem Audio Connector  | CC – 82439HX controller (TXC)                 |
| L – Creative Labs Vibra 16S audio, Yamaha <sup>†</sup> OPL3 FM synthesizer | DD – 256K L2 PBRAM                            |
| M – Midi Audio/Joystick connector  | EE – Riser Card 2/3 slot jumper               |
| N – Floppy connector   | FF – ATI Media Channel Connector for H/W MPEG |
| O – Power Supply control connector   | GG – ATI graphics controller                  |
| P – 3.3v Power connector   | HH – Configuration jumper blocks              |
| Q – Primary power connector  | II – Up to 2 MB graphics memory               |
| R – Six SIMM sockets (three banks)   | JJ – SGRAM Graphics memory upgrade header     |

(This figure identifies the location of motherboard manufacturing options. Not all locations will be populated on all motherboards.)

## LPX FORM FACTOR

The Advanced/RH motherboard is designed to fit into a standard LPX form factor chassis. Figure 2 illustrates the mechanical form factor for the Advanced/RH. The Advanced/RH LPX form factor does adhere to the standard LPX guidelines in that the outer dimensions are 13" x 9". Location of the I/O connectors, riser slot, and mounting holes are in strict compliance with the LPX specification. However, if business audio is selected by an OEM, a slight modification to the OEM's chassis may be necessary to accept the audio jacks on the motherboard.

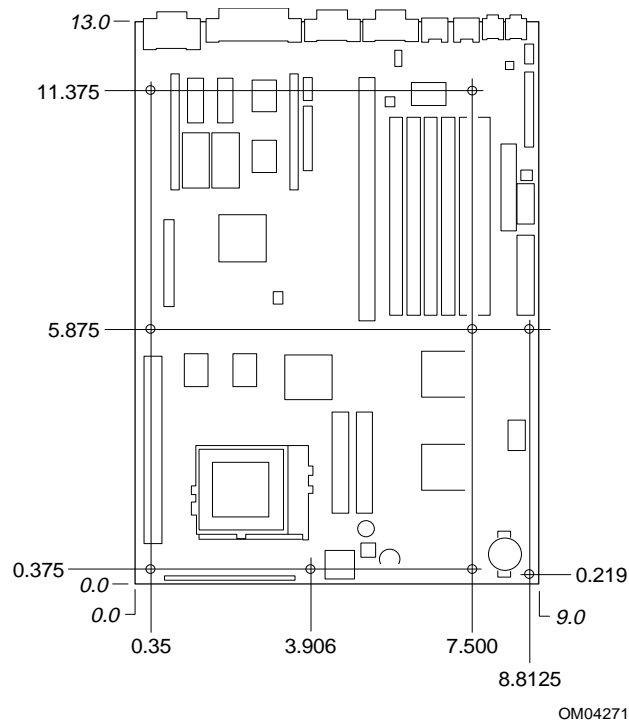


Figure 2. Advanced/RH Motherboard dimensions

## CPU

The Advanced/RH LPX motherboard is designed to operate with 3.3 volt Pentium processors. The 3.3 volt power is provided by a patented on-board voltage regulator circuit. An on-board jumper enables use of VRE specified processors. The voltage regulator provides the required voltage for the processor from the 5 volt output of a standard power supply. Processors which run internally at 75, 90, 100, 120, 133, 150 and 166 MHz, and have iCOMP<sup>®</sup> ratings of 615, 735, 815, 1000, 1110, 1176 and 1308 respectively are supported. Future Pentium processors will also be supported.

The Pentium processor maintains full backward compatibility with the 8086, 80286, Intel386<sup>™</sup> and Intel486<sup>™</sup> processors. It supports both read and write burst mode bus cycles, and includes separate 8 KB on-chip code and data write-back caches. Also integrated into the Pentium processor is an advanced numeric coprocessor which significantly increases the speed of floating point operations, while maintaining backward compatibility with the Intel486DX<sup>™</sup> math coprocessor and complying to ANSI/IEEE standard 754-1985.



## **PROCESSOR UPGRADE**

The Advanced/RH motherboard is manufactured with the 321-pin (socket 7) ZIF processor socket. Socket 7 provides a processor upgrade path that includes higher performance Pentium OverDrive processors than can be supported with socket 5. The motherboard is built to support uniplane CPUs. However, a manufacturing option allows the socket 7 design to support split voltage planes that can supply different voltages for a processor's CPU core and for the I/O core. Installing a split plane CPU into a motherboard configured only for uniplane processor may cause damage to the CPU.

## **SECOND LEVEL CACHE**

The Intel 82430HX PCIset supports a second level cache that uses high performance Synchronous Pipeline Burst SRAM. Asynchronous cache is not supported by the 82430HX controller. Pipeline Burst (PB) SRAM provides performance similar to expensive Synchronous Burst SRAMs for only a slight cost premium over slower performing asynchronous SRAMs.

As a manufacturing option, the Advanced/RH motherboard without onboard cache can be provided with a Card Edge Low Profile (CELP) version 2.1 socket that provides flexibility for second level cache options. The CELP socket can accommodate either a 256 KB or 512 KB cache module and is designed to work with modules that adhere to the COAST (Cache On A Stick) specification, version 2.1. The cache size is automatically detected and configured by the system BIOS for optimal performance. For a list of cache module suppliers or a copy of the COAST specification, contact your local Intel sales office or Intel authorized distributor.

## **SYSTEM MEMORY**

The Advanced/RH motherboard provides six 72-pin SIMM sites for memory expansion. The sockets support 512 KB x 32 (2MB double sided SIMMs only), 1M x 32 (4 MB), 2M x 32 (8 MB), 4M x 32 (16 MB), 8M x 32 (32 MB), 16M x 32 (64MB), and 32M x 32 (128MB) single-sided or double-sided SIMM modules. Minimum memory size is 8 MB and maximum memory size, using four 32M x 32 SIMM modules, is 512 MB. Memory timing requires 70 ns fast page devices or, for optimum performance 60 ns EDO DRAM. 36-bit SIMM modules may be used for parity or ECC generation and checking.

The six sockets are arranged as Bank 0, Bank 1, and Bank 2. Each bank consists of two sockets and provides a 64/72-bit wide data path. Both SIMMs in a bank must be of the same memory size and type, although each bank may have different types of memory installed. It is even possible to have 70 ns Fast Page DRAM in one bank and 60 ns EDO DRAM in the other, in which case each bank is independently optimized for maximum performance. Any combination of the banks may be populated. There are no jumper settings required for the memory size or type, which is automatically detected by the system BIOS. The Advanced/RH motherboard supports only tin-lead SIMMs.

When banks 1 and 2 are populated at the same time, memory timing is modified from x333 to x444. This is due to loading on the address line shared by these two banks. In most applications the L2 cache will mask any performance degradation that is incurred. In addition, when using EDO Parity memory in an ECC configuration memory timing is changed from x222 to x333 to allow the chipset to perform Read Modify Writes.

## **EDO DRAM**

Extended Data Out, or Hyper Page, DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard fast page mode DRAM which tri-states the memory data when CAS# negates to precharge for the next cycle. With EDO, the CAS# precharge overlaps the data valid time, allowing CAS# to negate earlier while still satisfying the memory data valid window time.

## EXPANSION RISER

An expansion slot riser connector of EISA form factor provides the capability to support either two or three PCI slots by changing a motherboard jumper to route any extra IRQ and ID selects. A riser board can also support up to five ISA expansion slots. The PCI bus is compliant with the PCI 2.1 specification.

To ensure that the lowest positioned slot on the riser card can support a full length add-in card the following conditions must be met.

- 1) The minimum height requirement for the lowest positioned slot on the CPU side of the riser is 1.2". Therefore the CPU heat sink should be no more than 1.2" high once installed on the processor.
- 2) The minimum height requirement for the lowest positioned slot on the SIMM side of the riser is 1.3". Therefore, once SIMM memory is installed they should not be taller than 1.3".

## PERIPHERAL COMPONENT INTERCONNECT (PCI) PCISSET

The Intel 82430HX PCISet is made up of two components: The 82439HX controller (TXC) and the 82371SB PCI ISA IDE Xcellerator (PIIX3) ISA bridge. The PCISet provides the following functions:

- CPU interface control
  - Integrated L2 write-back cache controller
    - Pipeline Burst SRAM
    - 256 KB or 512 KB Direct Mapped
  - Integrated DRAM controller
    - 64/72-bit path to Memory
    - Support for EDO and Fast Page DRAM
    - 8 MB to 512 MB main memory
    - Parity and ECC support
  - Fully synchronous PCI bus interface
    - 25/30/33 MHz
    - PCI to DRAM > 100 Mbytes/sec
  - Interface between the PCI bus and ISA bus
  - Universal Serial Bus Controller
- (with B0 stepping of the PIIX 3)
- Host/Hub Controller
  - Two USB ports
  - Integrated fast IDE interface
    - Support for up to 4 devices
    - PIO Mode 4 transfers up to 16 MB/sec
    - Integrated 8 x 32-bit buffer for Bus Master PCI IDE burst transfers
    - Bus Master mode
  - PCI 2.1 Compliant
  - Enhanced Fast DMA controller
  - Interrupt controller and steering
  - Counters/Timers
  - SMI interrupt logic and timer with Fast On/Off mode

### 82439HX TXC

The 439HX controller provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency. The 439HX controller comes in a 324 pin Ball Grid Array package.

### 82371SB PCI ISA IDE XCELERATOR (PIIX3)

The PIIX3 provides the interface between the PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting up to 4 devices. USB host/hub bus is provided by the PIIX 3. The PIIX3 integrates seven 32-bit DMA channels, five 16-bit timer/counters, two eight-channel interrupt controllers, PCI-to-AT interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry onto the same device. The PIIX3 comes in a 208 pin QFP package.

## **IDE SUPPORT**

The Advanced/RH motherboard provides two independent high performance bus-mastering PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The system BIOS supports Cylinder Sector Head (CHS), Logical Block Addressing (LBA) and Extended Cylinder Sector Head (ECHS) translation modes as well as ATAPI (e.g. CD-ROM) devices on both IDE interfaces. IDE device transfer rate and translation mode capability can be automatically determined by the system BIOS.

Normally, programmed I/O operations require a substantial amount of CPU bandwidth. In multi-tasking operating systems like Microsoft Windows 95, the CPU bandwidth freed up by using bus mastering IDE can be used to complete other tasks while disk transfers are occurring. A driver is required for the IDE interface to operate as a PCI bus master capable of supporting PIO Mode 4 devices with transfer rates up to 22 MB/sec while minimizing the system demands upon the processor.

Detailed information on the PCIset is available in the Intel 82430HX PCIset data sheet.

## **NATIONAL SEMICONDUCTOR PC87306B SUPER I/O CONTROLLER**

Control for the integrated serial ports, parallel port, floppy drive, RTC and keyboard controller is incorporated into a single component, the National Semiconductor PC87306B. This component provides:

- Two NS16C550-compatible UARTs with send/receive 16 byte FIFO
  - Support for an IrDA compliant Infra Red interface
- Multi-mode bi-directional parallel port
  - Standard mode; IBM<sup>†</sup> and Centronics<sup>†</sup> compatible
  - Enhanced Parallel Port (EPP) with BIOS/Driver support
  - High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)
- Integrated Real Time Clock accurate within +/- 13 minutes/yr at 25° C and 5 volts when the system is continuously powered on
- Integrated 8042 compatible keyboard controller

The PC87306B is normally configured by the BIOS automatically. However configuration of these interfaces is possible via the CMOS Setup program that can be invoked during boot-up. The serial ports can be enabled as COM1, COM2, IrDA, or disabled. The parallel port can be configured as normal, extended, EPP/ECP, or disabled. The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.2 MB, 1.44 MB, or 2.88 MB 3½" media. Header pins located near the back of the board allow cabling to use these interfaces

## **FLOPPY CONTROLLER**

The PC87306B is software compatible with the DP8473 and 82077 floppy disk controllers. The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.2 MB, 1.44 MB, or 2.88 MB 3½" media in the BIOS setup. By default, the Floppy A interface is configured for 1.44 MB and Floppy B is disabled. Another setup option prevents the user from being able to write to floppy. Configuring the floppy interface for 1.2 MB 3½" (3-mode floppy) requires the use of a driver to operate correctly.

## **KEYBOARD INTERFACE**

PS/2 keyboard/mouse connectors are located on the back panel side of the motherboard. The 5V lines to these connectors are protected with a PolySwitch<sup>†</sup> circuit which acts much like a self-healing fuse, re-establishing the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, care should be taken to turn off the system power before installing or removing a keyboard or mouse. The system BIOS can detect and correct keyboards and mice plugged into the wrong PS/2<sup>†</sup> style connector.

The integrated 8042 microcontroller contains the AMI Megakey keyboard/mouse controller code which, besides providing traditional keyboard and mouse control functions, supports Power-On/Reset (POR) password protection. The POR password can be defined by the user via the Setup program. The keyboard controller also provides for the following "hot key" sequences:

- <CTRL><ALT><DEL>: System software reset. This sequence performs a software reset of the system by jumping to the beginning of the BIOS code and running the POST operation.
- <CTRL><ALT><+> and <CTRL><ALT><->: Turbo mode selection. <CTRL><ALT><-> sets the system for de-turbo mode, emulating an 25 MHz AT, and <CTRL><ALT><+> sets the system for turbo mode. Changing the Turbo mode may be prohibited by an operating system, or when the CPU is in Protected mode or virtual x86 mode under DOS.
- <CTRL><ALT><defined in setup>: Power down and coffee-break key sequences take advantage of the SMM features of the Pentium Processor to greatly reduce the system's power consumption while maintaining the responsiveness necessary to service external interrupts.

## **REAL TIME CLOCK, CMOS RAM AND BATTERY**

The integrated Real Time Clock (RTC) is DS1287 and MC146818 compatible and provides a time of day clock and a 100-year calendar with alarm features. The RTC can be set via the BIOS SETUP program. The RTC also supports a 242-byte battery-backed CMOS RAM area in two banks. This area is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, the CMOS RAM values can be cleared to the system defaults by using a configuration jumper on the motherboard. Table B-1, in Appendix B, lists the configuration jumper settings.

An external coin-cell style battery provides power to the RTC and CMOS memory. The battery has an estimated lifetime of three years if the system is not plugged into the wall socket. When the system is plugged in, power is supplied from the LPX power supply's 5v standby current to extend the life of the battery. See Appendix A for information regarding replacement batteries.

## **IRDA (INFRA-RED) SUPPORT**

A 5-pin interface on the front panel I/O connector is provided to allow connection to a Hewlett Packard HSDSL-1000 compatible Infra-red (IrDA) transmitter/receiver. Once the module is connected to the front panel I/O header, serial port 2 can be re-directed to the IrDA module, allowing the user to transfer files to or from portable devices such as laptops, PDA's and printers using application software such as LapLink. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter.

## **PARALLEL PORT**

The Parallel port can be configured in the BIOS setup as output only compatible mode, bi-directional mode, ECP or EPP modes. The highly flexible parallel port can also be assigned to I/O addresses 278H, 378H, or 3BCH and IRQ's 5 or 7. Furthermore, a routable DMA scheme allows Plug 'N' Play operating systems such as Windows 95 to route either DMA channel 1 or 3 to the parallel port for ECP mode. EPP BIOS support must be provided by a device driver or TSR.

## **GRAPHICS SUBSYSTEM**

The ATI-264VT controller is a highly integrated multimedia graphics & video controller for PCI bus systems. The VT achieves enhanced performance with an all in one design that integrates a video scaler, a color space converter, a true color palette DAC, and a triple clock synthesizer with ATI's proven Mach64<sup>†</sup> graphics engine. The ATI-264VT controller is register compatible with ATI's Mach64 accelerator series, and therefore is immediately compatible with a wide range of software applications and drivers.

As a manufacturing option, the Advanced/RH board is also available with an ATI-264CT video controller and 1 MB of EDO video DRAM, upgradeable to a total of 2 MB by adding 1 MB of socketed video DRAM.

## ATI-264VT RESOLUTIONS SUPPORTED BY THE MOTHERBOARD

Resolution	1 MB SGRAM	2 MB SGRAM	Max Vertical Refresh Rate
640x480x4bpp	X	X	100 Hz
640x480x8bpp	X	X	100 Hz
640x480x16bpp	X	X	100 Hz
640x480x24bpp	X	X	100 Hz
640x480x32bpp		X	60 Hz
800x600x4bpp	X	X	100 Hz
800x600x8bpp	X	X	100 Hz
800x600x16bpp	X	X	100 Hz
800x600x24bpp		X	100 Hz
1024x768x4bpp	X	X	100 Hz
1024x768x8bpp	X	X	100 Hz
1024x768x16bpp		X	100 Hz
1280x1024x4bpp	X	X	75 Hz
1280x1024x8bpp		X	75 Hz

Table 1. Advanced/RH Audio resource mapping

## GRAPHICS DRIVERS AND UTILITIES

Graphics drivers and utilities for Windows<sup>†</sup> 3.11 or for Windows 95 are supplied with the Advanced/RH motherboard.

## AUDIO SUBSYSTEM

The Advanced/RH offers three audio options for the OEM. The consumer audio option uses an onboard header to route audio to a riser card in the I/O panel. Consumer audio also includes a wave table upgrade header for future expansion.

The business audio option includes mike and line jacks on the motherboard next to the mouse and keyboard connectors. A third option is to have the board with no on-board audio.

The Advanced/RH audio subsystem is based upon the Creative Labs Vibra 16S audio controller and Yamaha OPL3 FM synthesizer. The controller features a 16-bit stereo audio sub-system as a factory installed option along with the OPL3 FM synthesizer. The Vibra 16S controller provides all the digital audio and analog mixing functions required for recording and playing of audio on personal computers. These functions include stereo analog-to-digital and digital-to-analog converters, analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, and digital audio compression via selectable A-law /  $\mu$ law, and full digital control of all mixer and volume control functions.

## VIBRA 16S RESOURCE MAP

Base Address (software configured) 220H - 22FH(Default) or 240H - 24FH or 260H - 26FH or 280H - 28FH	Joystick Enable (software configured) Default Enabled
FM Address (fixed) 388H - 38BH	Interrupt (Software configured) IRQ2/9 or IRQ5 (default) or IRQ7 or IRQ10
Joystick Address/Game Port (fixed) 200H - 207H	8-bit DMA Channel (software configured) DMA Channel 1 (default) or DMA Channel 3
MPU-401 Address (software configured) 300H - 301H or 330H - 331H (default)	16-bit DMA Channel (software configured) DMA channel 5 (default) DMA channel 7
MPU-401 Enable (software configured) Default is disabled	

Table 2. Advanced/RH Audio resource mapping

## **AUDIO DRIVERS**

Audio software and utilities are provided for the Advanced/RH motherboard. A Windows setup program installs all of the software programs and utilities onto the system hard drive. Included in the Creative audio software are DOS utilities that allow the user to play a CD-ROM, control sound volume and mixer settings, run diagnostics, and switch between Sound Blaster Pro and Windows Sound System modes. Windows drivers and utilities include the Windows sound driver, audio input control panel, audio mixer control panel, and a business audio transport utility.

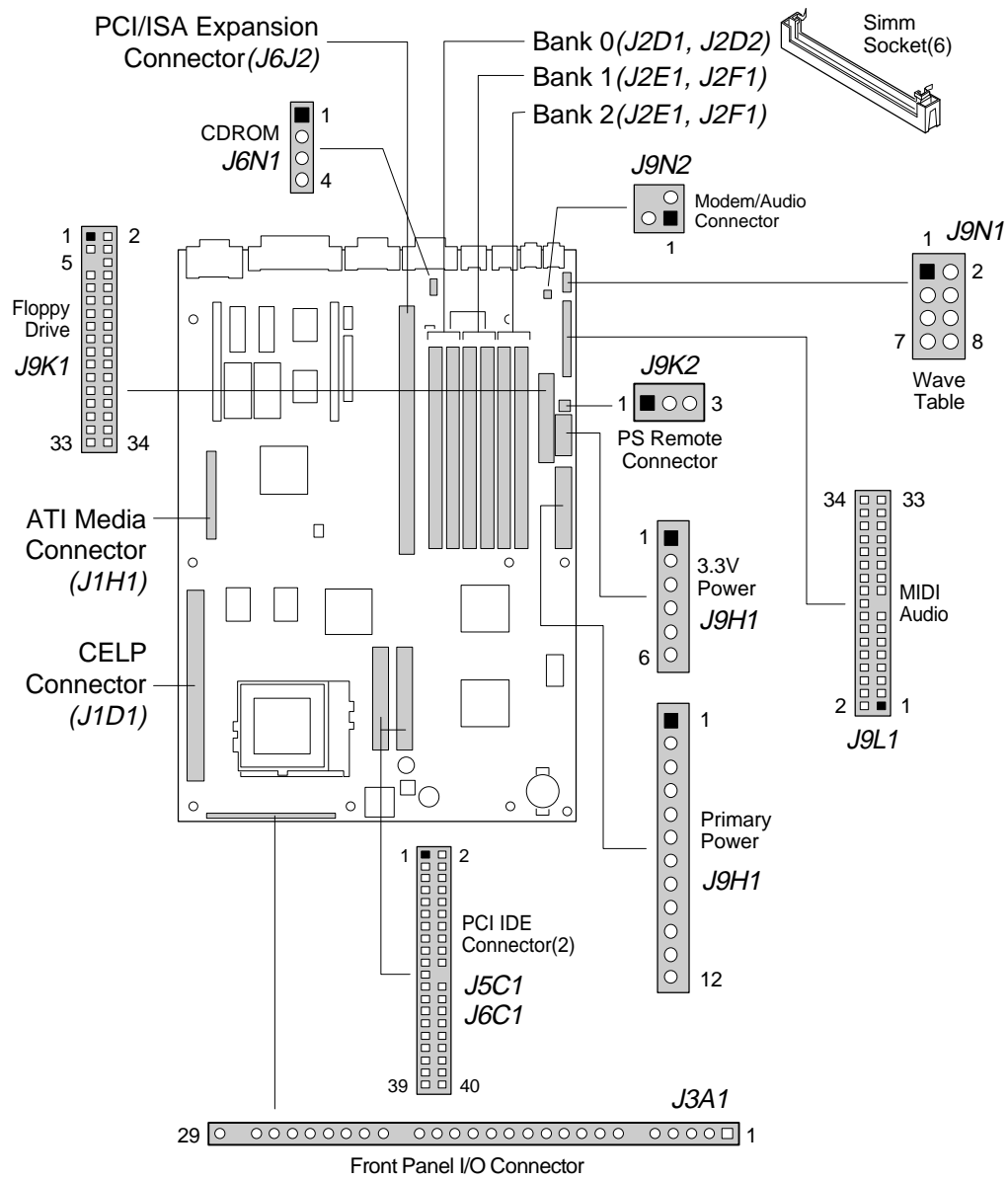
## **UNIVERSAL SERIAL BUS (USB)**

When B0 steppings of PIIX 3 are used in manufacturing, USB connectors may be added as a manufacturing option to support the new technology. The USB connector will occupy the serial 2 connector location, and there is a header to reroute COM2 to a breakout in the chassis or IO panel if the customer so desires.

# **Connectors**

## **MOTHERBOARD CONNECTORS**

There are connectors on-board for Floppy, IDE, Graphics memory upgrade sockets, VESA<sup>†</sup> feature connector, SIMMs, CELP cache modules, battery holder and front panel I/O connectors.



OM04275

Figure 3. Advanced/RH connector locations

## POWER SUPPLY CONTROL (J9H1,J9K2)

When used with a power supply that supports remote power on/off, the Advanced/RH motherboard can turn off the system power via software control (“soft-off”). The Powerman utility supplied for Windows 3.1x allows for soft-off as does the shutdown icon in Windows 95 Start menu. The system BIOS will turn the system power off when it receives the proper APM command from the OS. For example, Windows 95 will issue this APM command when the user selects the “Shutdown the computer” option. Note that APM must be enabled in the system BIOS and OS in order for the soft-off feature to work correctly. Power supplies that support “soft-off” connect to the motherboard via the 3-pin “PWS CNTRL” connector, which is a Molex 2695 connector featuring a security latch for reliability. In order for the system to recognize the presence of a “soft-off” power supply, the supply must tie pin 3 of the PWS Control connector to ground.

## FRONT PANEL CONNECTIONS (J3A1, J2A1)

The Advanced/RH motherboard provides header connectors to support functions typically located on the chassis bezel. Refer to Appendix G for exact pinout definitions for all of the connectors. Front panel features supported include:

- System Speaker
- Infra-Red (IrDA) port
- Sleep/Resume
- Hard Drive activity LED
- Power LED
- System Reset
- CPU fan

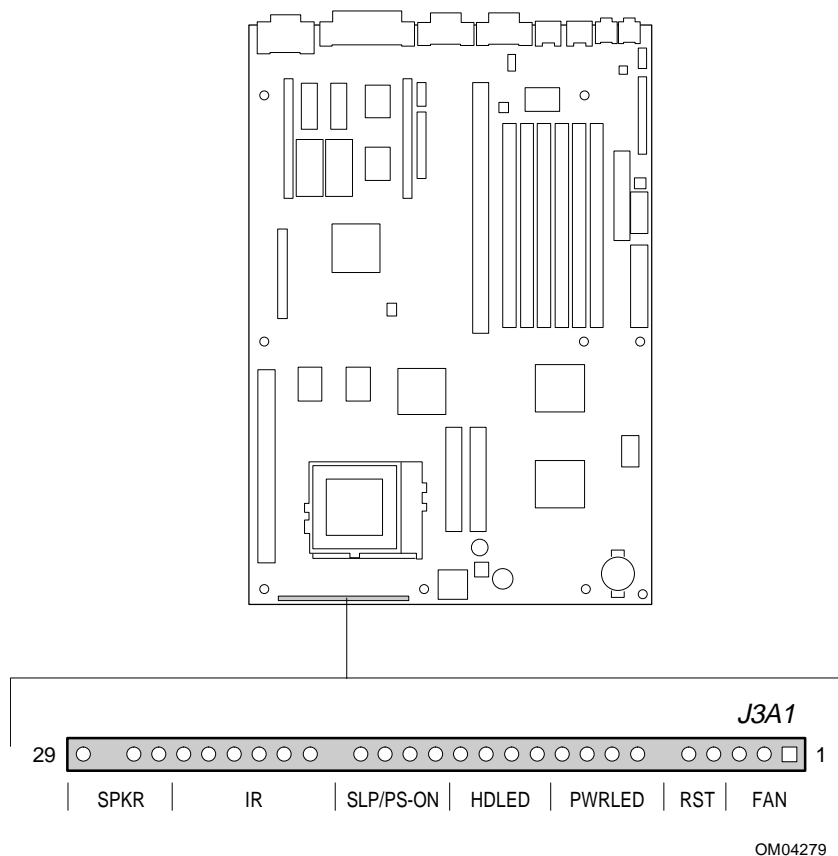


Figure 4. Front Panel I/O Connectors



## ***SPEAKER***

The external speaker provides error beep code information during the Power-On Self Test if the system cannot use the video interface. If no speakers are plugged into the audio output jack, the audio output is redirected to the external PC speaker.

## ***SLEEP / RESUME***

When Advanced Power Management (APM) is activated in the system BIOS and the operating system's APM driver is loaded, Sleep mode (Stand-By) can be entered in one of three ways: an optional front panel "Sleep/Resume" button, a user defined keyboard hot key, or prolonged system inactivity. The Sleep/Resume button is supported by a 2-pin header located on the front panel I/O connector. Closing the "Sleep" switch will generate an SMI (System Management Interrupt) to the processor which immediately goes into System Management Mode (SMM), the so called "Sleep" mode. The front panel "Sleep mode" switch must be a momentary two pin SPST type that is normally open. The function of the Sleep/Resume button can also be achieved via a keyboard hot-key sequence, or by a time-out of the system inactivity timer. Both the keyboard hot-key and the inactivity timer are programmable in the BIOS setup (timer is set to 10 minutes by default). To re-activate the system, or "Resume", the user must simply press the sleep/resume button again, or use the keyboard or mouse. Note that mouse activity will only "wake up" the system if a mouse driver is loaded. While the system is in Stand-By or "sleep" mode it is fully capable of responding to and servicing external interrupts (such as incoming fax) even though the monitor will only turn on if a user interrupt (keyboard/mouse) occurs as mentioned above. This interface is also supported by pins 1 and 2 of the PS SLEEP connector.

## ***INFRA-RED (IRDA) CONNECTOR***

Serial port 2 can be configured to support an IrDA module via a 5 pin header connector . Once configured for IrDA, the user can transfer files to or from portable devices such as laptop computers, PDA's or printers using application software such as Traveling Software's LapLink. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter.

## ***RESET***

This 2-pin header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the system will hard reset and run POST.

## **AUDIO CONNECTORS**

There are two methods of accessing the audio features on the Advanced/RH. The method installed depends on the audio option that has been selected. For business audio, audio is accessed using audio jacks provided on the motherboard. These two 1/8" jacks supply Line Out, and Mic In connections and are available through the back I/O panel.

### **MIDI/AUDIO I/O CONNECTOR**

Consumer audio is provided by using an audio riser card connected to the audio/midi connector of the motherboard. The audio riser card contains all of the necessary audio jacks (Speaker Out, Line In, Mic In) and the game port. It plugs into a 34-pin header connector on the motherboard. An example of the consumer audio riser card is shown below. The audio connectors are 1/8" stereo jacks

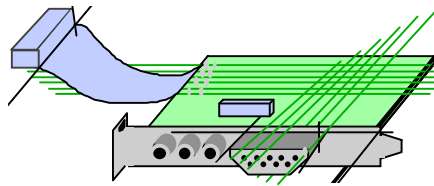


Figure 5. Advanced/RH Consumer audio I/O module

### **CD-ROM AUDIO INPUT**

A four pin connector is provided for interfacing the audio output stream from a CD-ROM reader into the audio sub-system mixer. This connector is compatible with the typical cable that is supplied with CD-ROM readers for interfacing to audio add-in cards. This feature is available in both consumer and business audio options.

## WAVE TABLE UPGRADE

An eight pin header is provided as part of the consumer audio option to connect to a wave table upgrade card for richer sound quality in both DOS and Windows environments. The wave table upgrade module is simply installed into a standard ISA slot with a cable routed to the connector.

Compatible wave table upgrade cards are available from several vendors; the ICS WaveFront upgrade module and the CrystaLake Series 2000 wave table product family add a complete General MIDI compatible music solution to the Advanced/RH based system.

For more information on CrystaLake products Contact CrystaLake Multitmedia at <http://www.teleport.com/~crystal>, or (503) 222-2603 ext. 209

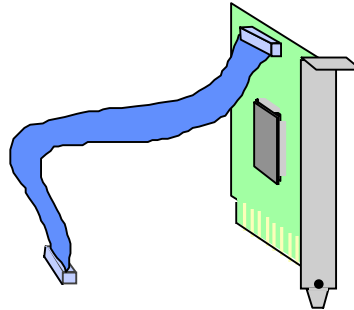
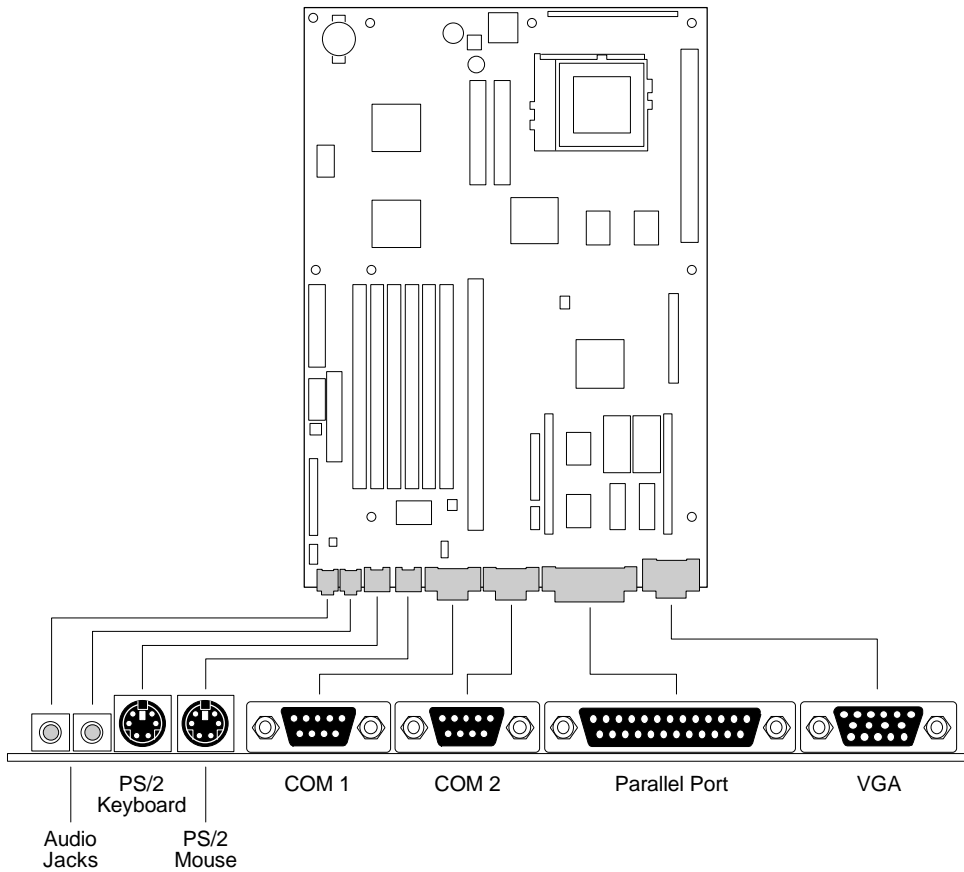


Figure 6. Advanced/RH Wave Table Upgrade module

## BACK PANEL CONNECTORS

The back panel provides external access to PS/2 style keyboard and mouse connectors as well as two serial and one parallel port, which are integrated on the Advanced/RH motherboard. If a USB connector is present, COM2 can be routed to a back panel knockout from the COM2 header on the motherboard. Audio jacks for Speaker Out and Microphone are provided for business audio on the back I/O panel. By adding an audio riser for consumer audio solutions a Midi/Game port can be made available through an ISA panel. Figure 5 shows the general location of the I/O connectors. Business audio jacks and the consumer audio/midi riser are mutually exclusive features.



OM04272

Figure 7. Back Panel I/O Connectors

# Power Consumption

Tables 3 and 4 list the measured current and voltage requirements for the Advanced/RH motherboard configured with 16 MB of DRAM. Table 5 lists the typical power consumed by the same configuration.. This information is preliminary and is provided only as a guide for calculating approximate total system power usage with additional resources added.

## Voltage

DC Voltage	Acceptable tolerance
+3.3V	+/- 5%
+5V	+/- 5%
+5V SB (stand by)	+/- 5%
-5V	+/- 5%
+12V	+/- 5%
-12V	+/- 5%

Table 3. Advanced/RH Voltage tolerance

## Current and Power

	AC (watts)	DC (amps)	
		+5v	+12v
No APM enabled			
DOS prompt	28	3.5A	160mA
Windows95 @1024x768	28	4.0A	160mA
APM enabled			
DOS prompt	24.3	2.2A	160mA
Windows95 @1024x768	24.4	2.2A	160mA
Suspended	20.3	2.2A	160mA

Table 4. Advanced/RH Power and Current Requirements

## System Configuration

System Configuration
Advanced/RH motherboard, 166 MHz Pentium Processor, 24 MB EDO RAM, 256 KB PDSRAM L2 cache, Floppy drive, 1.6 GB hard drive, Sony CDU-77E CD-ROM drive

Table 5. Power use by System Resources

# Appendix A – User-Installable Upgrades

## SYSTEM MEMORY

Supported SIMM Sizes	Bank Size	Note
512K x 32 (2 MB)	4MB	1
1M x 32 (4 MB)	8MB	
2M x 32 (8 MB)	16MB	
4M x 32 (16 MB)	32MB	
8M x 32 (32 MB)	64MB	2
16M x 32 (64MB)	128MB	2
32M x 32 (128MB)	256MB	2

Table A-1. Supported Memory SIMM Sizes and Configuration

Note 1: 512K x 32 SIMMs are supported, however, they must be double sided SIMMs

Note: 2 When using Single Sided High Density SIMMs such as 32 MB single sided, 64 MB double sided, or 128 MB SIMMs, SIMMs that have less than 32 MB per side will NOT be recognized in the system.

The Advanced/RH will support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed within the same memory bank. If Fast Page DRAM and EDO DRAM SIMMs are installed in separate banks, each bank will be optimized for maximum performance. Parity or ECC generation and detection are supported when parity SIMMs are the only SIMMs present on the motherboard. SIMM requirements are 70 ns Fast Page Mode or 60 ns EDO DRAM with tin-lead connectors.

8 MB is the minimum memory size supported by the Advanced/RH motherboard. 512 MB is the maximum memory that can be supported in any combination of SIMMs from the table.

## REAL TIME CLOCK BATTERY REPLACEMENT

The battery can be replaced with a Sanyo CR2032, or equivalent, coin cell lithium battery. This battery has a 220 mAh rating.

## CPU UPGRADE

A Type 7 Zero Insertion Force (ZIF) socket provides users with a performance upgrade path to the P54CTB OverDrive technology. LPX form factor makes it easier for the end user to replace the processor.

## GRAPHICS MEMORY UPGRADE

The ATI-264VT graphics subsystem has either 1 or 2MB of SGRAM soldered down on the base board. Video memory can be upgraded with a daughter card that is compatible with ATI PCI add in cards. Information on the memory upgrade can be obtained by contacting ATI Technologies at the numbers listed below in the HARDWARE MPEG MODULE section.

## ***HARDWARE MPEG MODULE***

ATI provides a hardware MPEG module that will work with the Advanced/RH. This module mounts onto connector J1H1, and uses mounting holes provided on the motherboard. This modul is also known as the ATI Multimedia Controller, or AMC.

For more information contact ATI Technologies at <http://www.atitech.ca>, or

(905) 882-2626 . . . . . Customer Support (voice)

(905) 882-0546 . . . . . Customer Support (fax)

(905) 764-9404 . . . . . ATI DOWNLOAD BBS (8N1)

# Appendix B – Configuration Jumper Settings

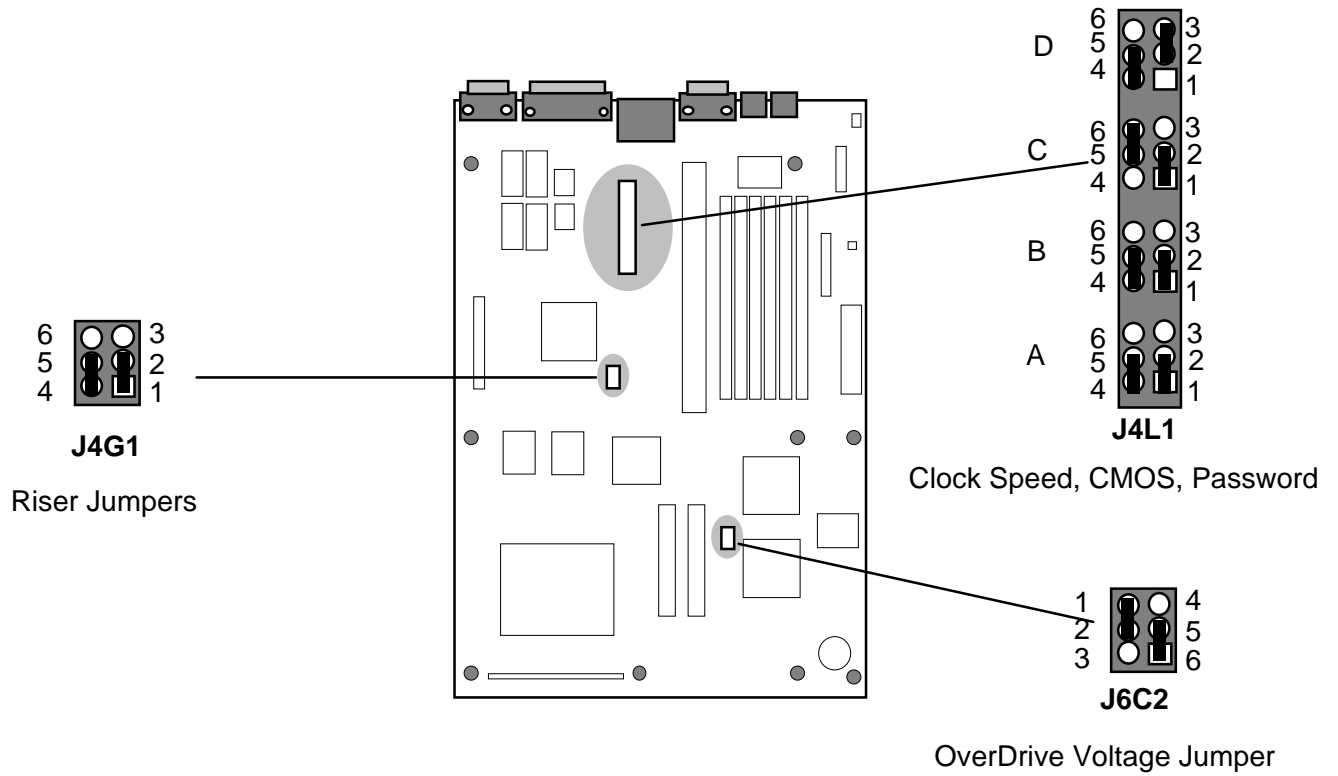


Figure B-1. Configuration Jumper locations



FUNCTION	JUMPER BLOCK	CONFIGURATION
FREQ ** (Note: These jumpers also set PCI, and ISA clock speeds.)	J4L1(C)	See table B-2 below
MULT (cpu clock multiplier)	J4L1(D)	See table B-2 below
CMOS (resets CMOS settings to default)	J4L1(A)	* 4-5 Keep (normal) 5-6 CLR (reset to default)
PSWD (Password Clear)	J4L1(A)	* 1-2 Keep (Password Enabled) 2-3 CLR (Password Clear/Disabled)
SETUP (CMOS Setup Access)	J4L1(B)	* 1-2 ENBL (Access Allowed) 2-3 DIS (Access Denied)
RISER (Select # of PCI slots on riser)	J4G1	* 1-2 & 4-5 2 SLOTS 2-3 & 5-6 3 SLOTS
Recovery	J6C2	*1-2 Normal operation 2-3 Recovery mode
Drive or OverDrive Processor Voltage **	J6C2	*5-6- Default voltage (VRE) 4-5 OverDrive processor voltage (VR)

\* Default configuration

\*\* As shipped

Table B-1. Configuration Jumper settings

## CPU CONFIGURATION - JUMPER BLOCK J4L1(C&D)

These allow the motherboard to be switched between different speeds of the Pentium processor. These jumpers also affect the PCI and ISA clock speeds according to the following table:

CPU Freq. (MHz)	Host Bus Freq. (MHz)	Host Bus pins J4L1C 1-3	Host Bus pins J4L1C 4-6	CLK Ratio	Clk Ratio pins J4L1D 1-3	Clk Ratio pins J4L1D 4-6	PCI Freq. (MHz)
166	66	1-2	5-6	5/2	2-3	5-6	33
150	60	2-3	4-5	5/2	2-3	5-6	30
133	66	1-2	5-6	2	2-3	4-5	33
120	60	2-3	4-5	2	2-3	4-5	30
100	66	1-2	5-6	3/2	1-2	4-5	33
90	60	2-3	4-5	3/2	1-2	4-5	30
75	50	2-3	5-6	3/2	1-2	4-5	25
reserved	-	1-2	4-5	-	X	X	-

Table B-2. CPU/SYSTEM speed settings (\* default setting)

The ISA clock is derived from the PCI bus clock. The BIOS automatically sets the ISA clock speed to one fourth of the PCI frequency.

PCI Frequency	ISA clock speed
25 MHz	6.25 MHz
30 MHz	7.5 MHz
33 MHz	8.25 MHz

Table B-3. ISA clock settings set by the BIOS based on PCI Clk Speed

### CMOS -J4L1 A PINS 4-6

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports "NVRAM cleared by jumper", the system can be turned off and the jumper should be returned to the 4-5 position to restore normal operation. This procedure should be done whenever the system BIOS is updated. Default is for this jumper to be on pins 4-5.

### PSWD -J4L1 A PINS 1-3

Allows system password to be cleared by moving the jumper from pins 1-2 to pins 2-3 and turning the system on. The system should then be turned off and the jumper should be returned to the 1-2 position to restore normal operation. This procedure should only be done if the user password has been forgotten. The password function is effectively disabled if this jumper is in the 2-3 position. Default is for the password to be enabled (1-2 position).

### SETUP - J4L1 B PINS 1-3

Allows access to CMOS Setup utility to be disabled by moving this jumper from the 1-2 position to the 2-3 position. Default is for access to setup to be enabled (1-2 position).

### RISER - J4G1

The riser jumper block allows routing of an extra IRQ and ID select to the riser card for an additional PCI slot to support a maximum of 3 PCI slots on a riser. Default is set for 2 PCI slots on the riser card (1-2 position and 4-5 position).

### ***DRIVE OR OVERDRIVE - J6C2***

Sets the CPU voltage to either standard voltage (3.3v), or OverDrive (3.6v). The Default setting is for a jumper to connect pin 5-6 for standard voltage. Move the jumper to connect pins 4-5 to select OverDrive voltage.

### ***RECOVERY JUMPER - J6C2***

This jumper should be set to normal mode, Pins 1-2, and should only be moved when a recovery is being performed, i.e. jumper 2-3.

## Appendix C – Memory Map

Address Range	Address Range	Size	Description
1024K-512M	100000-20000000	511M	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System run time BIOS
944K-959K	EC000-EFFFF	16K	Main BIOS Recovery Code
936K-943K	EA000-EBFFF	8K	ESCD (Plug 'N' Play configuration area)
928K-935K	E8000-E9FFF	8K	OEM LOGO (available as UMB)
896K-927K	E0000-E7FFF	32K	BIOS RESERVED (Currently available as UMB)
800-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K-799K	A0000-C7FFF	160K	Off-board video memory and BIOS
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9BFFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

Table C-1. Advanced/RH Memory Map

The table above details the Advanced/RH memory map. The ESCD area from EA000-EBFFF is not available for use as an Upper Memory Block (UMB) by memory managers. The area from E0000-E7FFF is currently not used by the BIOS and is available for use as UMB by memory managers. Parts of this area may be used by future versions of the BIOS to add increased functionality.

## Appendix D – I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX - DMA 1
0020 - 0021	2 bytes	PIIX - Interrupt
002E - 002F	2 bytes	Ultra I/O configuration
0040 - 0043	4 bytes	PIIX - Timer 1
0048 - 004B	4 bytes	PIIX - Timer 2
0060	1 byte	Keyboard Controller
0061	1 byte	PIIX - NMI, speaker
0064	1 byte	Kbd Controller,
0070, bit 7	1 bit	PIIX - Enable NMI
0070, bits 6:0	7 bits	PIIX - Real Time
0071	1 byte	PIIX - Real Time
0078	1 byte	Reserved - Brd.
0079	1 byte	Reserved - Brd.
0080 - 008F	16 bytes	PIIX - DMA Page
00A0 - 00A1	2 bytes	PIIX - Interrupt
00C0 - 00DE	31 bytes	PIIX - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE
01F0 - 01F7	8 bytes	Primary IDE Channel
0200 - 0207	8 bytes	Game Port
0220 - 022F	8 bytes	
0278 - 027B	4 bytes	Parallel Port 2
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0330 - 0331	1 bytes	MPU - 401 (MIDI)
0376	1 byte	Sec IDE Chan Cmd
0377	1 byte	Sec IDE Chan Stat
0378 - 037F	8 bytes	Parallel Port 1

Address (hex)	Size	Description
0388 - 038B	4 bytes	
03B4 - 03B5	2 bytes	
03BA	1 byte	
03BC - 03BF	4 bytes	Parallel Port 3
03C0 - 03CA	12 bytes	
03CC	1 byte	
03CE - 03CF	2 bytes	
03D4 - 03D5	2 bytes	
03DA	1 byte	
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel
03F6	1 byte	Pri IDE Chan
03F7 (Write)	1 byte	Floppy Chan 1
03F7, bit 7	1 bit	Floppy Disk
03F7, bits 6:0	7 bits	Pri IDE Chan
03F8 - 03FF	8 bytes	On-Board Serial
LPT + 400h	8 bytes	ECP port, LPT
04D0 - 04D1	2 bytes	Edge/Level
0608 - 060B	4 bytes	
0CF8*	4 bytes	PCI Config
0CF9	1 byte	Turbo & Reset
0CFC-0CFF	4 bytes	PCI Config Data
0FF0 - 0FF7	8 bytes	
FF00 - FF07	8 bytes	IDE Bus Master
FFA0 - FFA7	8 bytes	IDE primary
FFA8 - FFAF	8 bytes	IDE secondary

Table D-1. Advanced/RH I/O Address Map

I/O Port 78 is reserved for BIOS use. Port 79 is a read only port, the bit definitions are shown below in Table D-2.

Bit #	Description	Bit = 1	Bit = 0
0	Reserved	n/a	n/a
1	Soft Off capable power supply present	No	Yes
2	Onboard Audio present	Yes	No
3	External CPU clock	Table B-2	Table B-2
4	External CPU clock	Table B-2	Table B-2
5	Setup Disable	Enable access	Disable access
6	Clear CMOS	Keep values	Clear values
7	Password Clear	Keep password	Clear password

Table D-2. Advanced/RH Port 79 Definition

## Appendix E – PCI Configuration Space Map

The 82430HX PCIset uses Configuration Mechanism 1 to access PCI configuration space. The PCI Configuration Address register is a 32-bit register located at CF8h, the PCI Configuration Data register is a 32-bit register located at CFCh. These registers are only accessible by full DWORD accesses. The table below lists the PCI bus and device numbers used by the motherboard.

Bus Number	Dev Number (hex)	Func. Number	Description
00	00	00	Intel 82437HX
00	07	00	Intel 82371FB (PIIX 3) PCI/ISA bridge
00	07	01	Intel 82371FB (PIIX 3) IDE Bus Master
00	08	00	Video [ATI]
00	0B	00	Option PCI expansion Slot for 3 Slot Riser
00	11	00	PCI Expansion Slot
00	13	00	PCI Expansion Slot

Table E-1. Advanced/RH PCI Configuration. Space Map

## Appendix F – Interrupts & DMA Channels

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Audio
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available
10	User available
11	Audio
12	Onboard Mouse Port
13	Reserved, Math coprocessor
14	Primary IDE
15	Secondary IDE if present, else user available

Table F-1. Advanced/RH Interrupts

DMA	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port (for ECP/EPP Config.)
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

Table F-2. Advanced/RH DMA Map

## Appendix G – Connectors

### POWER SUPPLY

#### PRIMARY POWER J9H1

Pin	Name	Function
1	PWRGD	Power Good
2	+5 V	+ 5 volts Vcc
3	+12 V	+ 12 volts
4	-12 V	- 12 volts
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	-5 V	-5 volts
10	+5 V	+ 5 volts Vcc
11	+5 V	+ 5 volts Vcc
12	+5 V	+ 5 volts Vcc

#### PCI (3.3V) POWER J9J1 NOT POPULATED

Pin	Name	Function
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	+3.3 V	+ 3.3 volts
5	+3.3V	+ 3.3 volts
6	+3.3 V	+ 3.3 volts



## FRONT PANEL–J3A1

### SLEEP/RESUME

Pin	Signal Name
15	SW_ON
16	GND
17	SLEEP
18	SLEEPPU
19	KEY

### INFRA-RED

Pin	Signal Name
25	CONIRRX
24	IRTX
23	GND
22	IRRIN
21	NC
20	VCC

### POWER INTERFACE HARD DRIVE LED (DISK)

Pin	Signal Name
14	PWRPU
13	PWDRV
12	HDA
11	HDPU

### POWER INTERFACE CPU FAN

	Signal Name
3	Ground
2	+12V
31	Ground

### POWER LED / KEYLOCK

	Signal Name
10	PWDRV
9	NC
8	PWRPU
7	KEY

### POWER INTERFACE SPEAKER CONNECTOR

Pin	Signal Name
29	GND
28	Key
27	SPKSRC
26	SPKOUT

### POWER INTERFACE RESET CONNECTOR

Pin	Signal Name
6	Key
5	RESET
4	Ground

## BACK PANEL I/O

### PS/2 KEYBOARD J8N1 & MOUSE PORTS J7N1

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	Vcc
5	Clock

### SERIAL PORTS COM1 J6N2 & COM2 J5N1

Pin	Signal Name
1	DCD
2	Serial In - (SIN)
3	Serial Out - (SOUT)
4	DTR-
5	GND
6	DSR-
7	RTS-
8	CTS-
9	RI

### USB J5N2 REPLACES COM2

Pin	Signal Name
1	VCC
2	USBP0-
3	USBP0
4	GND
5	VCC
6	USBP1-
7	USBP1
8	GND

### LINE OUT J9N2

Pin	Signal Name
1	Line Out

### MIC IN J8N2

Pin	Signal Name
1	Line Out

### PARALLEL PORT J3N1

Signal Name	Pin	Pin	Signal Name
STROBE-	1	14	AUTO FEED-
Data Bit 0	2	15	ERROR-
Data Bit 1	3	16	INIT-
Data Bit 2	4	17	SLCT IN-
Data Bit 3	5	18	Ground
Data Bit 4	6	19	Ground
Data Bit 5	7	20	Ground
Data Bit 6	8	21	Ground
Data Bit 7	9	22	Ground
ACK-	10	23	Ground
BUSY	11	24	Ground
PE (Paper End)	12	25	Ground
SLCT	13	26	N.C.

### VIDEO MONITOR PORT J1N1

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No Connect
5	Ground
6	Ground
7	Ground
8	Ground
9	No Connect
10	Ground
11	No Connect
12	MONID1
13	Horizontal Sync.
14	Vertical Sync.
15	MONID2

## PERIPHERALS

### IDE CONNECTORS J5C1 & J6C1

Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DDRQ0 (DDRQ1)	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	Vcc pull-up
DDACK0 (DDACK1)-	29	30	Ground
IRQ14 (IRQ15)	31	32	NC
Addr 1	33	34	NC
Addr 0	35	36	Addr 2
Chip Select 1P (1S)-	37	38	Chip Select 3P (3S)-
Activity-	39	40	Ground

### FLOPPY CONNECTOR J9K1

Signal Name	Pin	Pin	Signal Name
Ground	1	2	DENSEL
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable A-
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable B-
MSEN1	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
MSEN0	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Diskette Change-

## MULTIMEDIA

### MIDI/AUDIO CONNECTOR J9L1

Signal Name	Pin	Pin	Signal Name
+5 V	1	2	+5 V
JoyStick But0	3	4	JoyStick But2
JoyStick X1	5	6	JoyStick X2
Ground	7	8	MIDI Out
Ground	9	10	JoyStick Y2
JoyStick Y1	11	12	JoyStick But3
JoyStick But1	13	14	MIDI In
+5 V	15	16	Key
Key	17	18	Key
Line Out Right	19	20	Ground
Right Speaker	21	22	Ground
Left Speaker	23	24	Key
Line Out Left	25	26	Ground
Line In Right	27	28	-12 V
Line In Left	29	30	Ground
Mic In	31	32	+12 V
Ground	33	34	Ground

(NOT A MM OPTION)

### WAVE TABLE UPGRADE CONNECTOR J9N1

Pin	Signal Name
1	Wave Right
2	Ground
3	Wave Left
4	Ground
5	Key
6	Ground
7	MIDI_Write
8	MIDI_OUT

### TELEPHONY CONNECTOR J9L2

Pin	Signal Name
1	Ground
2	Mono Out
3	Mic In
4	No Connect

### ATI MULTI-MEDIA CON. (AMC) J1H1

Signal Name	Pin	Pin	Signal Name
Ground	1	2	Data 0
Ground	3	4	Data 1
Ground	5	6	Data 2
Data enable	7	8	Data 3
Sync enable	9	10	Data 4
PCLK enable	11	12	Data 5
SDA	13	14	Data 6
Ground	15	16	Data 7
Ground	17	18	DCLK
Ground	19	20	BLANK
VFCNSNS	21	22	HSYNC
SCL	23	24	VSYSN
KEY	25	26	GND
key	27	28	key
VCC	29	30	SA
RST	31	32	SNRDY
SAD	33	34	VMASK
NC	35	36	
GND	37	38	+12V
NC	39	40	NC

### CD-ROM AUDIO INTERFACE J6N1

Pin	Signal Name
1	Ground
2	CD-LEFT
3	Ground
4	CD-Right

### MIDI/GAME PORT (ON AUDIO RISER)

Pin	Signal Name
1	Vcc
2	JSBUT0
3	JSX1R
4	GND
5	GND
6	JSY1R
7	JSBUT1
8	Vcc
9	Vcc
10	JSBUT2
11	JSX2R
12	MIDI-OUT-R
13	JSY2R
14	JSBUT3
15	MIDI-IN-R

**PCI / ISA RISER (J6J2)**

Signal Name	Pin	Pin	Signal Name
IOCHK-	A1	B1	GND
SD7	A2	B2	RSTDRV
SD6	A3	B3	Vcc
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	GND
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRESH-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	Vcc
SA1	A30	B30	OSC
SA0	A31	B31	GND
SBHE-	C1	D1	MEMCS16-
LA23	C2	D2	IOCS16-
LA22	C3	D3	IRQ10
LA21	C4	D4	IRQ11
LA20	C5	D5	IRQ12
LA19	C6	D6	IRQ15
LA18	C7	D7	IRQ14
LA17	C8	D8	DACK0-
MEMR-	C9	D9	DRQ0
MEMW-	C10	D10	DACK5-
SD8	C11	D11	DRQ5
SD9	C12	D12	DACK6-
SD10	C13	D13	DRQ6
SD11	C14	D14	DACK7-
SD12	C15	D15	DRQ7
SD13	C16	D16	Vcc
SD14	C17	D17	MASTER-
SD15	C18	D18	GND

Signal Name	Pin	Pin	Signal Name
GND	E1	F1	GND
GND	E2	F2	GND
PCIINT0-	E3	F3	PCIINT2-
PCIINT1-	E4	F4	PCIINT3-
Vcc	E5	F5	Vcc
Key	E6	F6	Key
Vcc	E7	F7	Vcc
PCIRST-	E8	F8	PCLKF
GNT0-	E9	F9	GND
REQ0-	E10	F10	GNT1-
GND	E11	F11	GND
PCLKE	E12	F12	REQ1-
GND	E13	F13	AD31
AD30	E14	F14	AD29
3.3V	E15	F15	3.3V
Key	E16	F16	Key
3.3V	E17	F17	3.3V
AD28	E18	F18	AD27
AD26	E19	F19	AD25
AD24	E20	F20	CBE3-
AD22	E21	F21	AD23
AD20	E22	F22	AD21
AD18	E23	F23	AD19
3.3V	E24	F24	3.3V
Key	E25	F25	Key
3.3V	E26	F26	3.3V
AD16	E27	F27	AD17
FRAME-	E28	F28	IRDY-
CBE2-	E29	F29	DEVSEL-
TRDY-	E30	F30	PLOCK-
STOP-	E31	F31	PERR-
SDONE	G1	H1	SERR-
SBO-	G2	H2	AD15
CBE1-	G3	H3	AD14
PAR	G4	H4	AD12
GND	G5	H5	GND
Key	G6	H6	Key
GND	G7	H7	GND
AD13	G8	H8	AD10
AD11	G9	H9	AD8
AD9	G10	H10	AD7
CBE0-	G11	H11	AD5
AD6	G12	H12	AD3
AD4	G13	H13	AD1
AD2	G14	H14	AD0
Key	G15	H15	Key
Vcc	G16	H16	Vcc
Vcc	G17	H17	Vcc
GND	G18	H18	GND
GND	G19	H19	GND

### CELP 2.1 CONNECTOR (J1D1)

Signal Name	Pin	Pin	Signal Name
GND	1	41	D58
TIO0	2	42	D56
TIO2	3	43	GND
TIO6	4	44	D54
TIO4	5	45	D52
TIO8	6	46	D50
VCC3	7	47	D48
TWE*	8	48	GND
CADS*	9	49	D46
GND	10	50	D44
CWE4*	11	51	D42
CWE6*	12	52	VCC3
CWE0*	13	53	D40
CWE2*	14	54	D38
VCC3	15	55	D36
CCS*	16	56	GND
GWE*	17	57	D34
BWE*	18	58	D32
GND	19	59	D30
A3	20	60	VCC3
A7	21	61	D28
A5	22	62	D26
A11	23	63	D24
A16	24	64	GND
VCC3	25	65	D22
A18	26	66	D20
GND	27	67	D18
A12	28	68	VCC3
A13	29	69	D16
ADSP*	30	70	D14
ECS1*	31	71	D12
ECS2*	32	72	GND
PD1	33	73	D10
PD3	34	74	D8
GND	35	75	D6
CLK1	36	76	VCC3
GND	37	77	D4
D62	38	78	D2
VCC3	39	79	D0
D60	40	80	GND

Signal Name	Pin	Pin	Signal Name
GND	81	121	D59
TIO1	82	122	D57
TIO7	83	123	GND
TIO5	84	124	D55
TIO3	85	125	D53
TI09	86	126	D51
VCC5	87	127	D49
TIO10	88	128	GND
CADV*	89	129	D47
GND	90	130	D45
COE*	91	131	D43
CWE5*	92	132	VCC5
CWE7*	93	133	D41
CWE1*	94	134	D39
VCC5	95	135	D37
CWE3*	96	136	GND
CAB3	97	137	D35
CALE	98	138	D33
GND	99	139	D31
RSVD	100	140	VCC5
A4	101	141	D29
A6	102	142	D27
A8	103	143	D25
A10	104	144	GND
VCC5	105	145	D23
A17	106	146	D21
GND	107	147	D19
A9	108	148	VCC5
A14	109	149	D17
A15	110	150	D15
RSVD	111	151	D13
PD0	112	152	GND
PD2	113	153	D11
PD4	114	154	D9
GND	115	155	D7
CLK0	116	156	VCC5
GND	117	157	D5
D63	118	158	D3
VCC5	119	159	D1
D61	120	160	GND

# Appendix-H Motherboard BIOS

The Advanced/RH motherboard uses an Intel BIOS, which is stored in Flash EEPROM and easily upgraded using a floppy disk-based program. BIOS upgrades can be down loaded from the Intel Applications Support electronic bulletin board service, or the Intel FTP site. In addition to the Intel BIOS, the Flash EEPROM also contains the Setup utility, Power-On Self Tests (POST), APM 1.1, the PCI auto-configuration utility, and Windows 95 ready Plug 'N' Play. This motherboard also supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the Advanced/RH will be identified as 1.00.01.CV0.

Information on BIOS functions can be found in the *IBM PS/2 and Personal Computer BIOS Technical Reference* published by IBM, and the *ISA and EISA Hi-Flex AMIBIOS Technical Reference* published by AMI. Both manuals are available at most technical bookstores.

## FLASH MEMORY IMPLEMENTATION

The Intel 2 Mb Flash component is organized as 32 x 8 (256 KB). The Flash device is divided into five areas, as described in Table H-1.

System Address		FLASH Memory Area
F0000H	FFFFFH	64 KB Main BIOS
EC000H	EFFFFH	16 KB System BIOS RECOVERY
EA000H	EBFFFH	8 KB Plug 'N' Play ESCD Storage Area
E8000H	E9FFFH	8 KB OEM Logo Area
E0000H	E7FFFH	32 KB System BIOS Reserved during boot

Table H-1. Flash memory organization

## BIOS UPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. BIOS upgrades are available to be down loaded from the secure section on the Intel bulletin board, or Intel's FTP site.

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed; or
- The BIOS in the Flash device can be compared with a file to ensure the system has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

## **SETUP UTILITY**

The ROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The Setup utility is accessible only during the Power-On Self Test (POST) by pressing the <F1> key after the POST memory test has begun and before boot begins. A prompt may be enabled that informs users to press the <F1> key to access Setup. A jumper setting (See table B-1 in appendix B) on the motherboard can be set to prevent user access to Setup for security purposes.

## **PCI AUTO-CONFIGURATION**

The PCI auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of PCI cards to the system without user intervention (Plug 'N' Play). When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space and other parameters. PCI interrupts are distributed to available ISA interrupts that have been not been assigned to an ISA card, or system resources. Those interrupts left set to "available" in the CMOS setup will be considered free for PCI add-in card use. It is nondeterministic as to which PCI interrupt will be assigned to which ISA IRQ.

The PCI Auto-Configuration function complies with version 2.10 of the PCI BIOS specification. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

PCI specification 2.1 for add-in card auto-configuration is also a part of the Plug 'N' Play BIOS. Peer-to-peer hierarchical PCI Bridge 1.0 is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

## **ISA PLUG 'N' PLAY**

The BIOS incorporates ISA Plug 'N' Play capabilities as delivered by Plug 'N' Play Release 1.0A (Plug 'N' Play BIOS V.. 1.0A, ESCD V.. 1.03). When used in conjunction with the ISA Configuration Utility (ICU) for DOS or Windows 3.x, the system allows auto-configuration of Plug 'N' Play ISA cards, PCI cards, and resource management for legacy ISA cards. Because the BIOS supports configuring devices across PCI bridges, release 1.41 or greater of the ICU must be used with the Advanced/RH motherboard to properly view and change system settings. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position (See Appendix B for jumper details).

The Advanced/RH BIOS also has a setup option to support the Windows 95 run time plug and play utilities. When this option is selected, only devices required to boot the system are assigned resources by the BIOS. Device Node information is available for all devices to ensure compatibility with Windows 95.

Copies of the IAL Plug 'N' Play specification may be obtained from the Intel BBS or from CompuServe by typing Go PlugPlay.

## **ADVANCED POWER MANAGEMENT**

The Advanced/RH BIOS has support for both 1.0 and 1.1 Advanced Power Management (APM). The version of APM drivers loaded in the operating system by the user will determine what specification the BIOS will adhere too. In either case the energy saving Stand By mode can be initiated by a keyboard hot key sequence set by the user, a time-out period set by the user, or by a suspend/resume button tied to the front panel sleep connector.

When in Stand-by mode, the Advanced/RH motherboard reduces power consumption by utilizing the Pentium processor's System Management Mode (SMM) capabilities and also spinning down hard drives and turning off VESA DPMS compliant monitors. The user may select which DPMS mode (Stand By, Suspend, or Off) to send to the monitor in setup. The ability to respond to external interrupts is fully maintained while in Stand-by mode allowing the system to service requests such as in-coming FAX's or network messages while unattended. Any keyboard or mouse activity brings the system out of the energy saving Stand By mode. When this occurs the monitor and IDE drives are turned back on immediately.



APM is enabled in BIOS by default, however, the system must be configured with an APM driver (such as Power.exe for DOS or vpowerd.386 for Windows 3.x) in order for the system power saving features to take effect. Windows 95 will enable APM automatically upon detecting the presence of the APM BIOS.

## **LANGUAGE SUPPORT**

The BIOS setup screen and help messages are supported in 32 languages. There are 5 languages translated at this time for use; American English, German, Italian, French, and Spanish. Translations of other languages will be available at a later date.

With a 1 Mb Flash BIOS, only one language can be resident at a time. The default language is American English, and will always be present unless another language is programmed into the BIOS using the Flash Memory Update Program (FMUP) available on the Intel BBS.

## **PCI IDE**

The two local bus IDE connectors with independent I/O channel support are setup up automatically by the BIOS if the user selects "Autoconfiguration" in setup. The IDE interface supports PIO Mode 3 and Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices. The BIOS will determine the capabilities of each drive and configure them to optimize capacity and performance. For the high capacity hard drives typically available today, the drive will be automatically configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive. The user is able to override the auto-configuration options by using the manual mode setting.

## **BOOT OPTIONS**

Booting from CD-ROM is supported in adherence to the "El Torito" bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the *Boot Options* field in setup, *CD-ROM* is one of four possible boot devices defined in priority order. The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device and CD-ROM to be the third device. The fourth device is set to *disabled* in the default configuration. The user can also select *network* as a boot device. The network option allows booting from a network add-in card with a remote boot ROM installed.

NOTE: A copy of "El Torito" is available on Phoenix Web page.

## **FLASH LOGO AREA**

Advanced/RH supports a 4 KB programmable flash user area located at EC000-ECFFF. An OEM may use this area to display a custom logo. The Advanced/RH BIOS accesses the user area just after completing POST. A utility called USRLUTIL is available on the Intel BBS to assist with installing a logo into flash for display during POST.

## **SECURITY FEATURES**

### **Administrative Password**

If enabled, the administrative password protects all sensitive Setup options from being changed by a user unless the password is entered. Without the proper password the user will be able to configure only the User password and the power management hot key fields. The User password does not alter the protection provided by the Administrative password.

### **User Password**

The User Password feature provides security, preventing the system from booting or entering setup unless the user selected password is entered during the boot process. The user password can be set using the Setup utility, and must be entered prior to peripheral boot or keyboard/mouse operation.

If the password is forgotten, it can be cleared by turning off the system and setting the "password clear" jumper (See Appendix B: table B-1) to the ON position and briefly powering up the system. The Administrative password and User password are both cleared by this operation. After returning the jumper to the "password keep" position, a new password can be entered in Setup to re-enable password protection.

### Setup Enable Jumper

A motherboard configuration jumper (See Appendix B: table B-1) controls access to the BIOS Setup utility. By setting the jumper to the disable position, the user is prevented from accessing the Setup utility during the Power-On Self Test or at any other time. The message prompting the user to press <F1> to enter setup is also disabled.

### Floppy Write Protect

A BIOS setup option under "floppy options" prevents writing to any attached floppy drives. This field is controlled by the administrative password and can be altered only if the administrative password (if set) is entered.

## Appendix I – PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device and function information.

```
<'NVRAM Checksum Error, NVRAM Cleared'>, \ ; String  
<'System Board Device Resource Conflict'>, \ ; String  
<'Primary Output Device Not Found'>, \ ; String  
<'Primary Input Device Not Found'>, \ ; String  
<'Primary Boot Device Not Found'>, \ ; String  
<'NVRAM Cleared By Jumper'>, \ ; String  
<'NVRAM Data Invalid, NVRAM Cleared'>, \ ; String  
<'Static Device Resource Conflict'>, \ ; String
```

The following messages chain together to give a message such as:

```
"PCI I/O Port Conflict: Bus: 00, Device 0D, Function: 01".
```

If and when more than 15 PCI conflict errors are detected the log full message is displayed.

```
<'PCI I/O Port Conflict:'>, \ ; String  
<'PCI Memory Conflict: '>, \ ; String  
<'PCI IRQ Conflict: '>, \ ; String  
<' Bus '>, \ ; String  
<', Device '>, \ ; String  
<', Function '>, \ ; String  
<',PCI Error Log is Full.'>, \ ; String  
<'Floppy Disk Controller Resource Conflict '>, \ ; Text  
<'Primary IDE Controller Resource Conflict '>, \ ; Text  
<'Secondary IDE Controller Resource Conflict '>, \ ; Text  
<'Parallel Port Resource Conflict '>, \ ; Text  
<'Serial Port 1 Resource Conflict '>, \ ; Text  
<'Serial Port 2 Resource Conflict '>, \ ; Text
```

## Appendix J– AMIBIOS Error messages and Beep Codes

Errors can occur during POST (Power On Self Test) which is performed every time the system is powered on. Fatal errors, which prevent the system from continuing the boot process, are communicated through a series of audible beeps. Other errors are displayed in the following format:

ERROR Message Line 1

ERROR Message Line 2

For most displayed error messages, there is only one message. If a second message appears, it is "RUN SETUP". If this message occurs, press <F1> to run AMIBIOS Setup.

### **BEEP CODES**

Beeps	Error Message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	Parity is not supported on this product, will not occur.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The CPU on the motherboard generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) may be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The CPU generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Rd/Wrt Error	The shutdown register for CMOS RAM failed.
1 LONG 3 SHORT	VIDEO ERROR	Video Controller failure

### **ERROR MESSAGES**

Error Message	Explanation
8042 Gate - A20 Error Address Line Short!	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042. Error in the address decoding circuitry on the motherboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	Most AT systems include two timers. There is an error in timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run AMIBIOS Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run AMIBIOS Setup.

## ERROR MESSAGES (CONT.)

CMOS Time and Date Not Set	Run Standard CMOS Setup to set the date and time in CMOS RAM.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	The display jumper is not implemented on this product, this error will not occur.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the system. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard. Set the Keyboard option in Standard CMOS Setup to Not Installed to skip the keyboard POST routines.
KB/Interface Error	There is an error in the keyboard connector.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is:  OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX)  XXXX is the hex address where the error occurred.
On Board Parity Error	Parity is not supported on this product, this error will not occur.
Parity Error ????	Parity error in system memory at an unknown address.

## ISA NMI MESSAGES

ISA NMI Message	Explanation
Memory Parity Error at xxxxx	Memory failed. If the memory location can be determined, it is displayed as xxxxx. If not, the message is Memory Parity Error ????.
I/O Card Parity Error at xxxxx	An expansion card failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O Card Parity Error ????.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

## Appendix K – Soft-off Control

The Advanced/RH design supports Soft-off control via the SMM code in the BIOS. The CS1 pin out of the National 306B Ultra I/O controller is connected to the Soft-off control line in our power supply circuit.

The registers in the Ultra I/O controller that sets the I/O address and control of the CS1 pin is NOT setup until the SMM code is activated. The code performs the following operations:

OUT 0Ch to I/O port 2Eh  
OUT 75h to I/O port 2Fh

OUT 11h to I/O port 2Eh  
OUT 00h to I/O port 2Fh

OUT 0Dh to I/O port 2Eh  
OUT A0h to I/O port 2Fh

After setting the above registers, any read operation to I/O location 75H will trigger the Soft-off circuit and turn the power supply off.

# Appendix L – Environmental Standards

## MOTHERBOARD SPECIFICATIONS

Parameter	Condition	Specification		
Temperature	Non-Operating	-40°C to +70°C		
	Operating	+0°C to +55°C (minimum air flow of 200 LFM)		
DC Voltage	+5 V	±5 %		
	-5 V	±5 %		
	+12 V	±5 %		
	-12 V	±5 %		
Vibration	Unpackaged	5 Hz to 20 Hz : 0.01g <sup>2</sup> Hz sloping up to 0.02 g <sup>2</sup> Hz 20 Hz to 500 Hz : 0.02g <sup>2</sup> Hz (flat)		
	Packaged	10 Hz to 40 Hz : 0.015g <sup>2</sup> Hz (flat) 40 Hz to 500 Hz : 0.015g <sup>2</sup> Hz sloping down to 0.00015 g <sup>2</sup> Hz		
Shock	Unpackaged	50 G trapezoidal waveform Velocity change of 170 inches/sec.		
	Packaged	Half Sine 2 millisecond	Free Fall	Velocity
		Product	(Height in inches)	(Change (in / sec))
		(Weight)		
		< 20 lb.	36	167
		21 - 40	30	152
		41 - 80	24	136
		81 - 100	18	118

Table L-1. Environmental standards

## Appendix M – Reliability Data

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55C.

Advanced/RH motherboard

72706 Hours



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